Recent Advances in High κ Gate Dielectrics

For Si and Compound Semiconductors

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Materials	Characterizations	Si and GaAs Device and Processing
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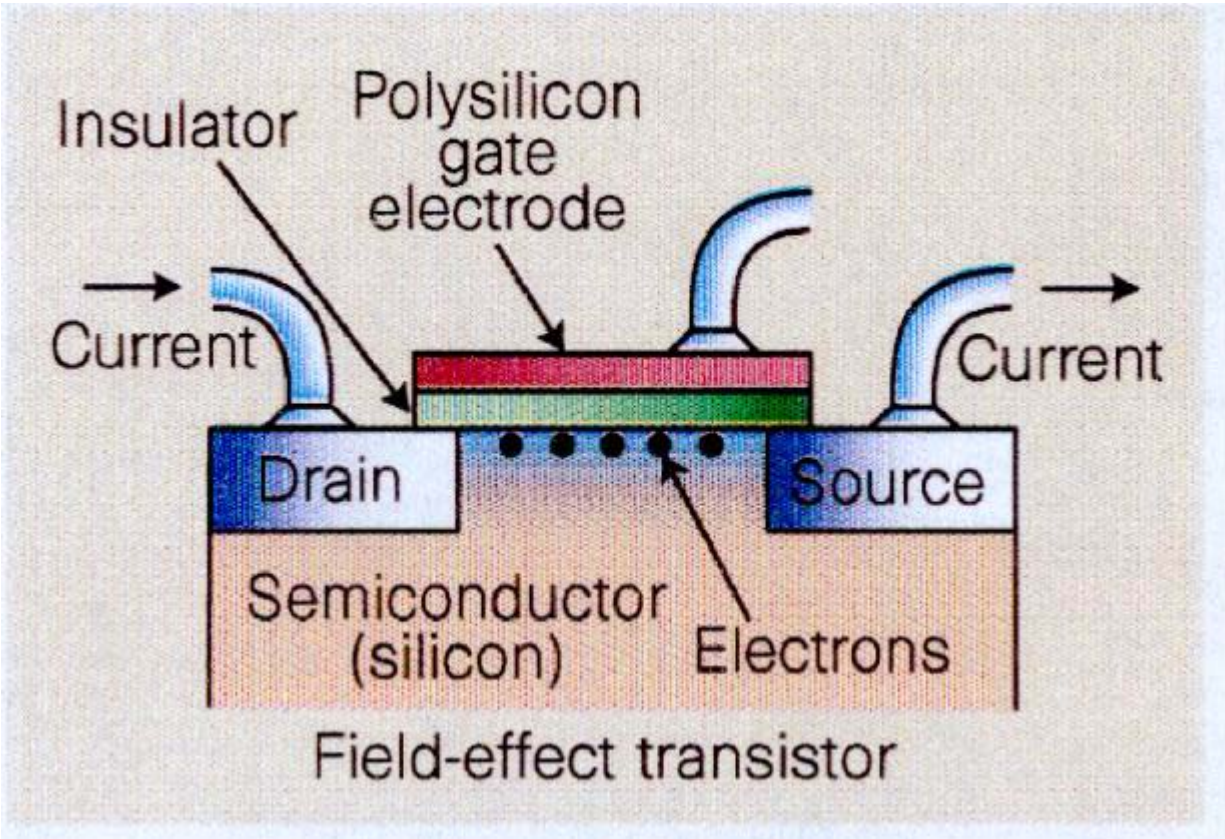
OUTLINES

- Introduction : The call for alternative high κ gate dielectrics for 45 nm Si CMOS by year 2010
  - * Fundamental materials requirements
  - * Processing integration issues for Si CMOS scaling
- The discovery of compound semiconductors passivation using $Ga_2O_3(Gd_2O_3)$ and Gd_2O_3 oxides
- Summary of results and achievements of high κ gate dielectrics of Gd_2O_3 and Y_2O_3 on Si
- New research programs
- Anticipated accomplishments
  - * Technology
  - * Research

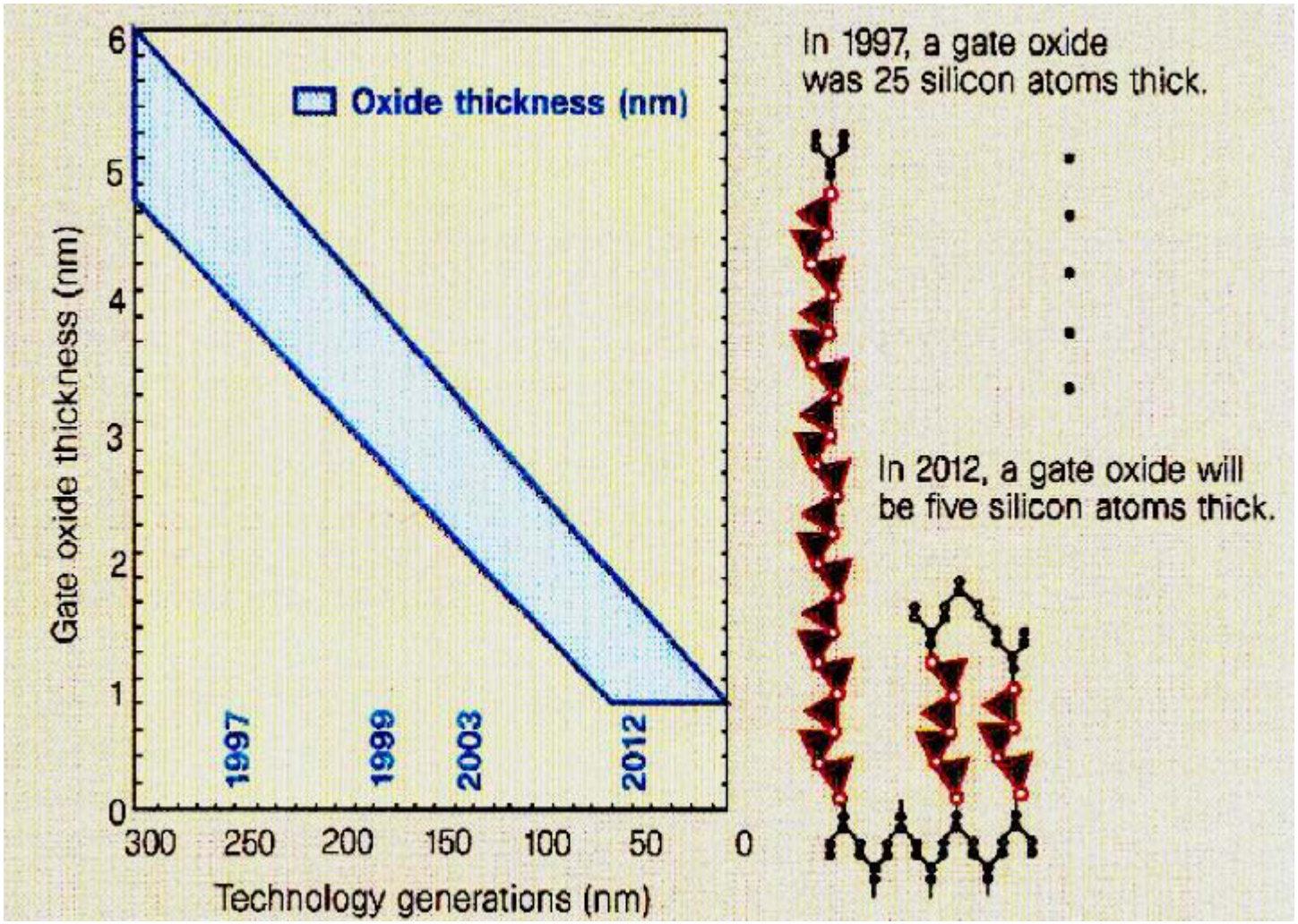
INTRODUCTION

The Call for Alternative High κ Gate Dielectrics for Si CMOS

MOSFET (互補式金氧場效電晶體)

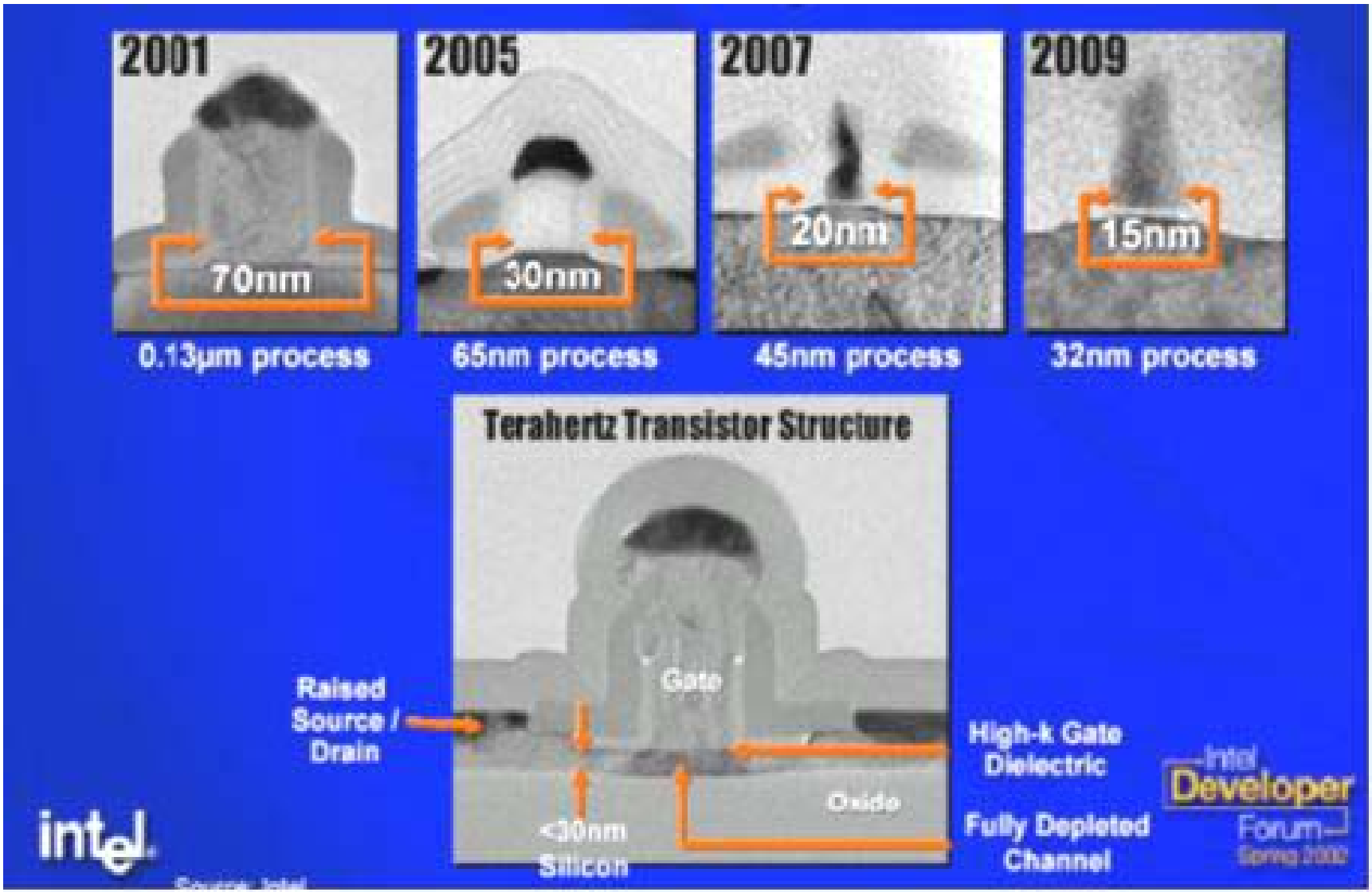


1960 Kahng and Atalla, First MOSFET
1970 First IC, 1 kbit, 750 khz microprocessor


Oxide thickness (nm)
Gate oxide thickness (nm)
6
5
4
3
2
1
0
1997
1999
2003
2012
300
250
200
150
100
50
0
Technology generations (nm)
In 1997, a gate oxide was 25 silicon atoms thick.
In 2012, a gate oxide will be five silicon atoms thick.

Moore's Law

Intel Semiconductor CMOS Roadmap



When do we stop ?

Reliability: ~~25~~ ~~22~~ ~~18~~ 16 Å

processing and yield issue

Tunneling : 15 Å

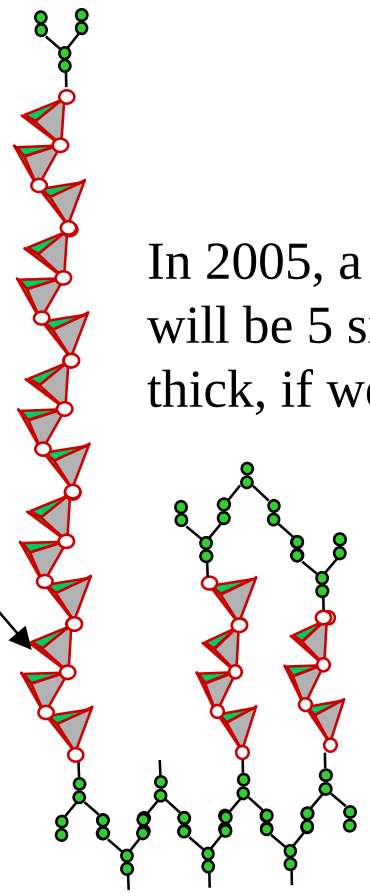
Design Issue: chosen for 1A/cm^2 leakage
I_{on}/I_{off} >> 1 at 12 Å

Bonding:

Fundamental Issues-

- how many atoms do we need to get bulk-like properties?
- Is the interface electronically abrupt?
- Can we control roughness?

In 1997, a gate oxide was 25 silicon atoms thick.



In 2005, a gate oxide will be 5 silicon atoms thick, if we still use SiO_2

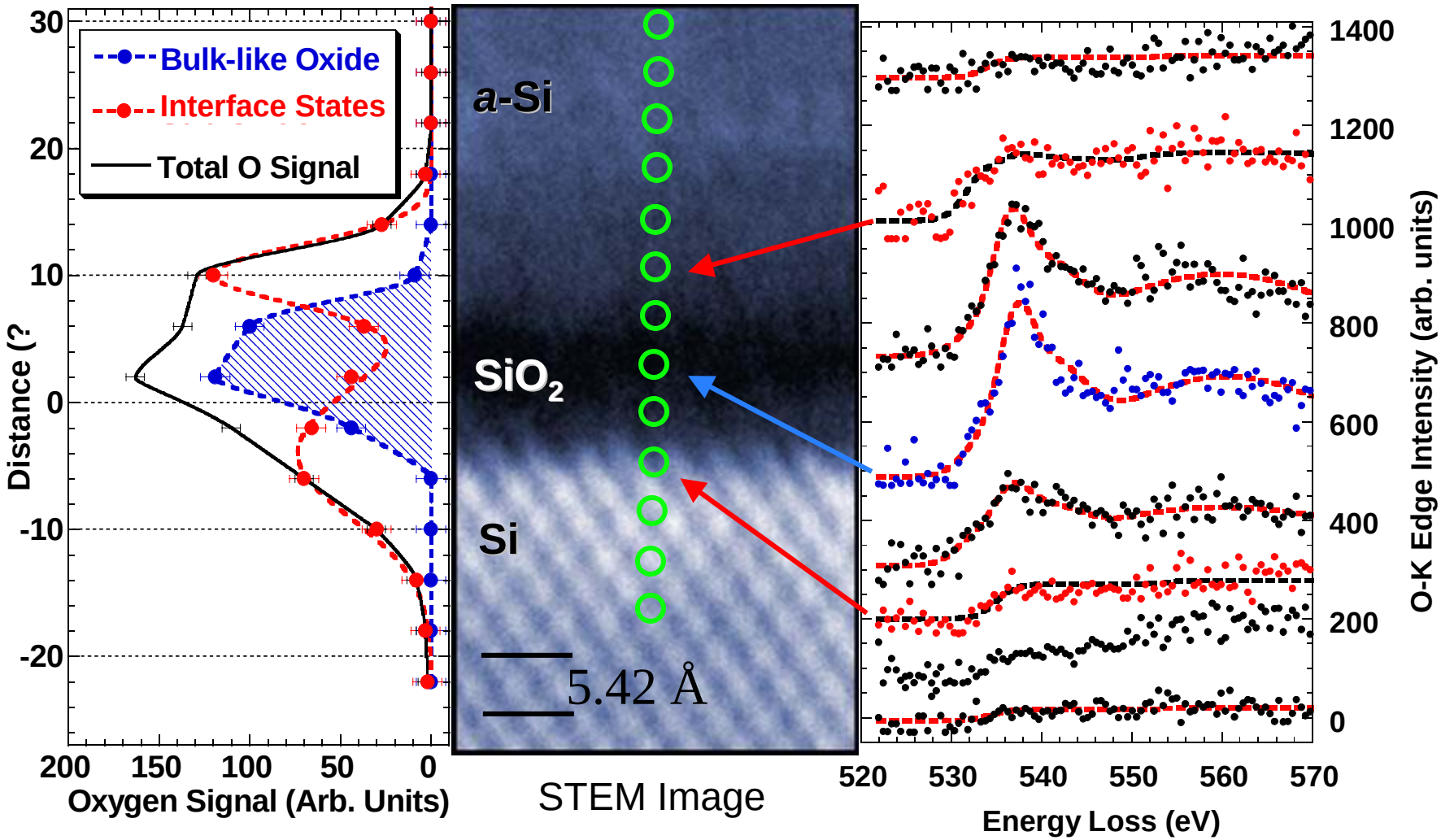
and at least 2 of those 5 atoms will be at the interfaces.

Oxygen Bonding from EELS

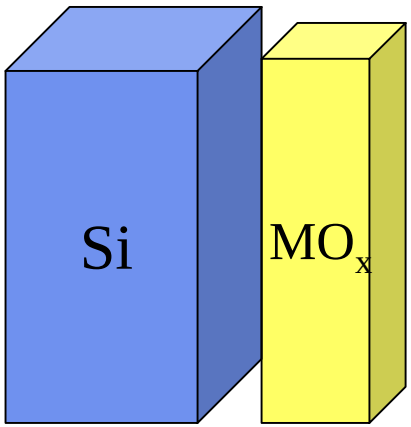
Nominal 1.1 nm SiO_2:

0.8 - 1 nm Bulk SiO_2

1.6 nm wide oxygen profile



Fundamental Materials Selection Guidelines



$Si + MO_x \rightarrow M + SiO_2$

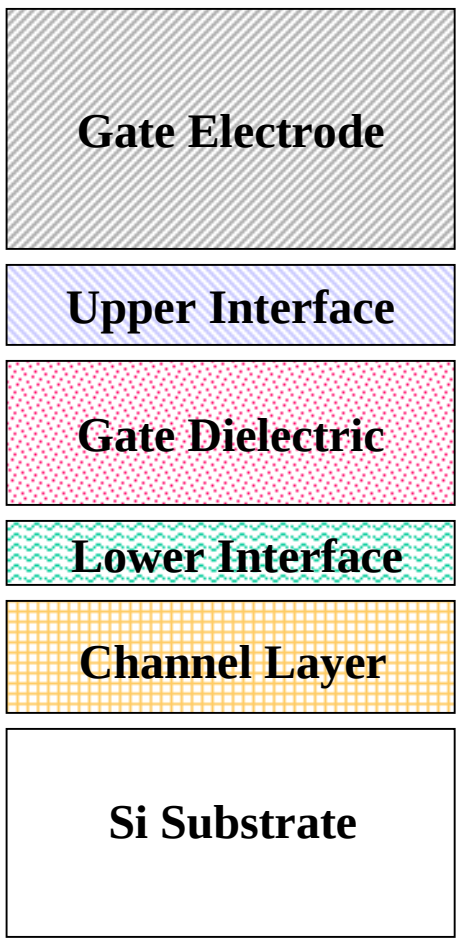
$Si + MO_x \rightarrow MSi_2 + SiO_2$

$Si + MO_x \rightarrow MSiO_x + SiO_2$

- Thermodynamic stability in contact with Si to 750ºC and higher. **(Hubbard and Schlom)** **Alkaline earth oxide, IIIB, IVB oxide and rare earth oxide**
- Dielectric constant, band gap, and conduction band offset
- Defect related leakage, substantially less than SiO_2 at $t_{eq} < 1.5$ nm
- Low interfacial state density $D_{it} < 10^{11}\ eV^{-1}cm^{-2}$
- Low oxygen diffusivity
- Crystallization temperature >1000°C

Basic Characteristics of Binary Oxide Dielectrics

Dielectrics	SiO_2	Al_2O_3	Y_2O_3	HfO_2	Ta_2O_5	ZrO_2	La_2O_3	TiO_2
Dielectric constant	3.9	9.0	18	20	25	27	30	80
Band gap (eV) Band offset (eV)	9.0 3.2	8.8 2.5	5.5 2.3	5.7 1.5	4.5 1.0	7.8 1.4	4.3 2.3	3.0 1.2
Free energy of formation $MO_x+Si_2 \rightarrow M+ SiO_2$ @727C, Kcal/mole of MO_x	-	63.4	116.8	47.6	-52.5	42.3	98.5	7.5
Stability of amorphous phase	High	High	High	Low	Low	Low	High	High
Silicide formation ?	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hydroxide formation ?	-	Some	Yes	Some	Some	Some	Yes	Some
Oxygen diffusivity @950C (cm^2/sec)	$2x\ 10^{-14}$	$5x\ 10^{-25}$	?	?	?	10^{-12}	?	10^{-13}



Critical Integration Issues

- Morphology dependence of leakage
  Amorphous vs crystalline films?
- Interfacial structures
- Thermal stability
- Gate electrode compatibility
- Reliability

Fundamental Limitations

- Fixed charge
- Dopant depletion in poly-Si gate
- Dopant diffusion
- Increasing field in the channel region

The Discovery of novel oxides of $(Ga, Gd)O_x$ and Gd_2O_3 for GaAs Passivation

GATE DIELECTRICS FOR III-V SEMICONDUCTORS

❖ **Why GaAs ?**

Higher electron mobility and semi-insulating substrate
For high speed signal processing, and high power applications

HOW TO PASSIVATE GaAs SURFACE ?

❖ **Previous efforts over thirty five years !**

- Anodic, thermal, and plasma oxidation of GaAs
- Wet or dry GaAs surface cleaning followed by deposition of various dielectric materials

THE KEY is to identify a dielectric being thermodynamically and electronically stable, and showing a low D_{it} with GaAs.

❖ **Our breakthrough**

- Novel gate oxides **$Ga_2O_3(Gd_2O_3)$ and Gd_2O_3** in-situ deposited by MBE of low D_{it}
- Have successfully applied to GaAs, AlGaAs, InGaAs, InP, GaN, and Si

ULTRAHIGH VACUUM DEPOSITION OF OXIDES

Initial thinking: to attain pure Ga_2O_3 film for passivation

High-purity single crystal $Ga_5Gd_3O_{12}$ (GGG) source

Evaporation (sublime) by e-beam

Gd_2O_3 ionic oxide
T_m > 4000K

Ga_2O_3 more covalent oxide
T_m ~ 2000K

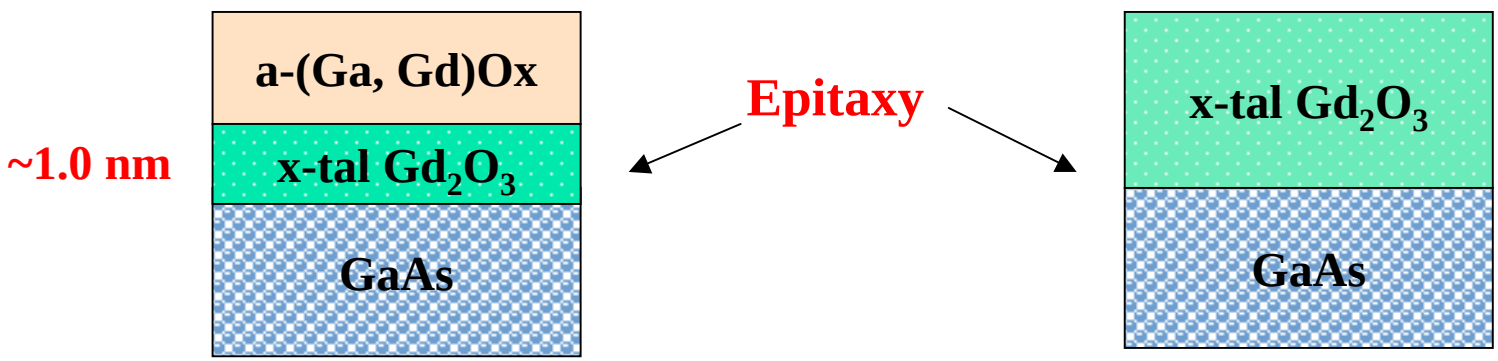
Ga_2O_3 evaporated mostly, and formed amorphous Ga_2O_3 film

Mixed Oxide (Ga, Gd)O_x

Gd/(Ga+Gd) > 20%
Gd^{+3} stabilize Ga^{+3}

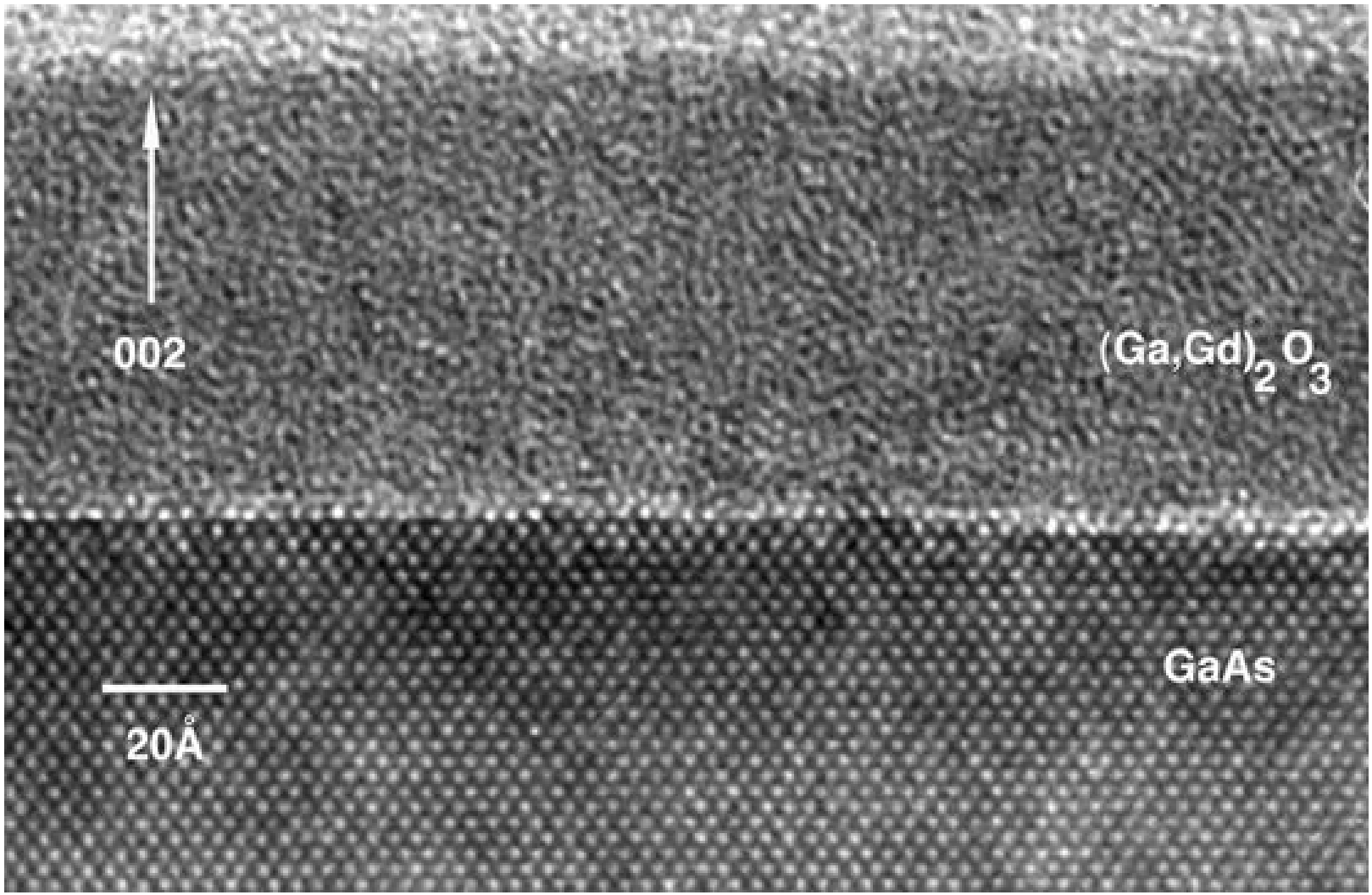
Pure Gd_2O_3 Film

Single domain, epitaxial film
in (110) Mn_2O_3 structure



J. Kwo et al, APL, **75**, 116, (1999)

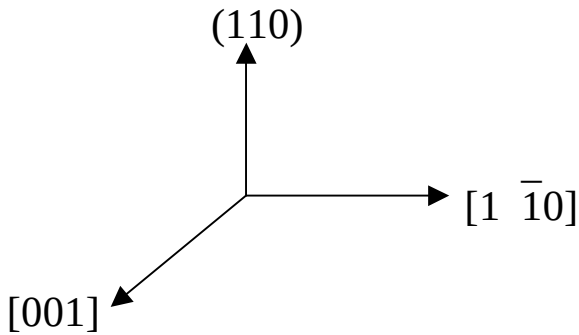
Cross sectional TEM of $(Ga, Gd)_2O_3$ on GaAs



Single Domain Growth of (110) Gd_2O_3 Films on (100) GaAs

Mn_2O_3 Structure

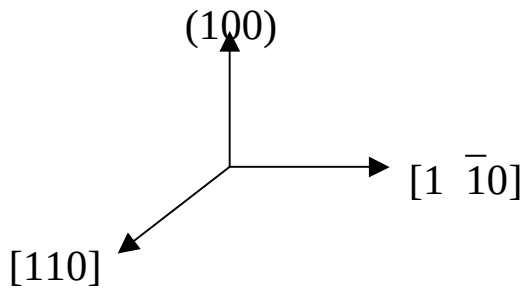
Gd_2O_3 a= 10.81Å

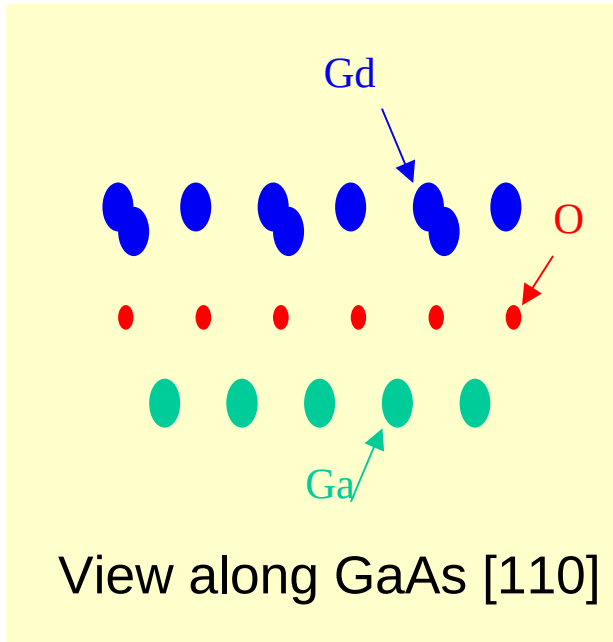


3: 4 match

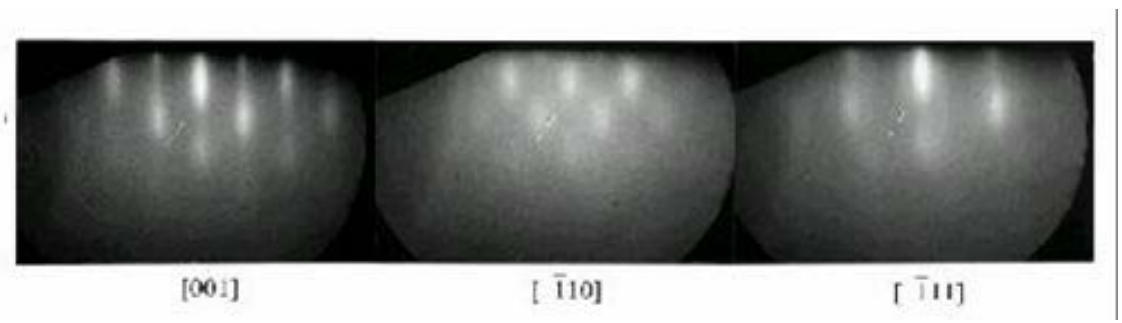
1: 2 match

GaAs a=5.65Å



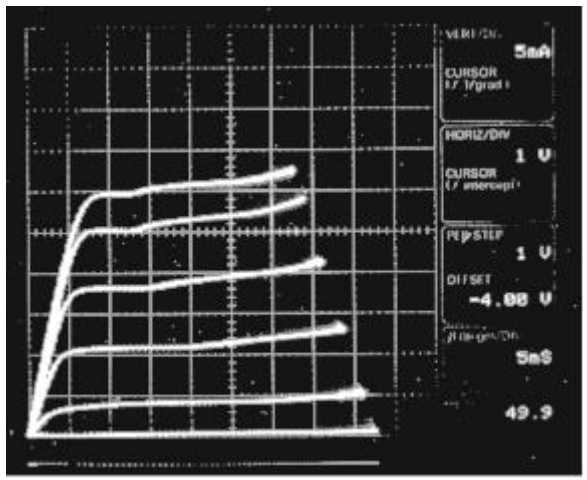


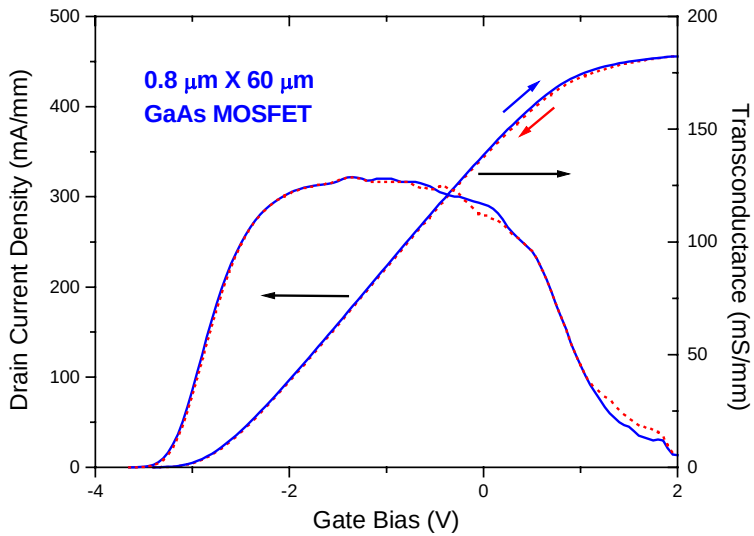
Gd_2O_3
(110)
25Å



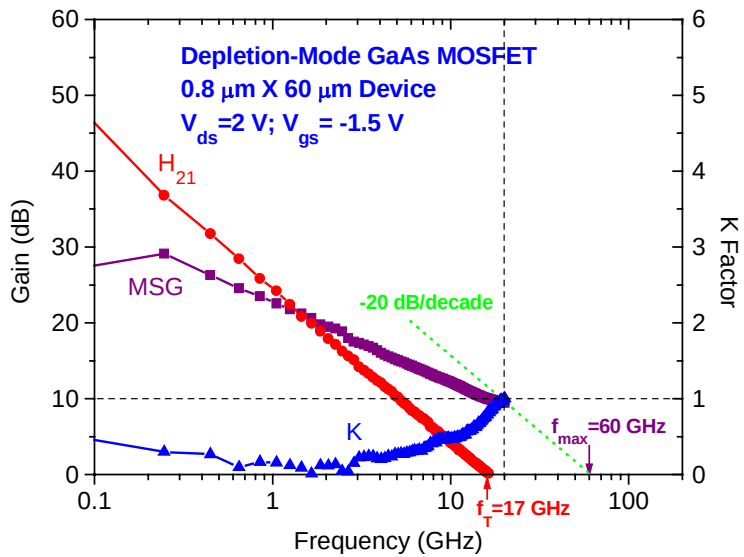
0.8 μm D-Mode GaAs MOSFET

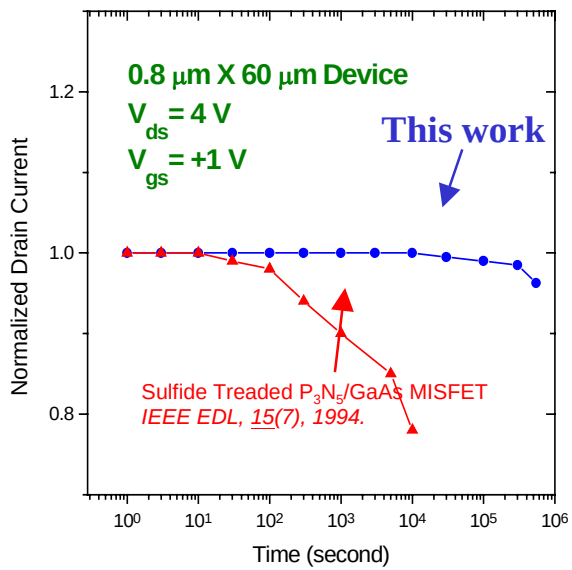
Vertical: 5mA/div
Horizontal: 1V/div
V_g=+1V
Step= -1V





- **Mobility μ_n = 1100 (cm^2/V sec)**





Summary of results and achievements

High κ gate dielectrics of Gd_2O_3 and Y_2O_3 on Si

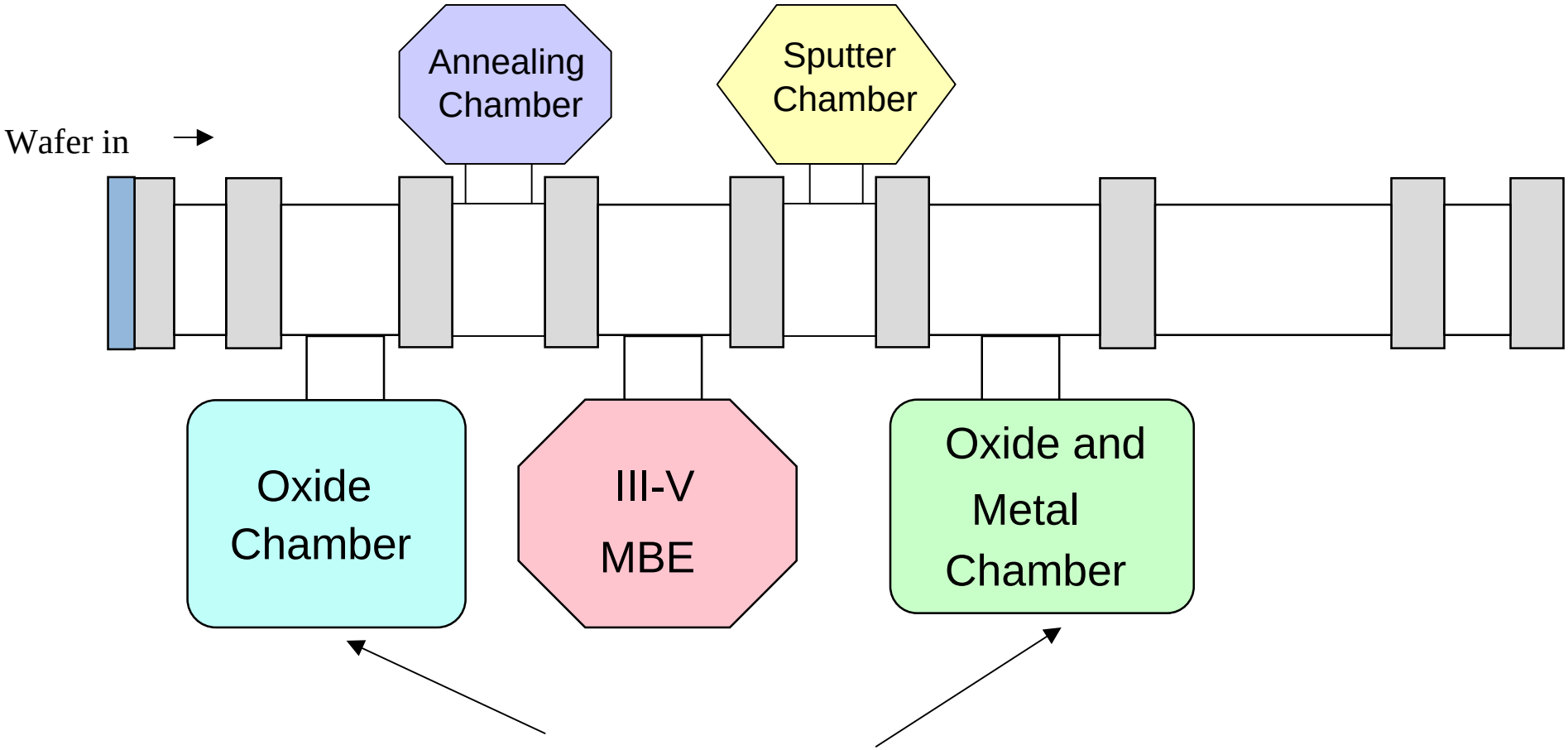
Gd_2O_3 **κ = 14**

Y_2O_3 **κ = 18**

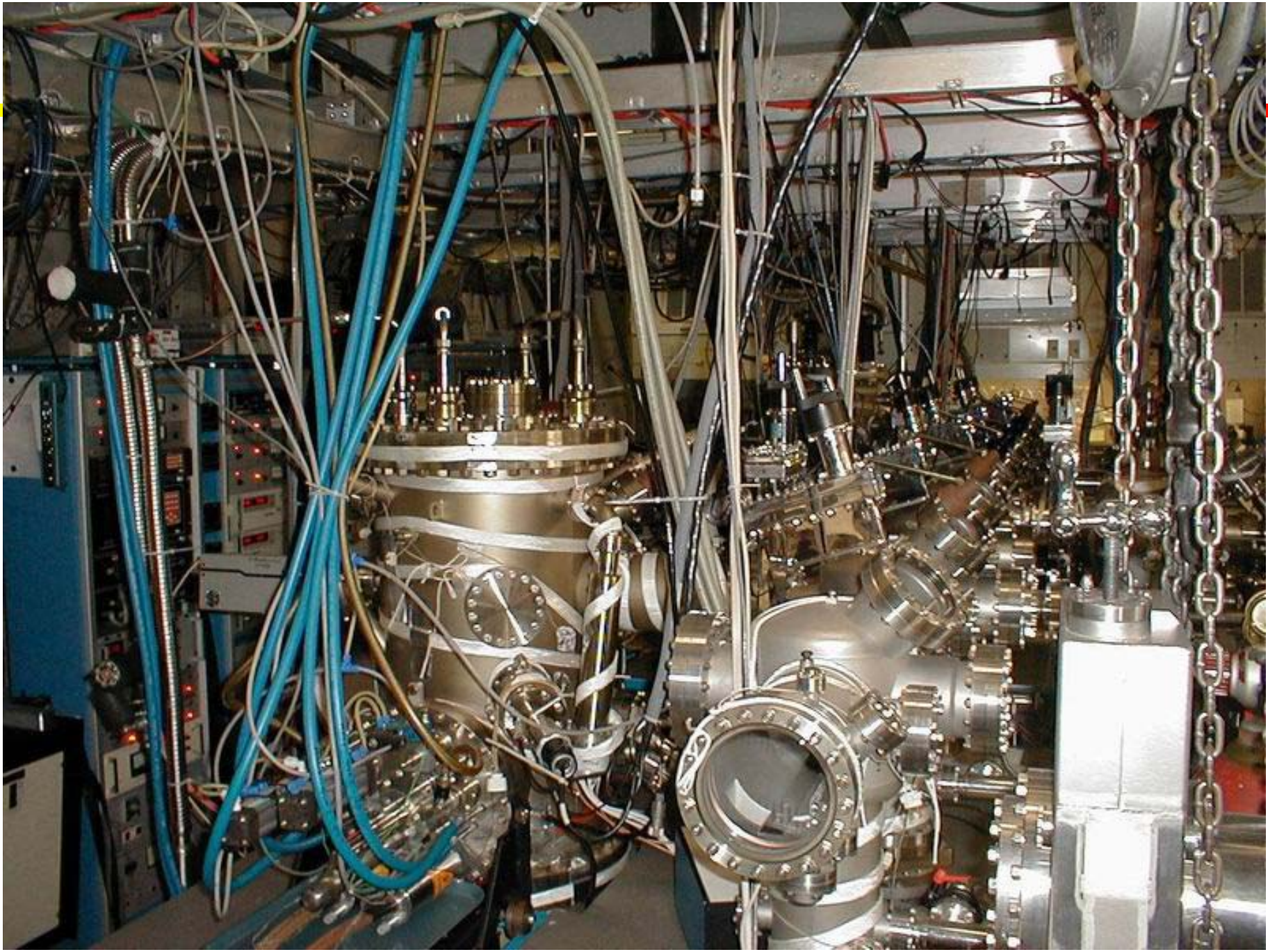
In both epitaxial and amorphous films

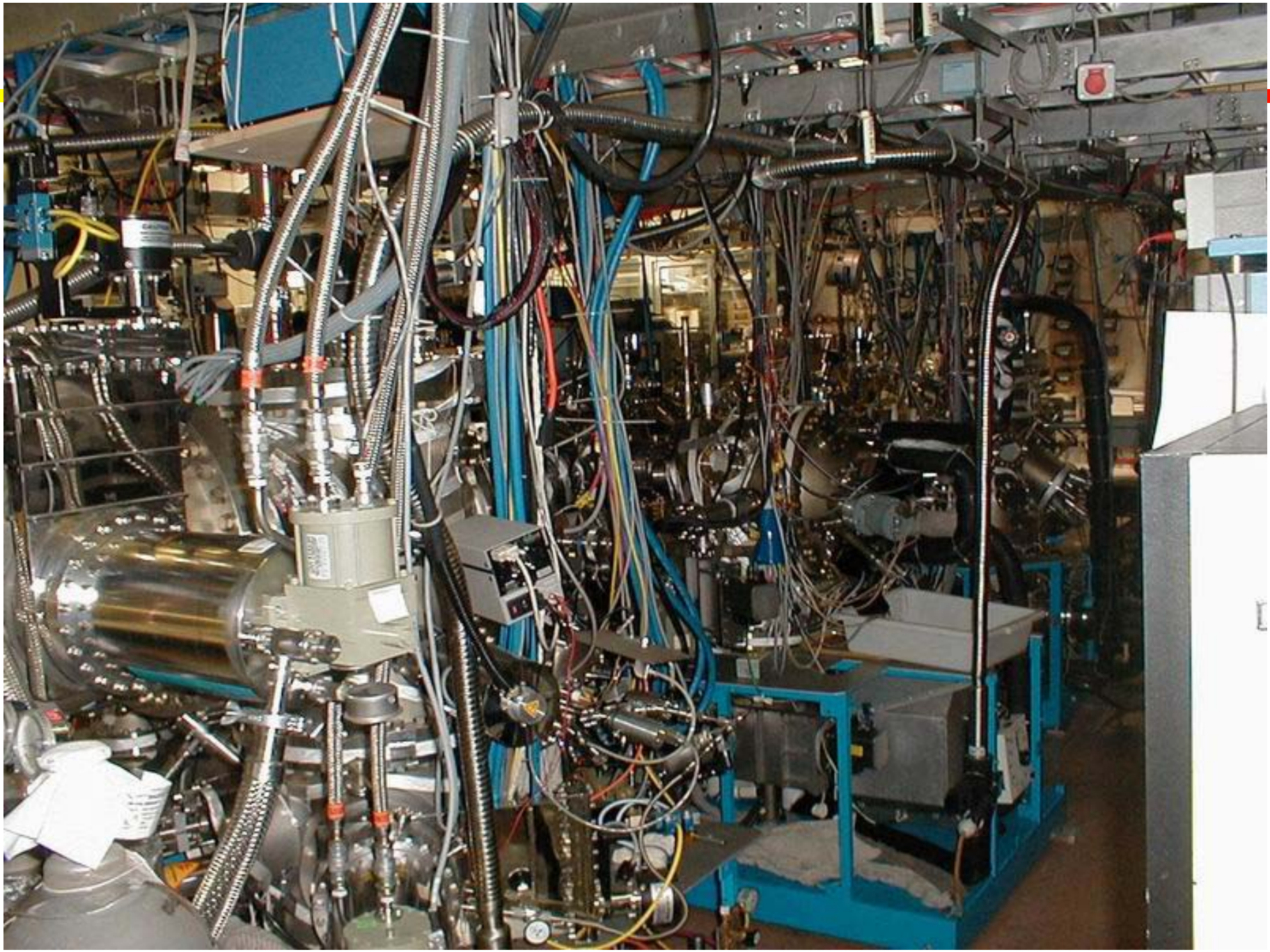
J. Kwo, et al APL, **77**, 130, (2000)
J. Kwo, et al J. Appl. Phys. **89**, 3920 (2001)

In-situ Fabrication: UHV Integrated Processing System



Equipped with electron beam evaporators and effusion cells

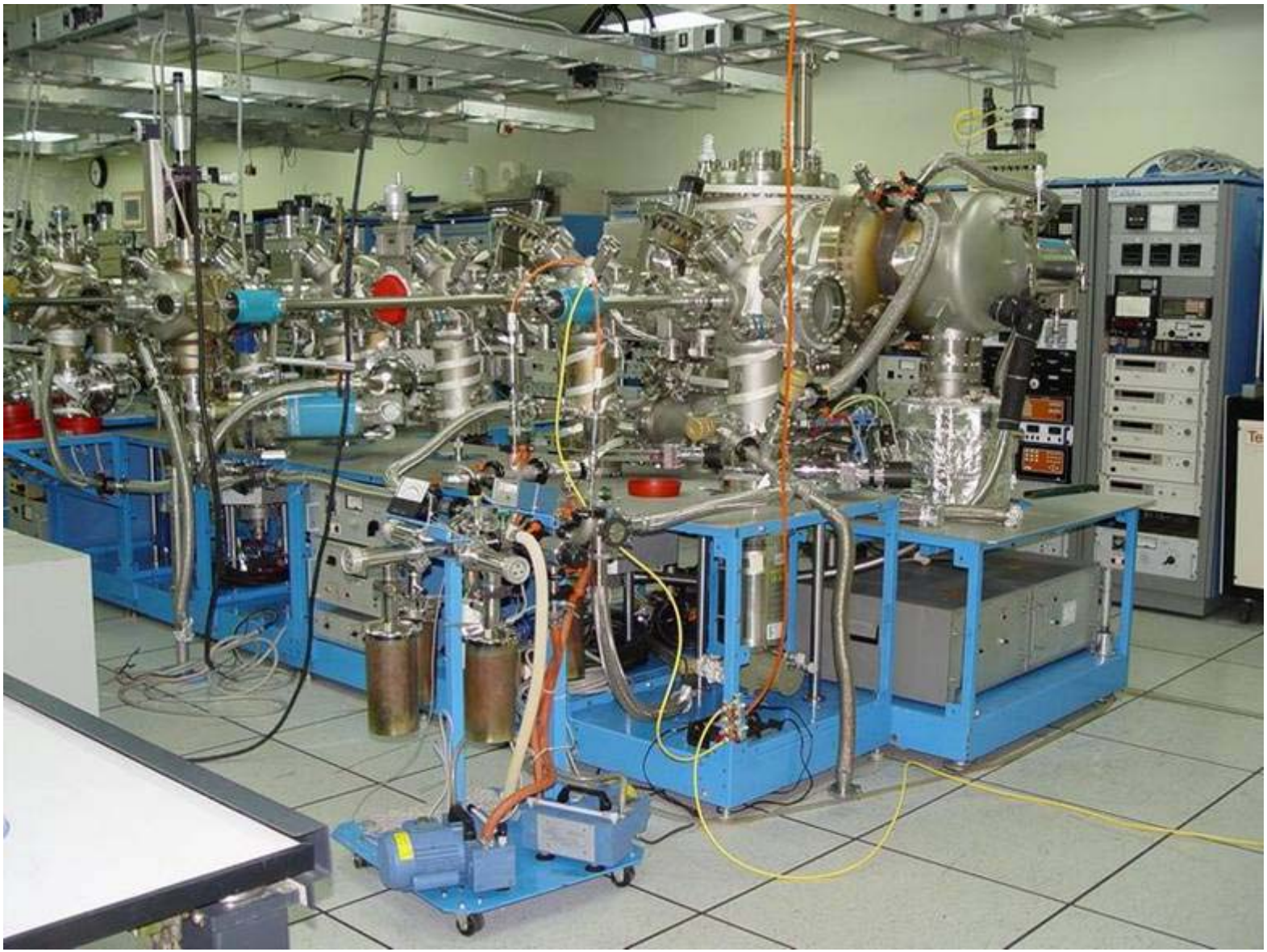




Part of the equipment-left

Part of the equipment-middle

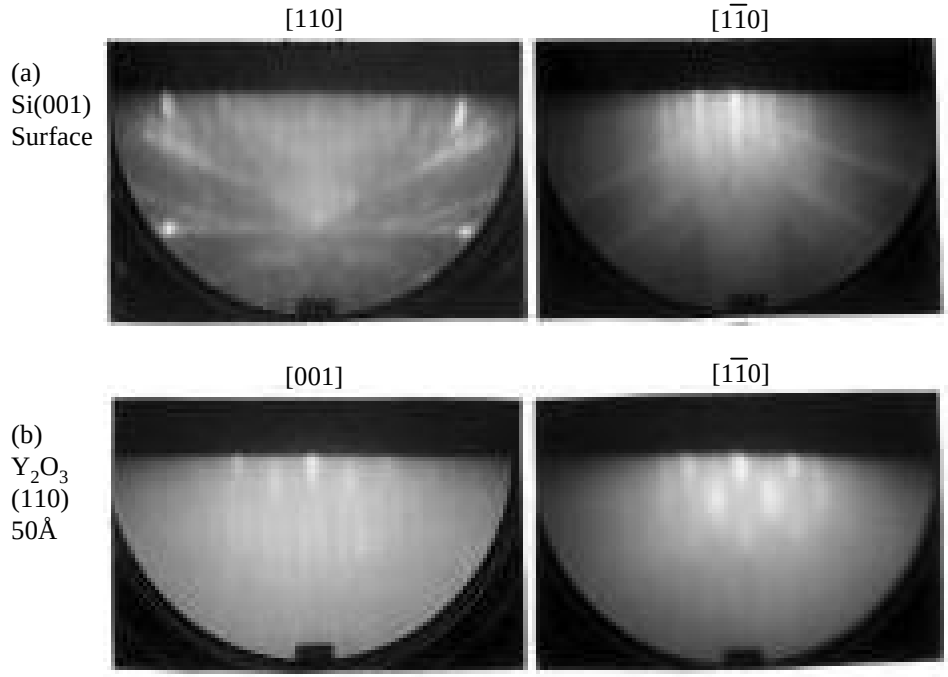
Part of the equipment-right

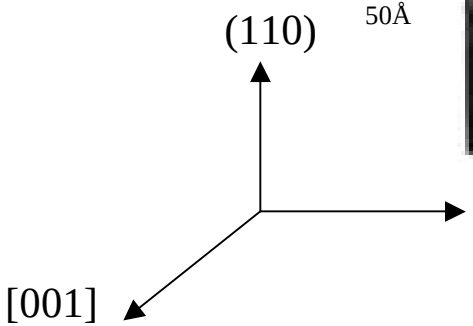


UHV Deposition of the Oxides on Si

- Ultrahigh vacuum, multi-chamber MBE system.
- Electron-beam evaporation of oxide sources from pressed ceramic pellets.
- 2 inch RCA-cleaned Si wafers, hydrogen passivated, followed by prompt insertion into UHV.
- In-situ heating to 400-500C to attain a (2 x 1) reconstructed Si surface.
- Substrate temperature of 550C for **epitaxial** films.
- Room temperature deposition for **amorphous** films.
- Maintain **low pressure** during growth $< 1.0 \times 10^{-9}$ torr.

Single Domain Growth of (110) Gd_2O_3 Films on Vicinal (100) Si

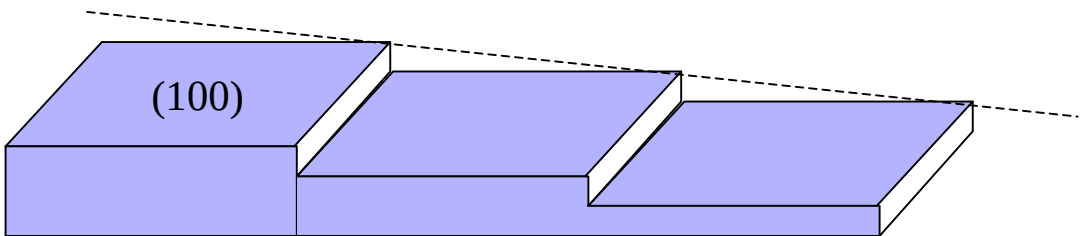


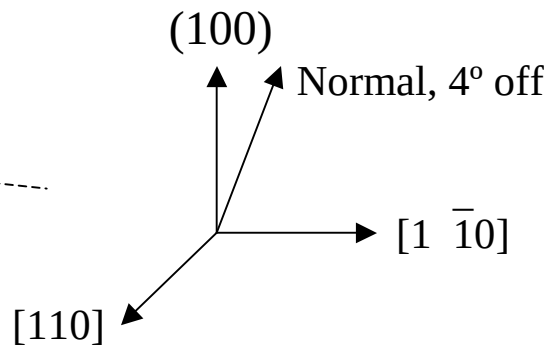


Gd_2O_3 a= 10.81 Å

Y_2O_3 a= 10.60 Å

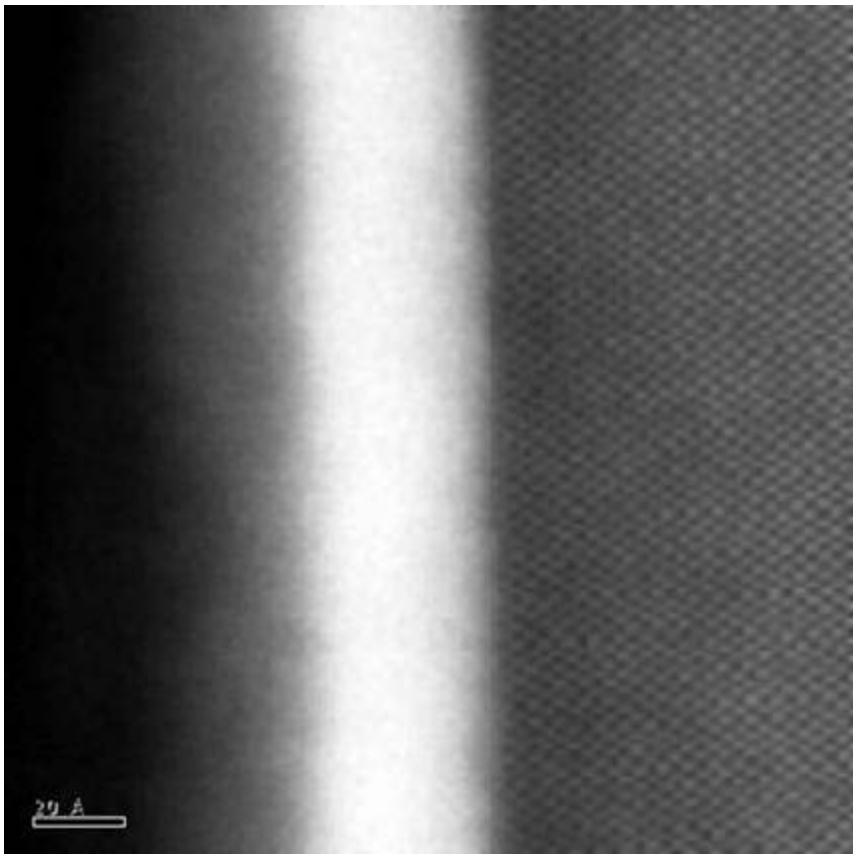
Si a=5.43 Å



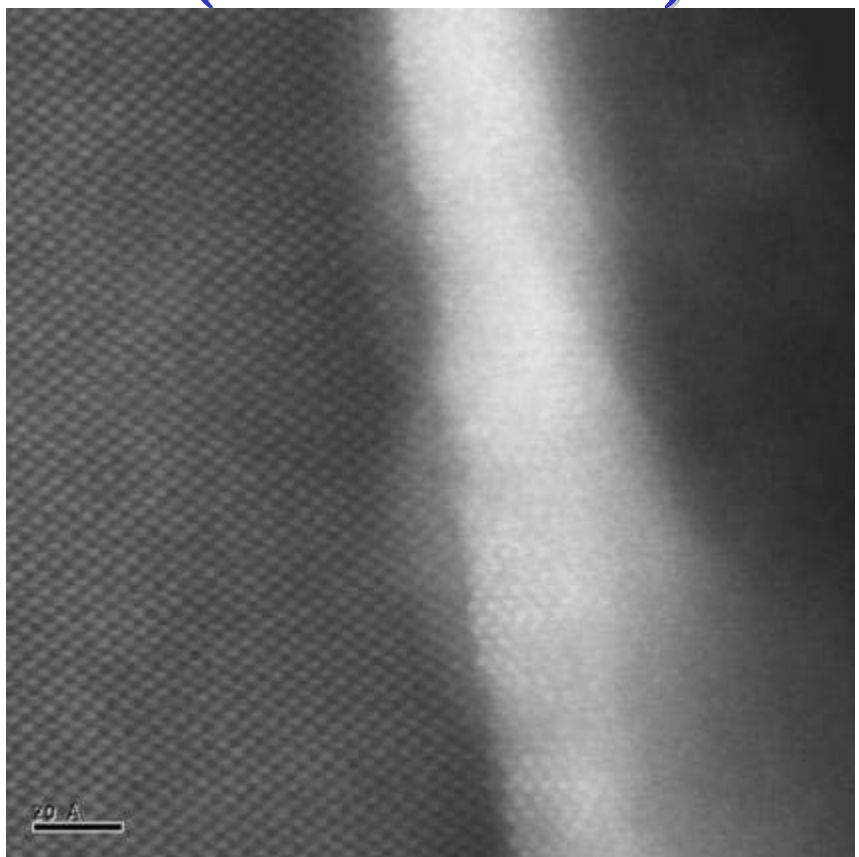


ADF-STEM Image

Amorphous Gd_2O_3 on Si



Crystalline Gd_2O_3 on Si (two domain film)

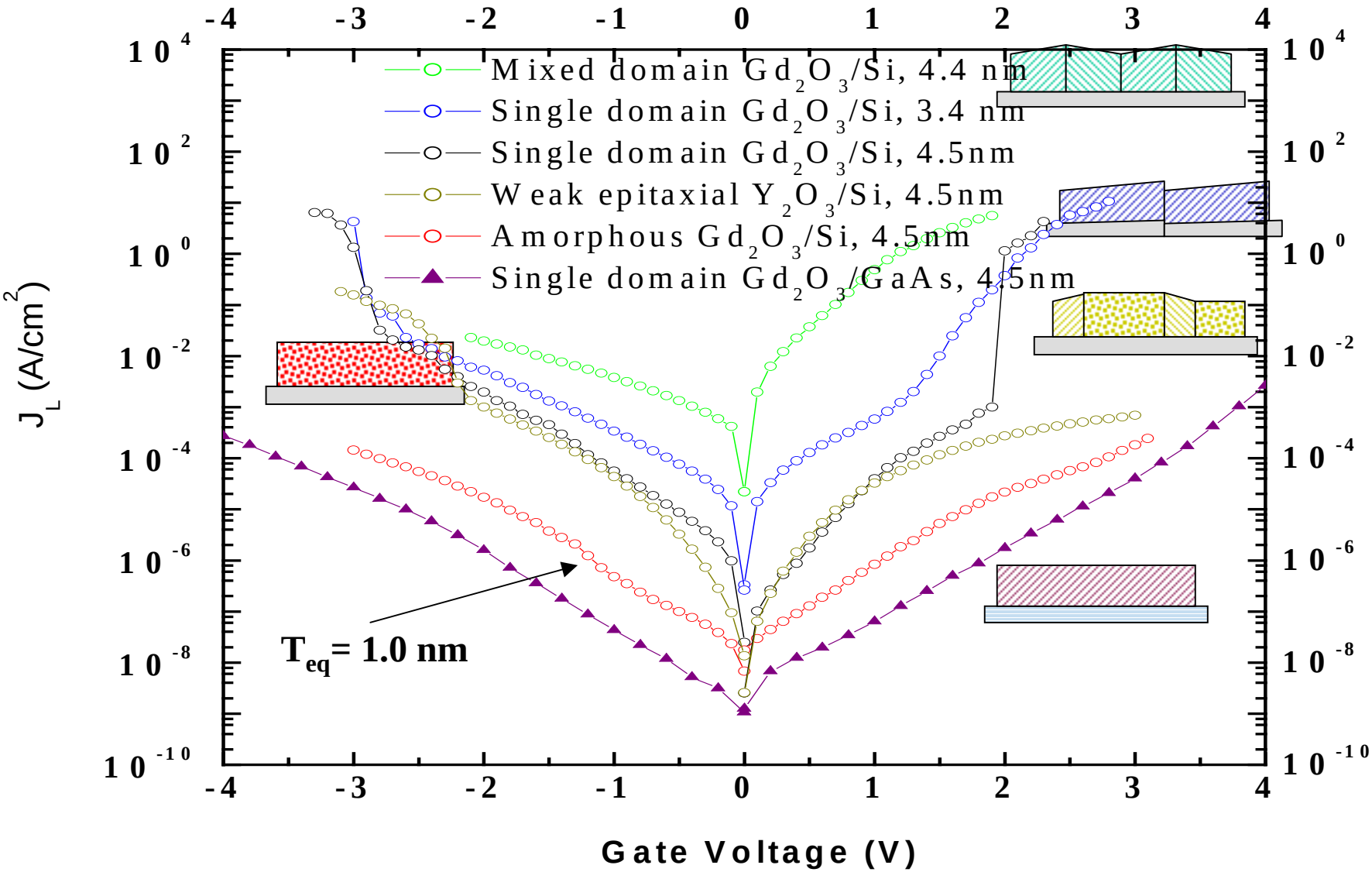


No Evidence of SiO_2 Formed at the Interface

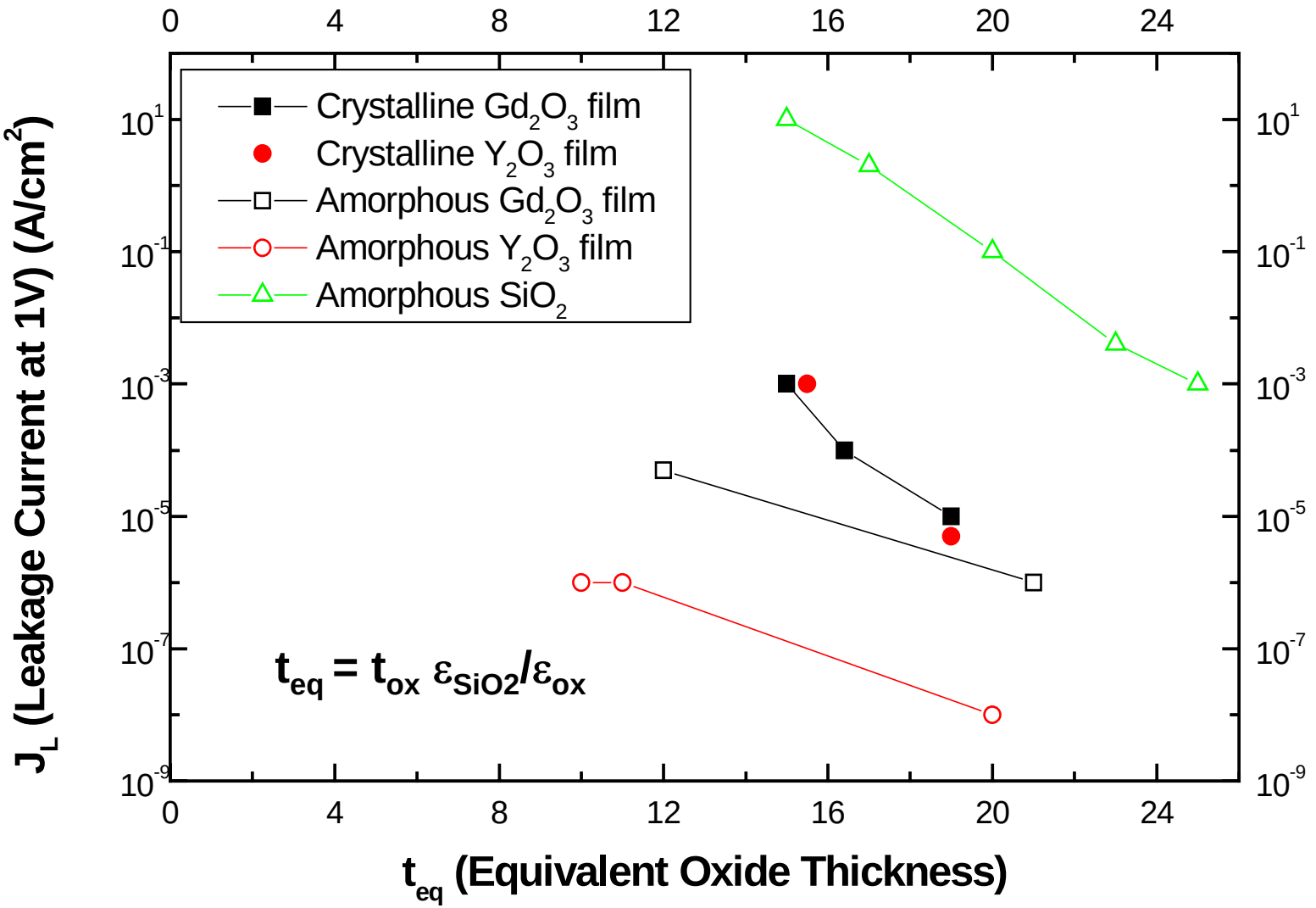
Critical Materials Integration Issues

- **Morphology, amorphous vs crystalline films?**
- Interfacial structures
- Thermal stability
- Gate electrode compatibility

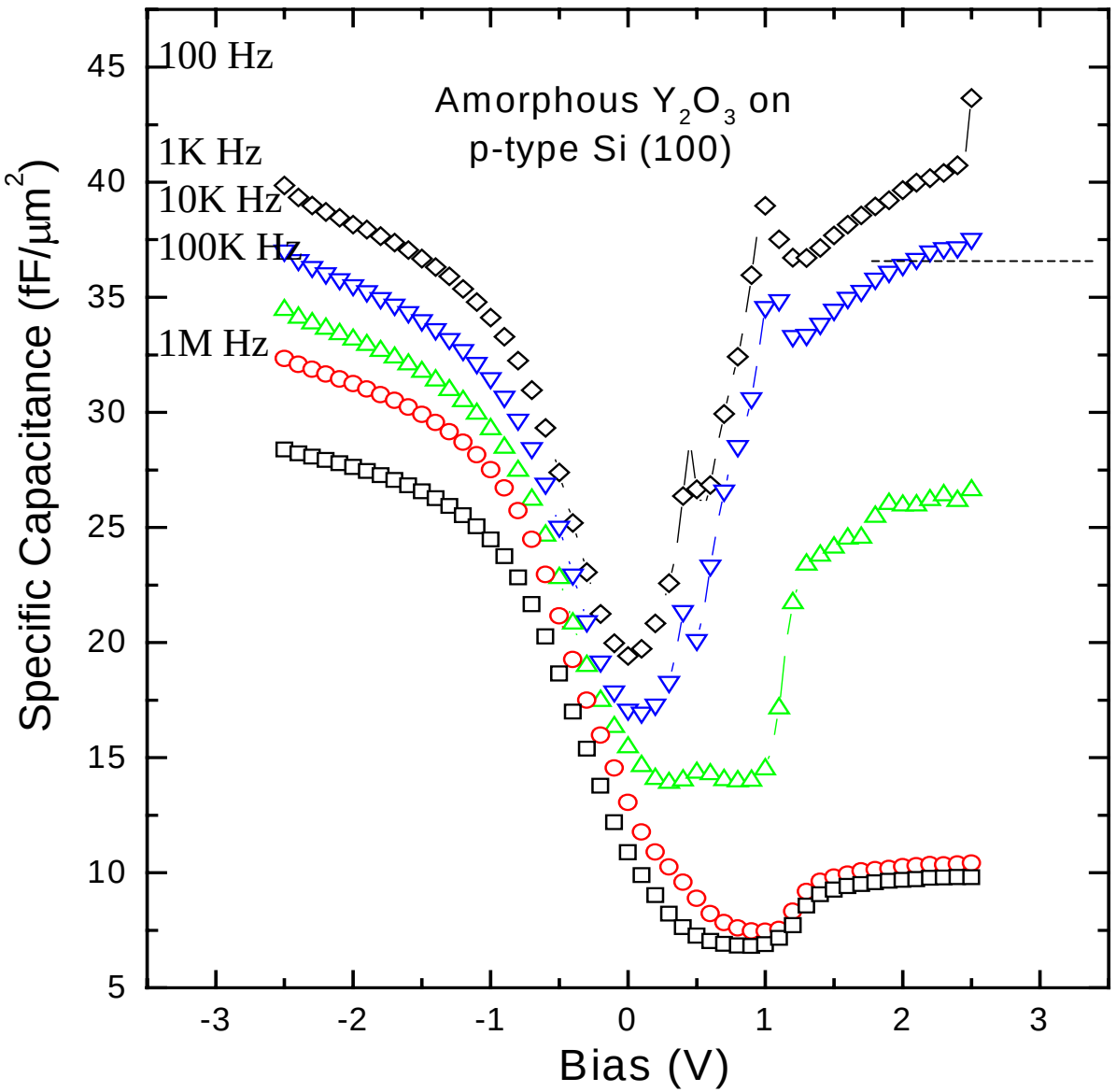
Morphology Dependence of Gd_2O_3 and Y_2O_3



Comparison of Leakage Current vs Oxide Thickness



C-V Electrical Characteristics of Y_2O_3 on Si



1.0 nm SiO_2 equivalent

Terman Method
D_{it} ~10^{12}cm^{-2}eV^{-1} as upper limit

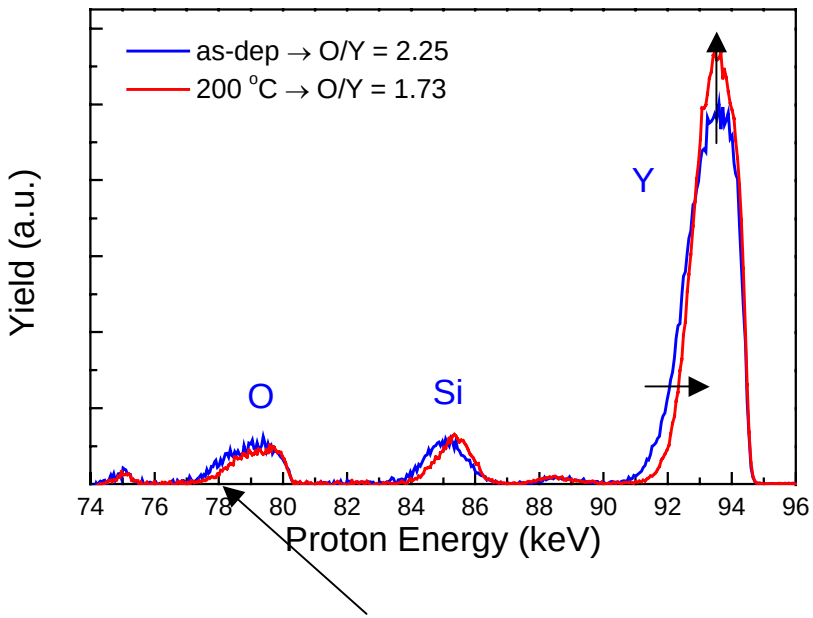
D_{it} ~10^{11}cm^{-2}eV^{-1}

Critical Materials Integration Issues

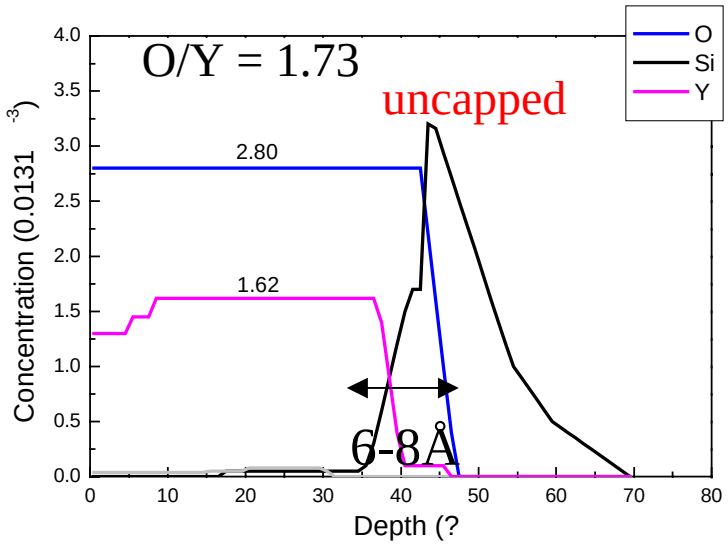
- Morphology, amorphous vs crystalline films?
- **Interfacial structures**
- Thermal stability
- Gate electrode compatibility

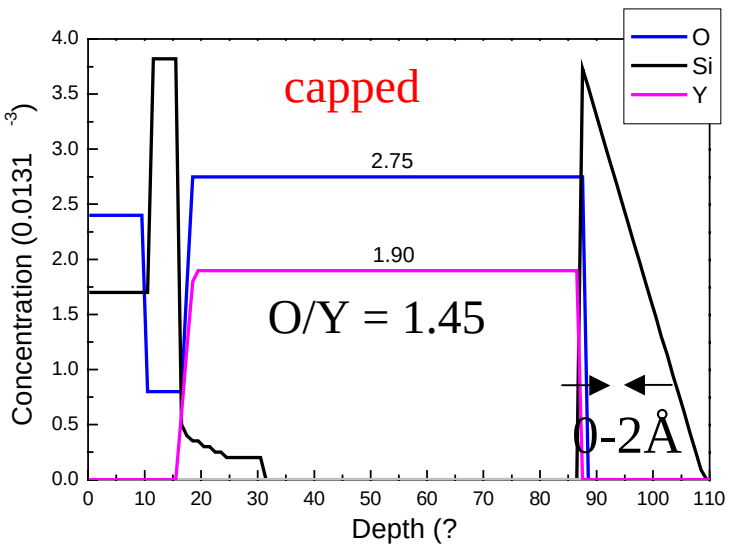
Medium Energy Ion Scattering

With Rutgers University
Using 100 keV proton beam

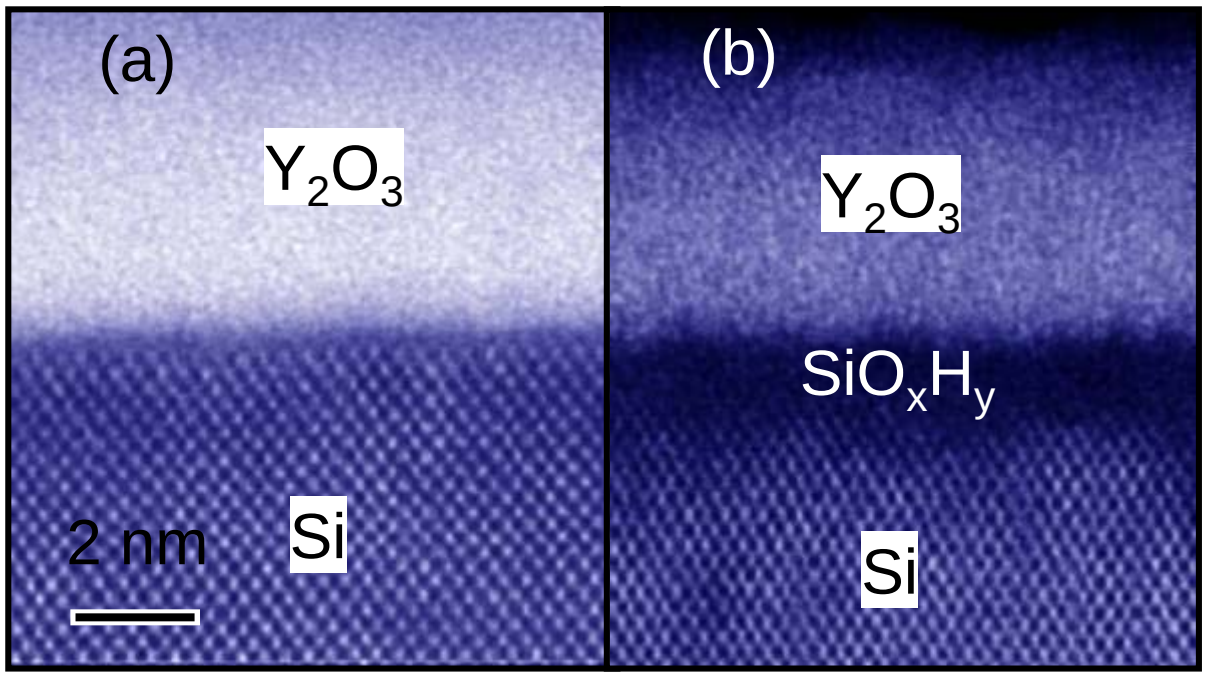


Clear loss of O: film becomes denser, O/Y decreases, but remains > 1.5





STEM Cross Sectional Images



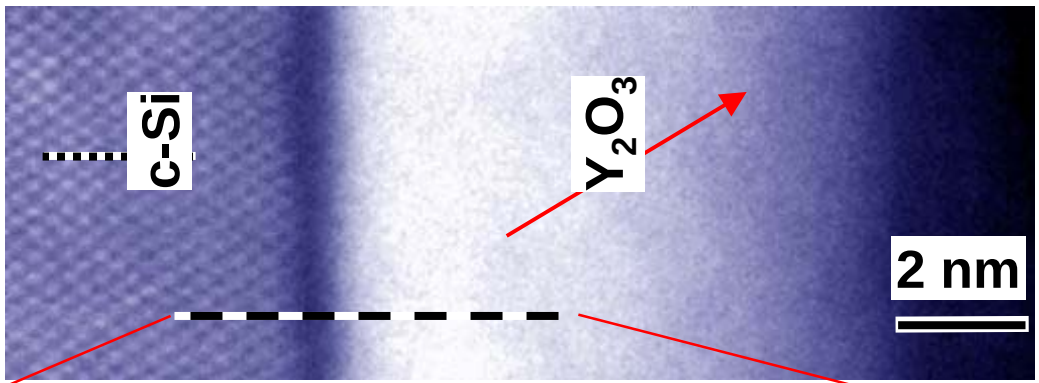
(Thick cross section) (Thin cross section)

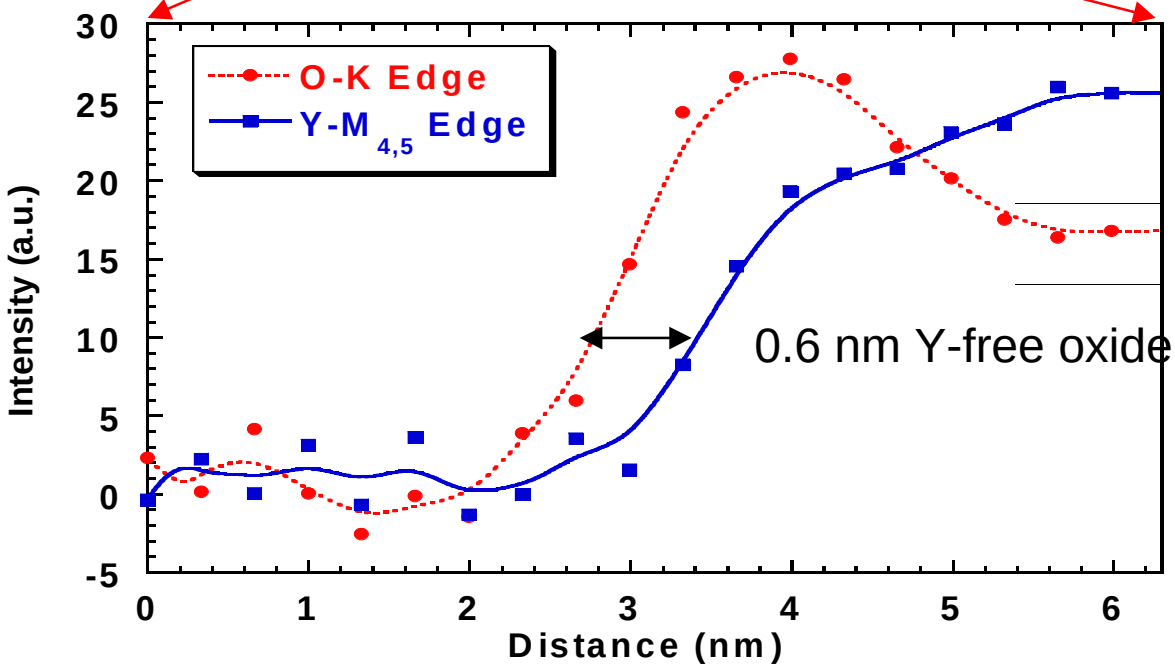
Amorphous Si/Y_2O_3/Crystalline-Si

D. Muller

Yttrium Oxide on Silicon

(capped in-situ with Si, no anneal)





May be caused by TEM specimen thinning process

Between the Y_2O_3 and C-Si is a graded Si_xY_yO layer

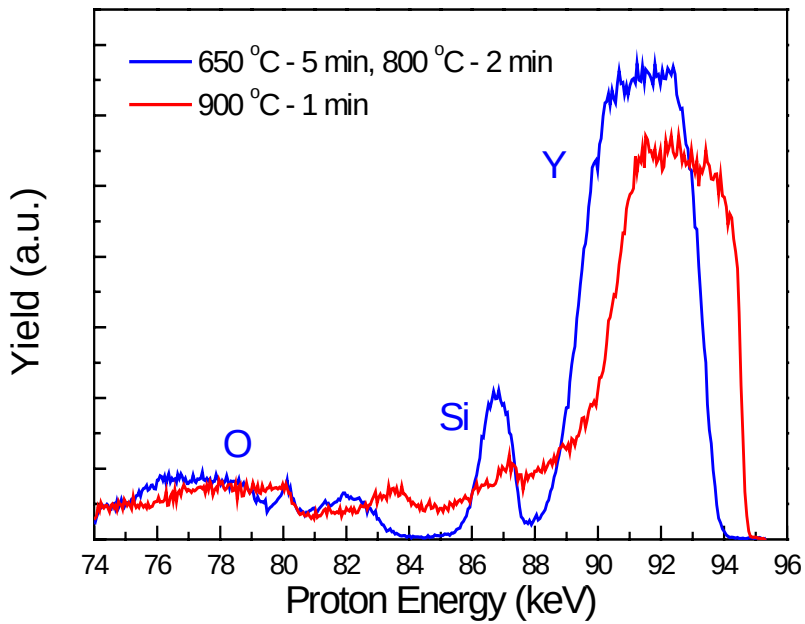
D. Muller

Critical Materials Integration Issues

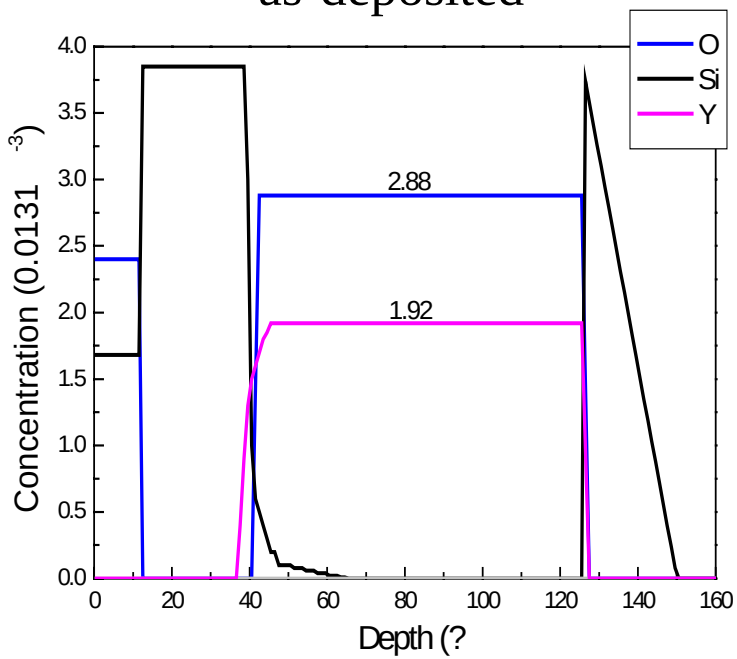
- Morphology, amorphous vs crystalline films?
- Interfacial structures
- **Thermal stability**
- Gate electrode compatibility

Thermal Stability

Thick capping layer case: a-Si(40Å)/Y_2O_3(90Å)/Si interface is stable at 800°C, reaction has occurred at 900°C.



as-deposited



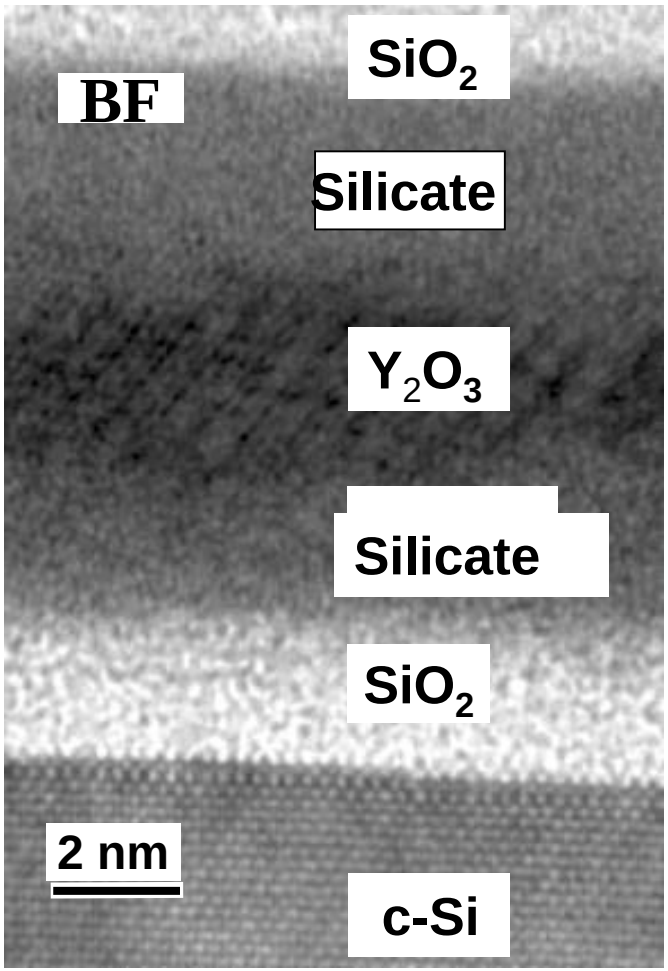
Not much change here from as-dep to 650°C to 800°C.

Critical Materials Integration Issues

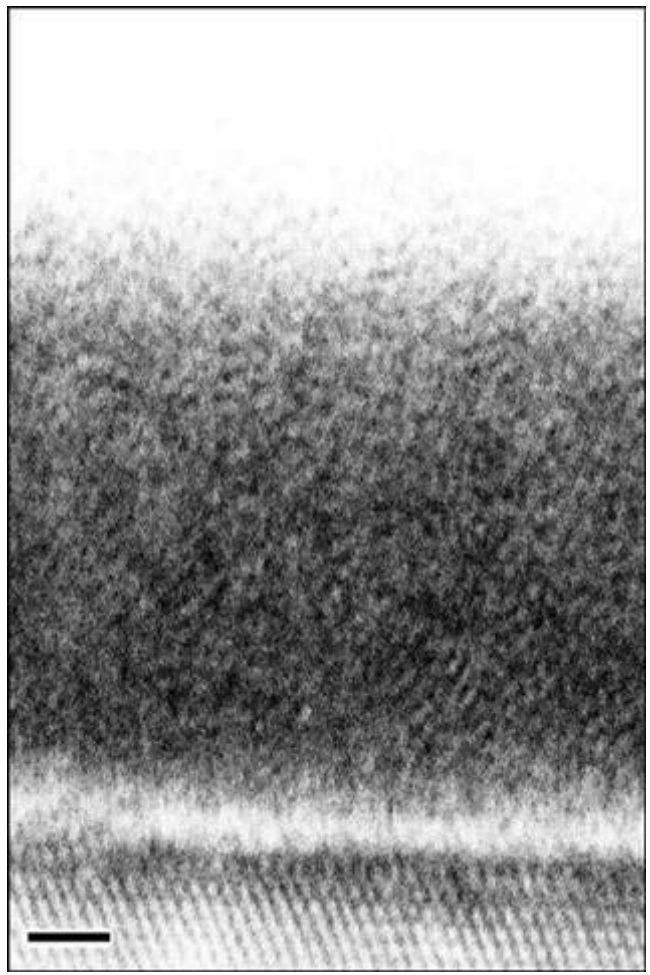
- Morphology, amorphous vs crystalline films?
- Interfacial structures
- Thermal stability
- **Gate electrode compatibility**

Compatibility of Gate Electrode

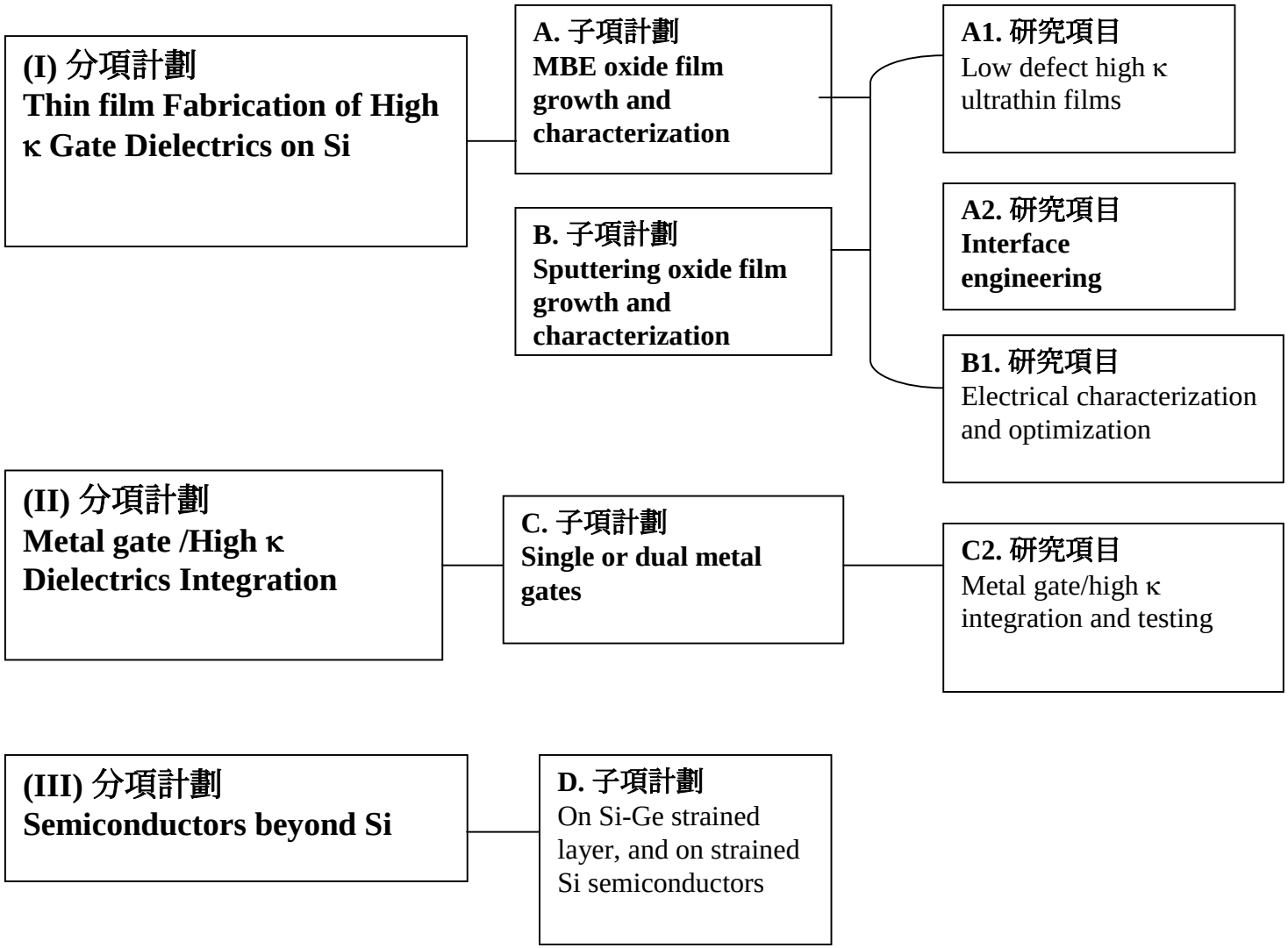
Annealed at 850C/15 min in O_2



Annealed in 850C/15 min in N_2



High K Gate Dielectrics Project



New Research Programs

- Low defect high κ ultrathin films
- Interface engineering
- Electrical characterization and optimization

- Identify new material candidates for metal gate
- Metal gate/high κ integration and testing

- Integration of high κ, and metal gate with Si- Ge strained layer and testing
- Integration of high κ, and metal gate with strained Si and testing

Low Defect High κ Ultrathin Films

New dielectric films by sputtering and MBE

-- HfO_2 and ZrO_2 systems doped with N, Al, and Si

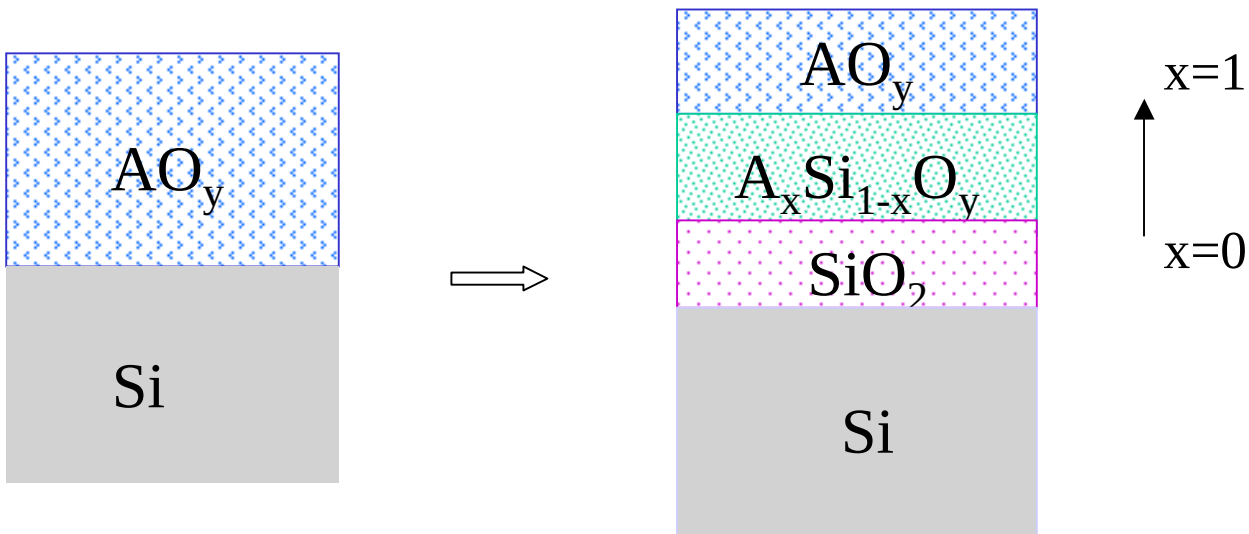
* To reduce charge trapping, and the fixed charge density.
* To raise the recrystallization temperature

-- Ternary oxides of rare earth aluminate on Si such as $(Al, Y)_2O_3$

* To exceed the figure of merit over Al_2O_3

Interface Engineering

Graded composition growth scheme to engineer the interface with Si



Electrical characterization and optimization

Three major problems :

- **Large trapped charge**
- **Low channel mobility**
- **Electrical stability and reliability**

Our approaches :

- **In-situ doped polysilicon gate or metal gate to avoid the hydroxide formation (frequency dispersion).**
- **Nitrogen doping and post anneals to reduce the fixed charge density.**
- **To correlate interfacial state density with the materials parameters and the device mobility.**

Metal Gate Electrode

- Compatible work function,
- High carrier concentration,
- Thermal/chemical stability with the underlying dielectric.

--- To replace the *n*+, and *p*+ poly, it is necessary to identify pairs of metals with work functions that are respectively within 0.2 eV of the conduction and valence band edges of Si.

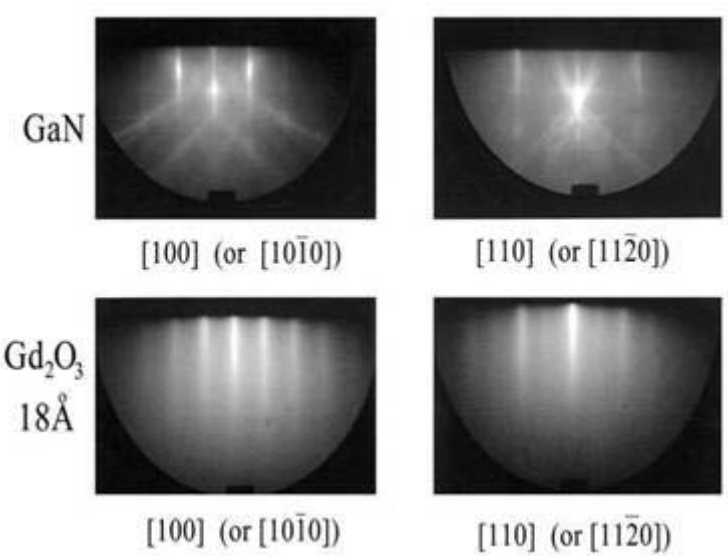
Solutions:

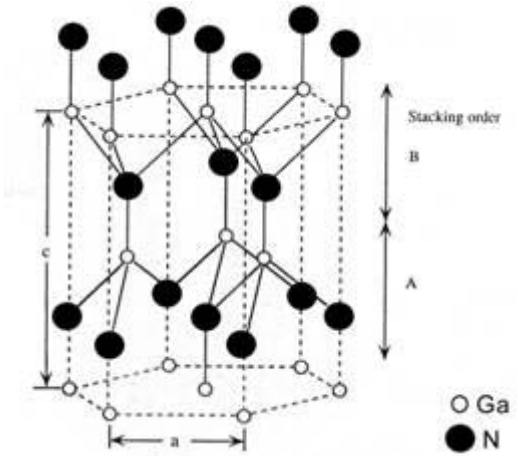
(1) To introduce N and /or Si in the low work function metal. Metal alloys TaN, and TaNSi are potential NMOS gate electrodes.

(2) To obtain low-work function films by the alloying of elemental metals with compositional control such as binary alloys of Ta-Ru

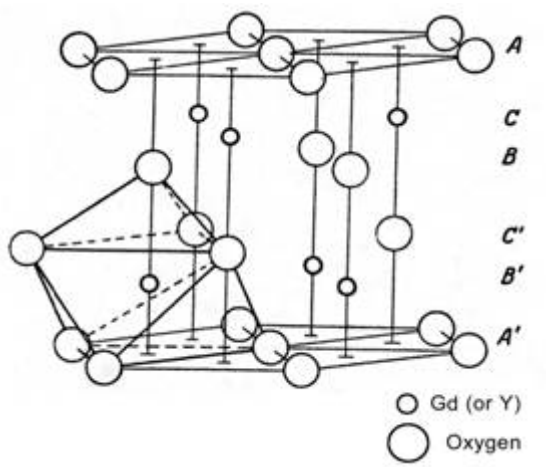
(3) Conducting metal oxides like IrO_2 and RuO_2 as PMOS gate electrode.

Gd_2O_3 on GaN





wurtzite GaN
hcp phase
a = 3.189 Å
c = 5.185 Å



hcp rare earth
sesquioxide
a = 3.86 Å
c = 6.16 Å

A strong tendency to conform to the substrate

Low D_{it} of ~ 10^{11} $cm^{-2}eV^{-1}$

Summary

- Surface passivation using stable low D_{it} oxides $Ga_2O_3(Gd_2O_3)$ and Gd_2O_3 for GaAs and GaN
- Strong tendency to conform to underlying substrates

  insight for low D_{it} and passivation !

- Crystalline and amorphous Gd_2O_3 and Y_2O_3 as alternative gate dielectrics for Si with sharp interfaces without reactions.
- Model systems to investigate critical materials integration issues of the high κ gate dielectric for Si CMOS processing.

- Better understandings of the leakage conduction, fixed charges, mobile ions, and interfacial structures are needed to establish the reliability of the oxides.

Anticipated Accomplishments

RESEARCH

- Understand the interfacial structures and the atomic bonding of the MBE and ALD oxides on Si to establish the mechanism of a low D_{it} on Si, and Si-Ge.
- Identify the charge carriers and underlying transport mechanism of the newly developed dielectric materials.
- Study and understand the physics, such as interfacial scattering and mobilities in the inversion channel and device performance on the MOS devices.

Anticipated Accomplishments (Conti)

TECHNOLOGY

- Achieve significant reduction in D_{it}, electrical leakage, and fixed charge density in MBE and ALD oxides on Si after systematic anneal studies
- Establish the ALD growth/process parameters for high-performance oxide
- Establish process flow and masks for fabricating the sub-micron and nano- MOS and MOSFET devices using high κ dielectrics on Si and Si-Ge
- Develop IP's for the new materials, growth methods, devices, and technology, thus establish our position in these new technologies