April 18 2007 前沿物理演講 Department of Physics / NTHU

Nano-devices at the scaling limit

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Technology Roadmap – Introduction

- Fundamental limits to scaling
- Future nano-devices
 - Single electron transistor



Introduction: Technological and biological length scales



Why scale down?





Electromechanical relay

Vacuum tube

Solid state transistor

Why Physicist?

Nobel Prize in Physics

"for their researches on semiconductors and their discovery of the transistor effect"



1956



William Bradford Shockley



John Bardeen



Walter Houser Brattain

Solid state transistor



 "for developing semiconductor
 heterostructures used in high-speed and optoelectronics"



Zhores I Alferov



Herbert Kroemer

"for his part in the invention of the integrated circuit"



Jack S Kilby

IC



What's the problem? Current status.



Gate leakage
 SD leakage
 Device-device variability

Power dissipation limits device density

 CMOS will operate near ultimate limits



nm

- A physical system as a computing medium:
- 1. Distinguish ability
- 2. Conditional change of the state



- D: Distinguishability
- P: probability of spontaneous transition
- e.g. D=Max, P=0 D=0, P=0.5

$$P_{Classical} = \exp(-\frac{E_b}{k_B T})$$

Suppose the minimum distinguishable barrier:

$$\frac{1}{2} = \exp(-\frac{E_b}{k_B T})$$
$$\implies E_b = k_B T \ln 2$$

Minimum energy dissipation per logic transition

See Zhirnov, Cavin, Hutchby, and Bourlanoff. Prof. IEEE, special issue on nanoelectronics and nanoscale processing. Nov. 2003

Least energy computer

 $\begin{aligned} E_b &= k_B T \ln 2 \\ \Delta x \Delta p \geq \hbar \\ \Delta E \Delta t \geq \hbar \end{aligned}$

Heisenberg – uncertainty principle

- Min switch time

Min device size

- Max gate density

$$t_{\min} = \frac{\hbar}{E_b} = \frac{\hbar}{2k_B T \ln 2} = 1.2 \times 10^{-13} s$$
$$x_{\min} = \frac{\hbar}{\sqrt{2mE_b}} = 1.5nm \quad \text{T=300K}$$
$$n = \frac{1}{x_{\min}^2} = 4.6 \times 10^{13} \frac{gate}{cm^2}$$

Total power consumption







FET (Field Effect Transistor) \Rightarrow Materials RSFQ (Rapid single flux quantum device)



 $-\mathbb{X}$



RTD (Resonance tunneling diode)





Spin transistor

SET (Single electron transistor)

Quantum coherent devices





Top-down / Bottom-up approach



Single Electron Transistor – single quantum dot –artificial atom



• Capacitive Charging Model



 \Rightarrow Coulomb blockade



AI - Single Electron Transistor



Double quantum dot – artificial molecular





Coupling strength $J=4t_c^2/U_i$ U_i: intradot charging energy Γ : Lead-dot coupling





Advantage:

J and Γ can be tuned by the external gate voltages. On-site Coulomb interaction can be externally adjustable

Coupled Double Quantum Dots





Ref. W.G. van der Wiel Rev. Modern Physics Vol 75, p.1 (2003)

Double quantum dot –Coulomb Blockade Spectrum





EF.

80

Jun Kondo 1964 s-electron

Quantum dot used to simulate Kondo effect

N=odd \Rightarrow unpaired electron Local magnetic moment











Hybrid QD+AI-SET





Al-SET is a very sensitive probe to detect the electronic environment nearby.





Al-SET is a very sensitive probe to detect the electronic environment nearby.

QD: source/drain grounded $V^{SET}_{SD} = 800 \mu V (DC) + 20 \mu V (AC)$



Classical memory bits become indistinguishable, which limits our ability to use them for computation.



The superposition of indistinguishable states is a key concept of quantum computation.

A quantum bit or qubit is a physical system with two quantum states.

Construct computation schemes and systems resembling operation of human brains

◇ Properties of human brain:
◇ Mass: ~1.5kg
◇ Volume:1.5l
◇ Energy consumption:~10W
◇ Information stored: 10¹⁴ bits
◇ 10¹³ bits/s



Summary

Message:

- The goal of nano-electronic research
- 1. Short term: the inventions of new-type device and materials that extend CMOS technology.
- 2. Long term: the inventions of completely new information technology.