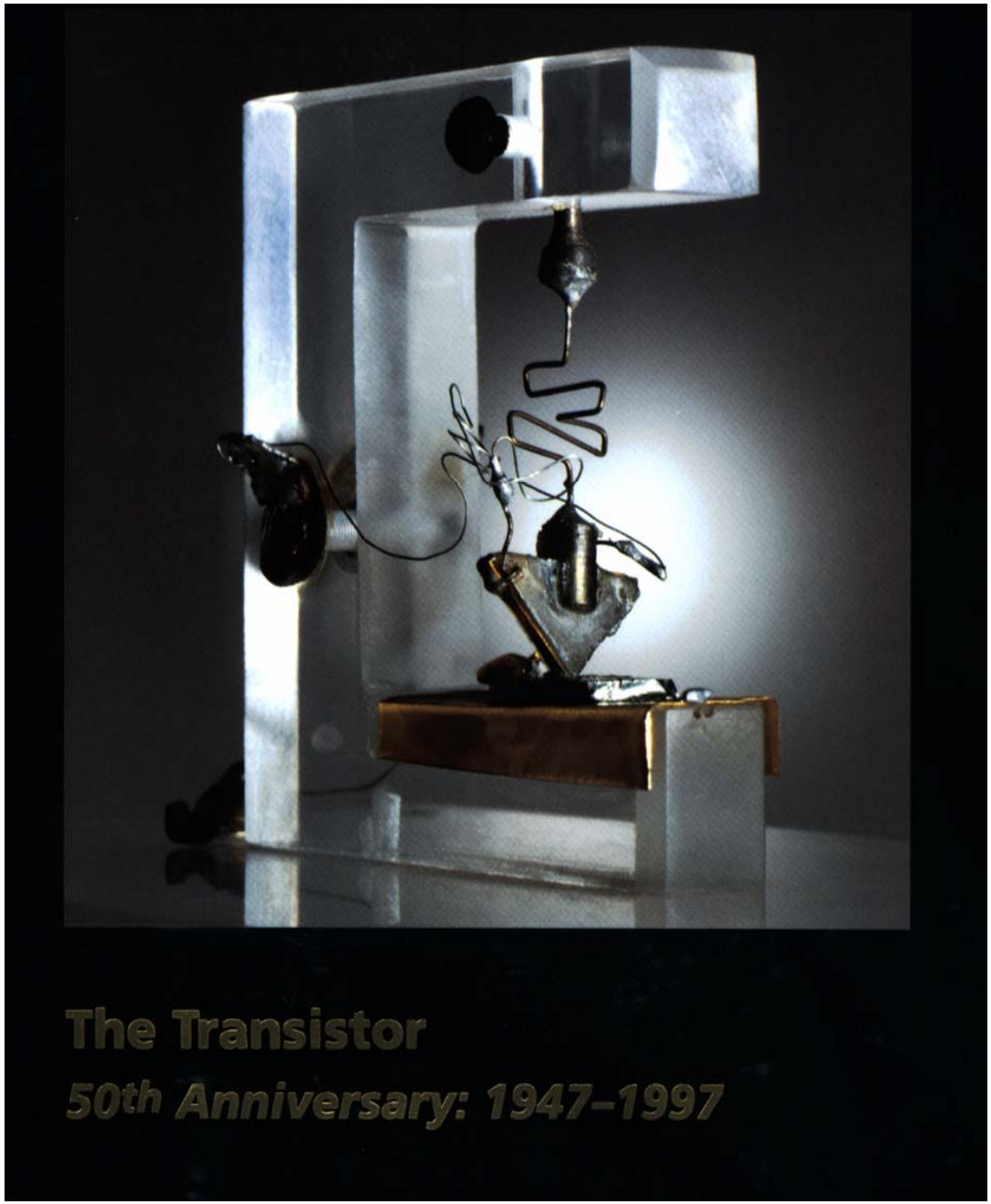
1897 J. J. Thomson discovery of electron



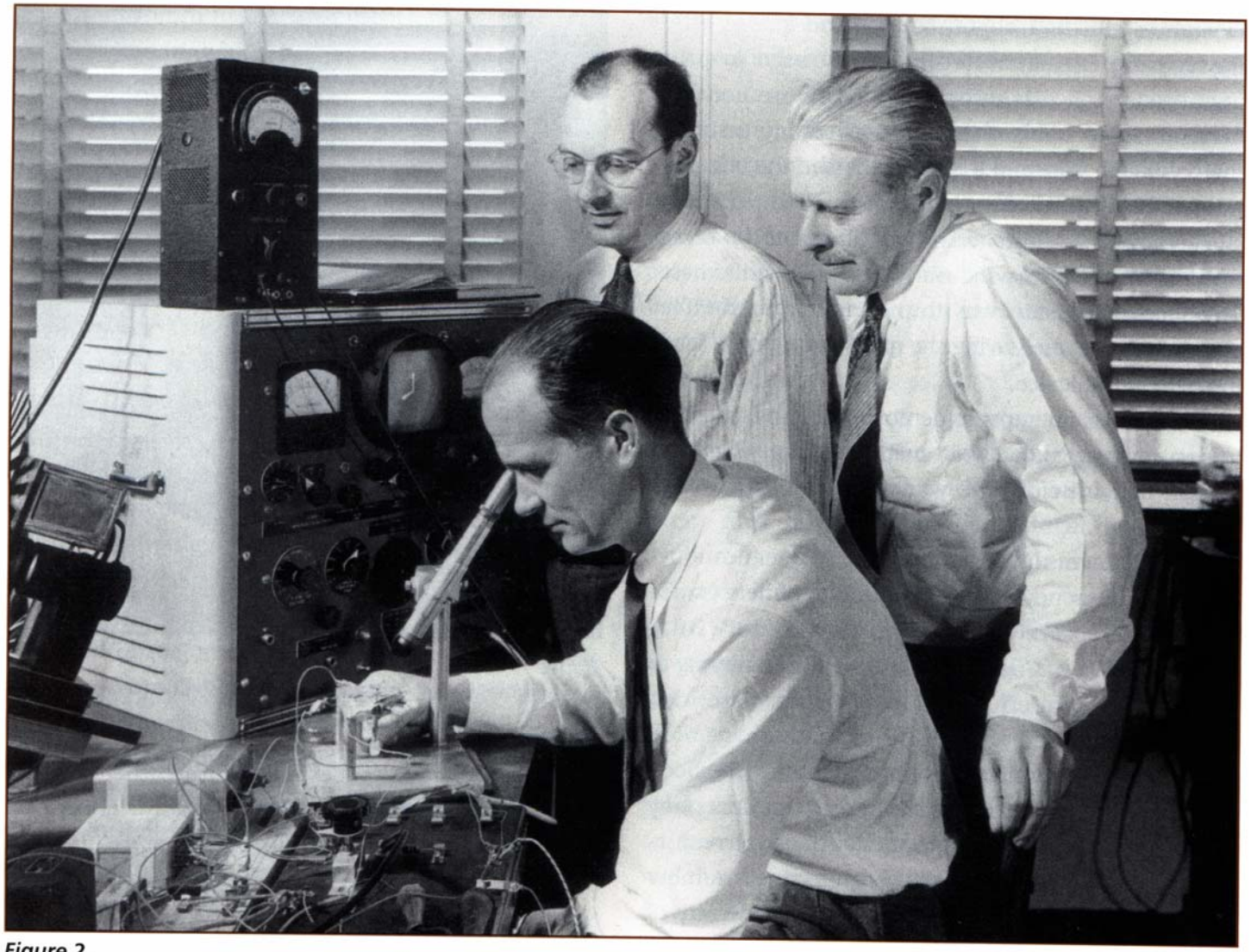


Figure 2.
The three inventors of the transistor: (left to right) William Shockley, John Bardeen, and Walter Brattain, who were awarded the 1956 Nobel Prize in physics.

William Shockley, John Bardeen, and Walter Brattain, Bell Labs

In the summer of 1947, any of a number of technical societies could have held a symposium to commemorate the 50th anniversary of J. J. Thomson's discovery of the electron. That 1947 event could surely qualify as the start of the electronics discipline and the industry that followed. It was the new understanding of the properties of the electron that created the field of electronics, and that, combined with our developing capability in the electrical, magnetic, and mechanical arts, enabled a rich array of new products and services.

The symposium would have been an upbeat event. Vacuum tube technology had fully matured with a wide range of tubes – diodes, pentodes, CRTs, klystrons, and traveling-wave tubes – in high-volume manufacture. Vacuum tubes were the key component in an array of electronic equipment that seemed to meet all conceivable information needs.

Mervin Kelly, the then Director of Research at Bell Labs who later became Bell Labs president, might well have been invited to submit a paper to the symposium. And he would also have been upbeat. Electromechanical relay technology was making possible fully automatic telephone dialing and switching. Microwave radio was providing high-quality telephone transmission across the continent. Again, available technology appeared capable of meeting conceivable needs.

Yet Kelly would have raised a word of caution. Although relays and vacuum tubes were apparently making all things possible in telephony, he had predicted for some years that the low speed of relays and the short life and high power consumption of tubes would eventually limit further progress in telephony and other electronic endeavors.

Not only had he predicted the problem, he had already taken action to find a solution.

In the summer of 1945, Kelly had established a research group at Bell Labs to focus on the understanding of semiconductors. The group also had a long-term goal of creating a solid-state device that might eventually replace the tube and the relay.

Kelley's vision trigged one of the most remarkable technical odysseys in the history of mankind, a journey that has continued through fifty years and longer. The semiconductor odyssey produced a revolution in our society at least as profound as the introduction of steel, of steam engines and the total Industrial Revolution. Today electronics pervades our lives and affects everything we do.

The progress made by semiconductor physics, from what was described by Wolfgang Pauli as 'Physik der Dreckeffekte' or 'dirt physics' in 1920s, over the eight decades or so of the last century is truly amazing. The technological revolution unfolded by this progress has ushered in a new epoch in human civilization. The information age is but a spin-off of this revolution. Arguably no other field of human endeavor has had such a profound and wide ranging impact on human society over the last century. The story of this march from 'dirt physics' to such subtle and complex effects as the fractional quantum Hall effect (FQHE) is full of numerous exciting thrills ranging from our deeper understanding of the defect (dirt) states and how to control them to a level where semiconductors rank among the cleanest man-made materials with unparalleled purity, so high as to exhibits ever unknown physical phenomena such as FQHE and Wigner crystallization.

(Semiconductor hetero-structures (AlGaAs-GaAs) made by MBE.)

But what has really reached the common man out of this progress is the phenomenal range of electronic applications which have unleashed a flood of consumer goods and communication gadgets, starting from the wireless radio to the present day personal computer and the mobile phone, coupled with the software resolution engendered by the Internet.

MBE – compound semiconductor growth

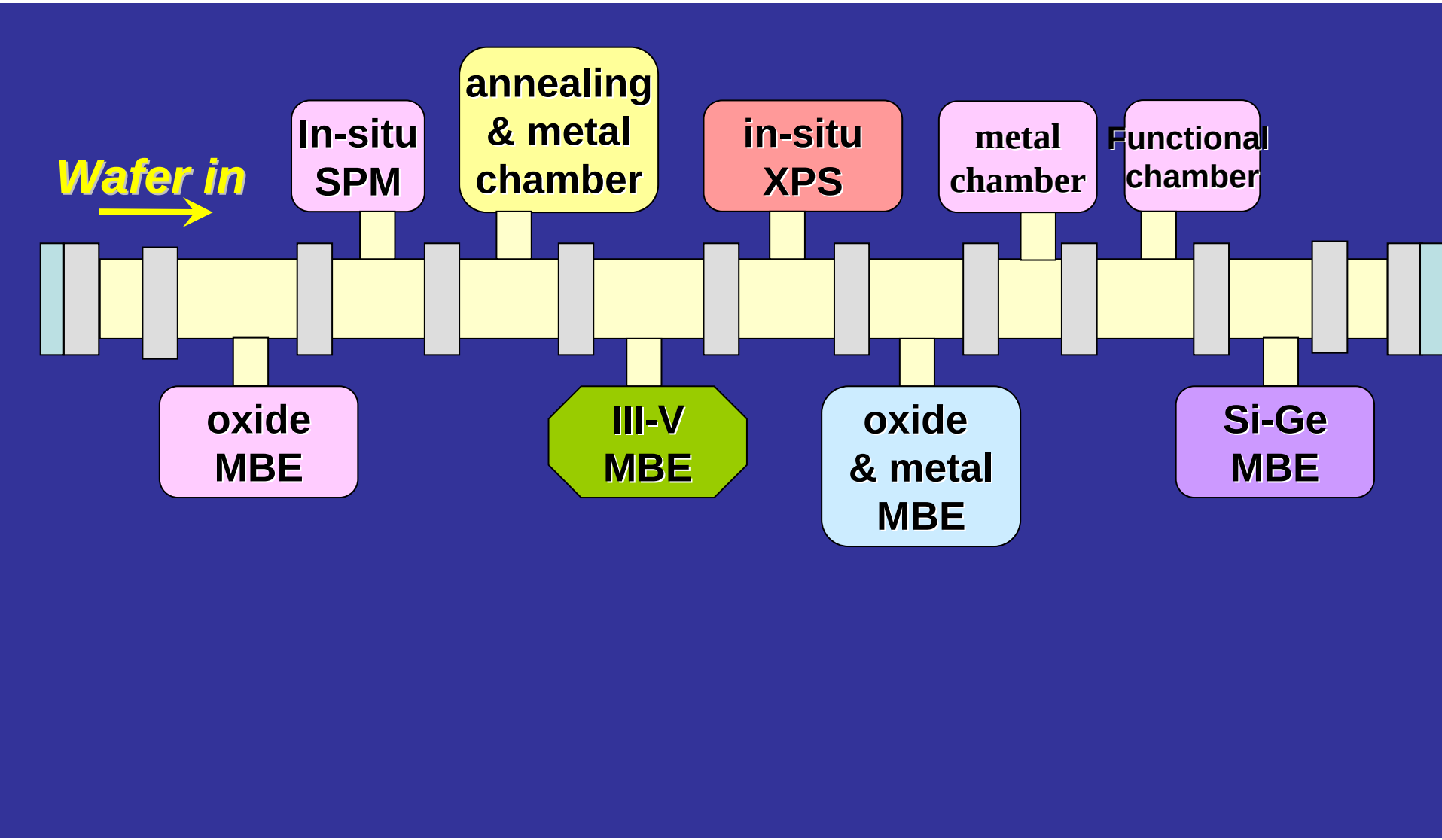
- Alfred Y. Cho (卓以和) and co-workers
- RHEED (reflection high energy electron diffraction)
- Liquid nitrogen shroud
- Load-lock chamber vs single chamber (New Jersey humid weather affecting semiconductor laser life time)
- Ion pump, cryo-pump, turbo pump, mercury pump, diffusion pump, dry pump, mechanical pump, absorption pump, etc
- Effusion cells
- Flux gages
- Manipulator
- Heaters
- GaAs wafer surface oxide absorption

MBE – metal and oxide growth

- Raynien Kwo (郭瑞年) and co-workers
- Electron mean-free path
  - In metals vs in semiconductors
- Metal superlattices
  - Historical background
    - Cu-Ni compositional multi-layers
      - Enhancement of magnetic moments and elastic modules
- Magnetism
  - Rare earth superlattices
    - Long range coupling
      - Ferro- and anti-ferro-magnetic coupling
  - GMR
- Non-alloyed ohmic contacts
- Schottky barrier
- Silicide (WSi, CoSi, etc) on Si
  - Metal base transistors
- $Fe_3(Al,Si)$, CoNi, etc on GaAs

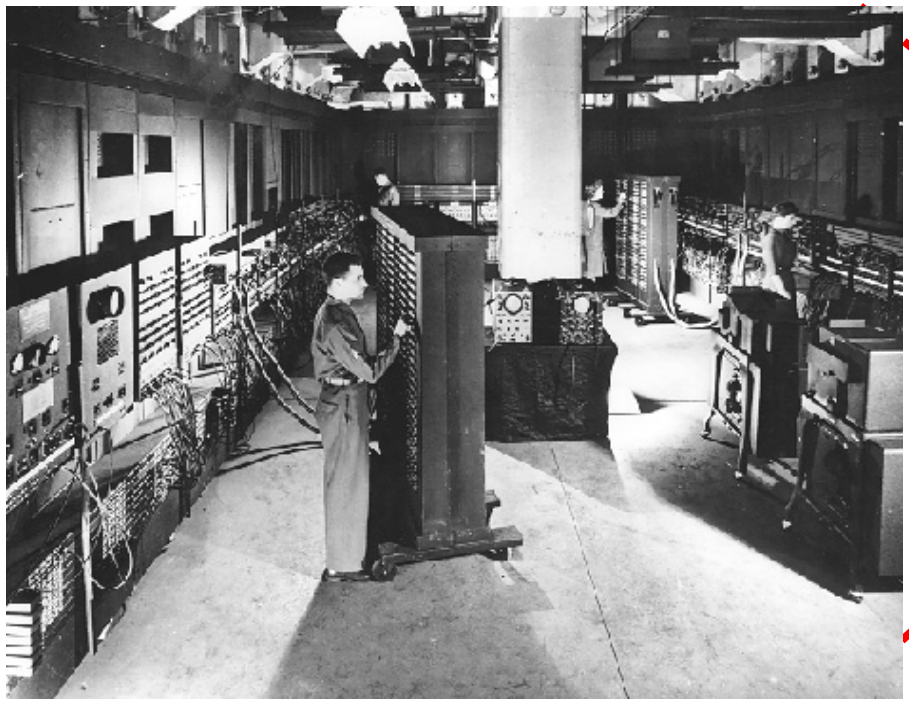
- MBE growth chamber
  - RHEED
  - Liquid nitrogen shroud
  - Load-lock chamber vs single chamber (humid weather in Taiwan)
  - Ion pump, cryo-pump, turbo pump, diffusion pump, dry pump, mechanical pump, absorption pump, etc
  - Effusion cells and e-guns
  - Charges (or source materials)
  - Flux gages
  - Manipulator
  - Heaters
  - substrates? Unlike GaAs or Si growth

Multi-chamber MBE/in-situ analysis system

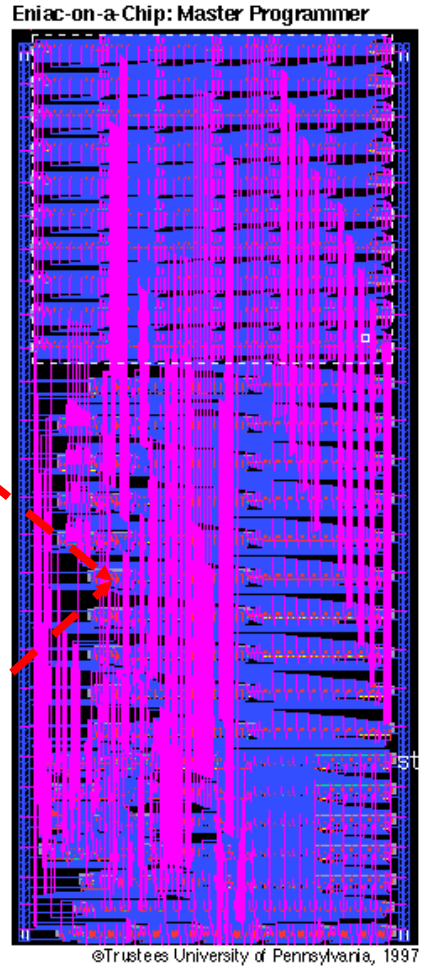


I think that there's a world market for about 5 computers.

Thomas J. Waston, Sr.
IBM Chairman of the Board, ca1946



The ENIAC machine occupied a room 30 x 50 ft. (van Pelt Library, U Penn)



Size: **7.44mm x 5.29mm**; 174,569 transistors; 0.5 um CMOS technology

Intel (Sematech) Transistor Scaling and Research Roadmap

Ultimate scaling of CMOS

(22 nm node and beyond)

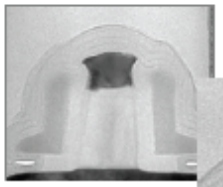
90nm Node
2003

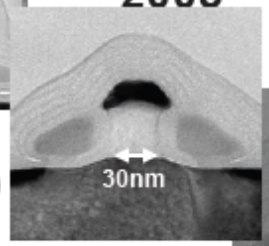
65nm Node
P1264
2005

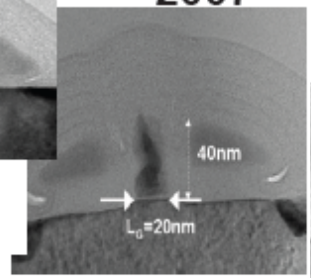
45nm Node
P1266
2007

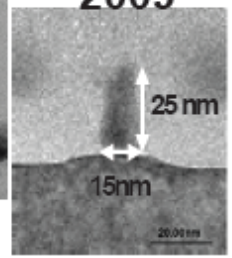
32nm Node
P1268
2009

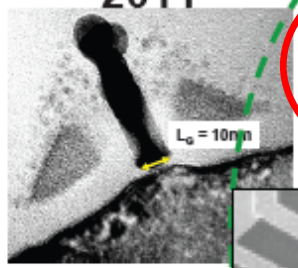
22nm Node
P1270
2011



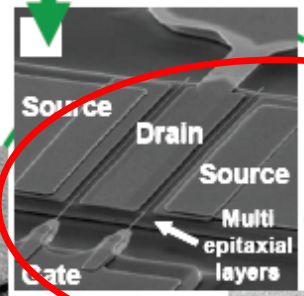




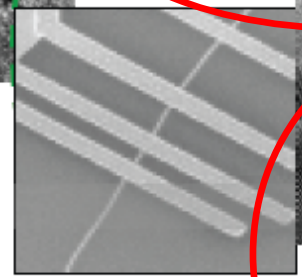




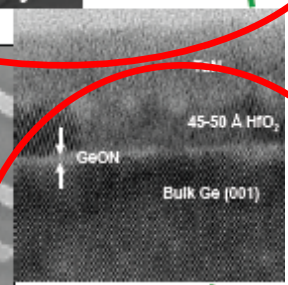
2013-2019



III-V Device Prototype (Research)



C-nanotube Prototype (Research)



Ge Device Prototype (Research)

(Production)

(Development)

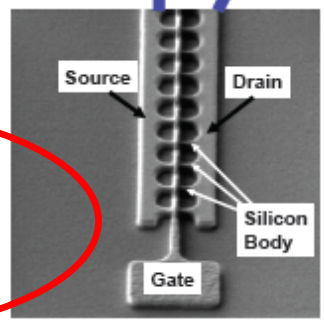
Uniaxial Strain

SiGe S/D

(Development)

(Research)

(Research)



Tri-Gate Architecture

High-K/ Metal-Gate

The drive for alternative high k dielectrics (for replacing SiO_2) and metal gates initiated a decade ago has resulted in a recent ***Intel's news announcement of high k + metal gate transistor breakthrough on 45 nm microprocessors,*** indeed a scientific and technological achievement. The high k dielectrics have shown impressive properties with an equivalent oxide thickness (EOT), defined as teq (k_{SiO2} /k_{oxide}), as thin as or even less than 1.0 nm. These relevant parameters include dielectric constant, band gap, conduction band offset, leakage, mobility, and good thermodynamic stability in contact with Si up to 1000ºC. However, Coulomb scattering from charge trapping and the phonon issue related to high k gate dielectrics leads to degraded channel mobility.

It is adamant with consensus that beyond the 22 nm node technology, higher mobility-channel materials such as III-V compound semiconductors and Ge have to be employed.

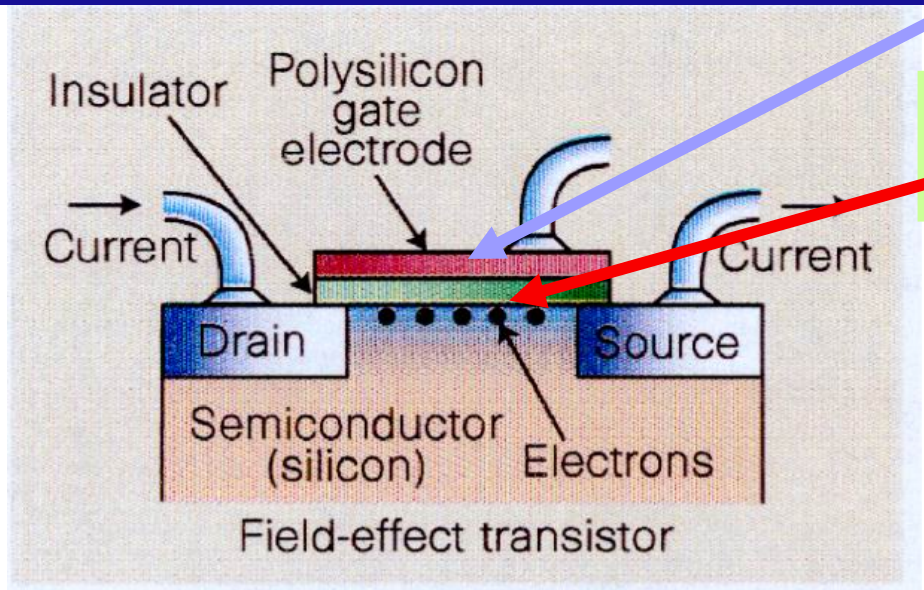
	Si	GaAs/$In_{0.2}Ga_{0.8}As$	InP/ $In_{0.53}Ga_{0.47}As$/ $In_{0.7}Ga_{0.3}As$	GaN	InAs	InSb	units
Energy gap	1.12	1.43	0.75	3.40	0.354	0.17	eV
Lattice constant	5.431	5.65	5.87	3.19	6.06	6.50	Å
Electron effective mass	0.19	0.063	0.041	0.20	0.023	0.014	-
Electron mobility	1500	8500	14000	1300	25000	78000	$cm^2 V^{-1} s^{-1}$
Electron saturation velocity	1×10^7	2×10^7	8×10^6	3×10^7	3×10^7	5×10^7	$cm\ s^{-1}$
Electron mean free path	0.07	0.15	0.19	0.2	0.27	0.58	μm

Motivation

- Rapid shrinkage of transistor size in Si industry
  - 65 nm node in production, 50 nm or smaller in R&D, with channel length ~ 10 nm by 2010, and SiO_2 thickness to quantum tunneling limit of 1.0nm
  - Called for replacing SiO_2 with high k dielectrics; EOT as thin as 1.0 nm or less
  - Coulomb scattering and phonon issue related to high k gate dielectrics leading to degraded channel mobility
  - higher mobility materials such as **Ge**, and **III-V's**
- Ge MOSFET
  - Ge offers **two times higher mobility for electrons** and **four times higher for holes** comparing with Si
  - lack of stable native oxide hindering Ge passivation, making fabrication of Ge MOSFET difficult
- III-V MOSFET (III-V's: GaAs, InSb, InAs, GaN,….)
  - **electron mobility in III-V's much higher than those in Si and Ge**
  - A mature III-V MOS technology with electron mobilities at least 10 times higher than that in Si and with dielectrics having k several times higher that of SiO_2 would certainly enable the electronic industry to continue pushing its new frontiers for a few more decades
  - **bandgap engineering and direct bandgaps in the III-V's**, not available in Si- and Ge-based systems, providing novel designs and making highly-performed **integrated optoelectronic circuits of combining MOS and photonic devices a reality**

Device Scaling, Moore's Law

1960 Kahng and Atalla, First MOSFET



Moore's Law:
The number of transistors per square inch doubles every 18 months

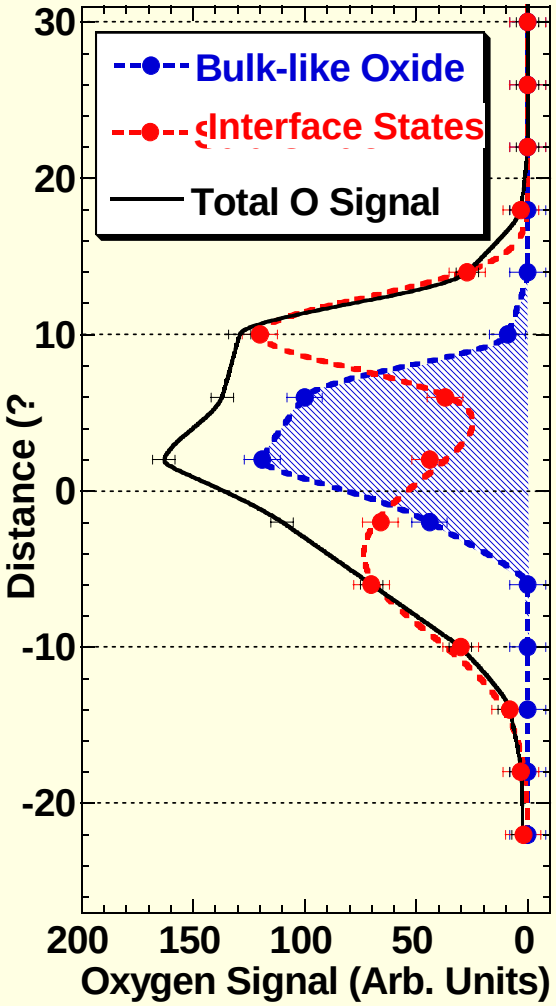
Shorter gate length L
Thinner gate dielectrics t_{ox}

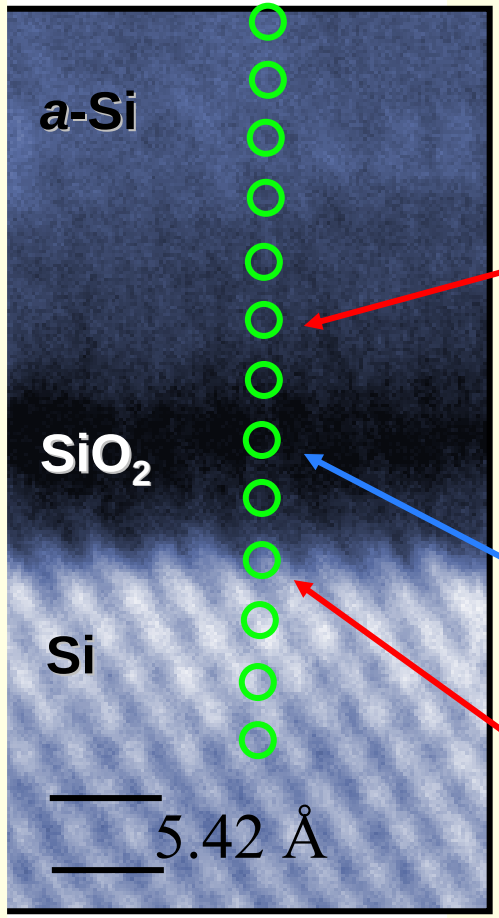
Driving force :
High speed
Lower power consumption
High package density

Oxygen Bonding from EELS (Chemistry on an Atomic Scale)

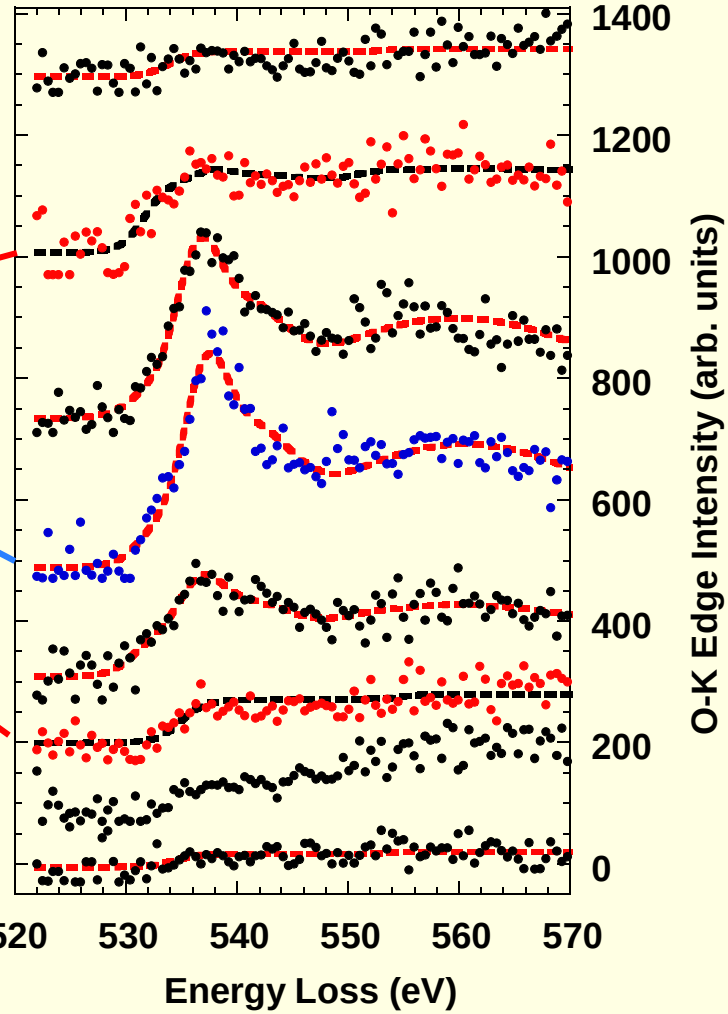
Nominal 1.1 nm SiO_2:

1.6 nm wide oxygen profile





STEM Image



CMOS scaling, When do we stop ?

Reliability: 25 22 18 16 Å

processing and yield issue

Tunneling : 15 Å

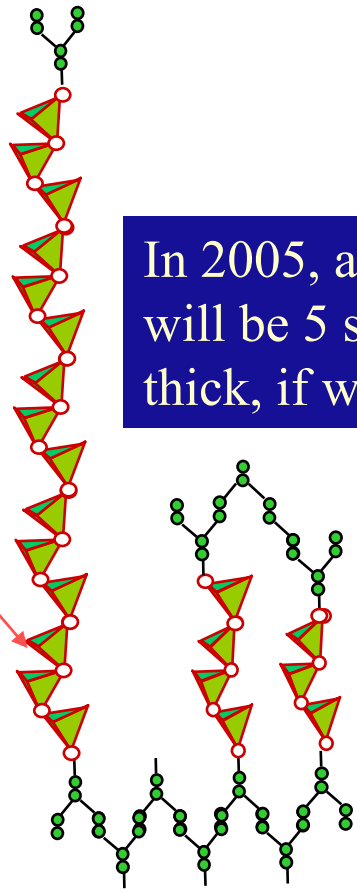
Design Issue: chosen for 1A/cm^2 leakage
I_{on}/I_{off} >> 1 at 12 Å

Bonding:

Fundamental Issues---

- How many atoms do we need to get bulk-like properties?
  EELS -- Minimal 4 atomic layers !!
- Is the interface electronically abrupt?
- Can we control roughness?

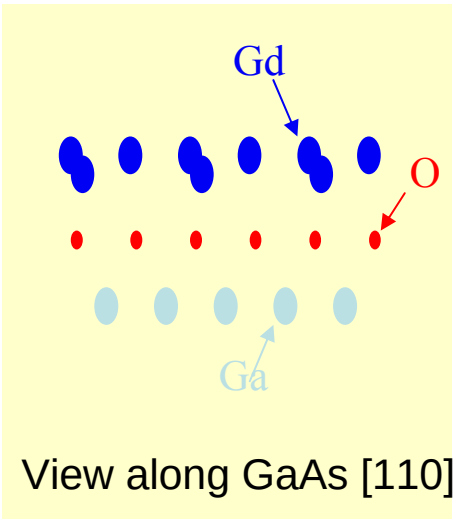
In 1997, a gate oxide was 25 silicon atoms thick.



In 2005, a gate oxide will be 5 silicon atoms thick, if we still use SiO_2

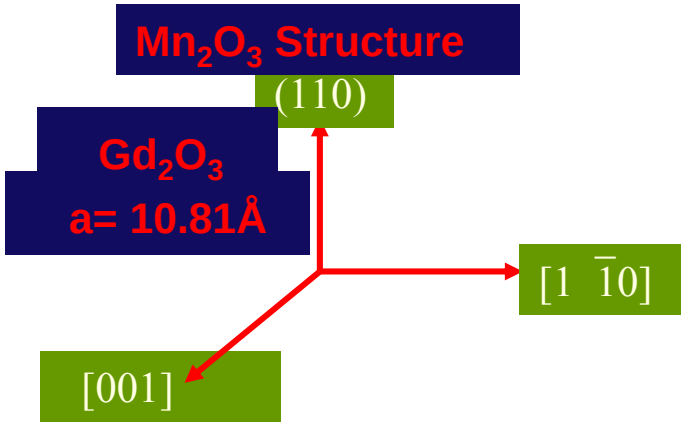
and at least 2 of those 5 atoms will be at the interfaces.

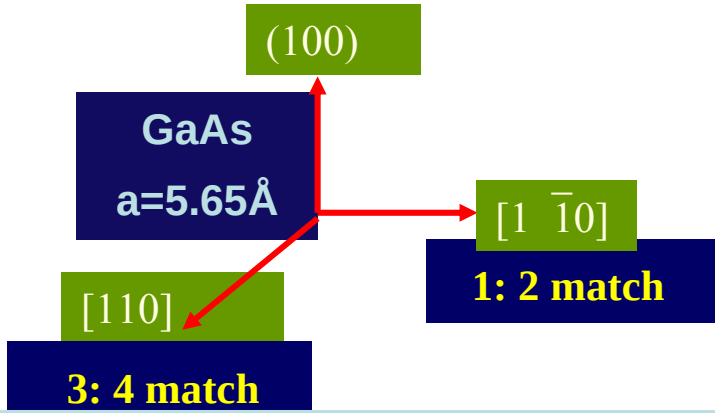
Pioneer Work : Single Domain Growth of (110) Gd_2O_3 Films on (100) GaAs



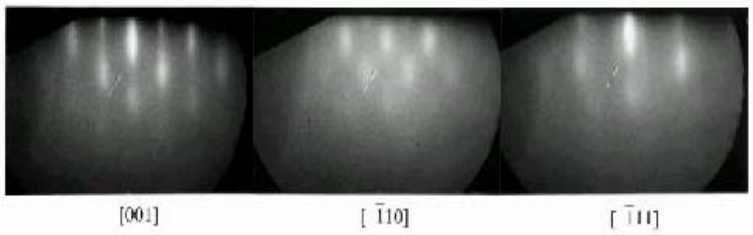
View along GaAs [110]

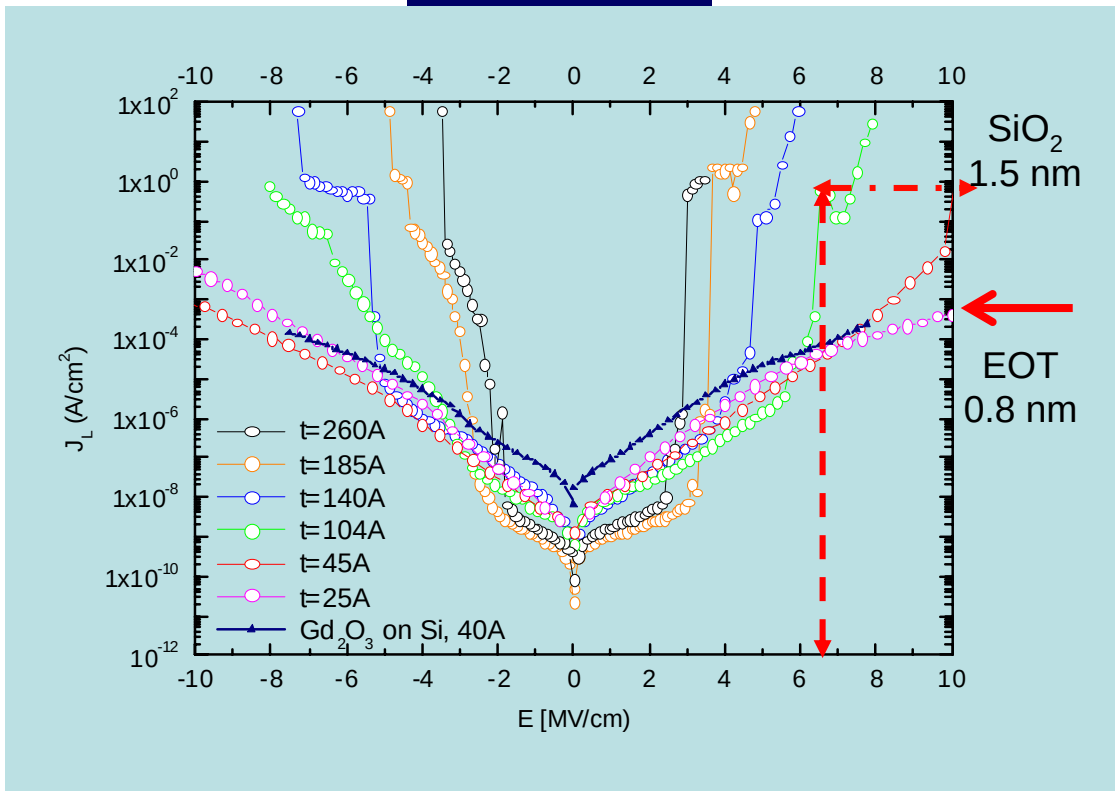
M. Hong, J. Kwo et al, Science 283, p.1897, 1999





Gd_2O_3 (110) 25Å



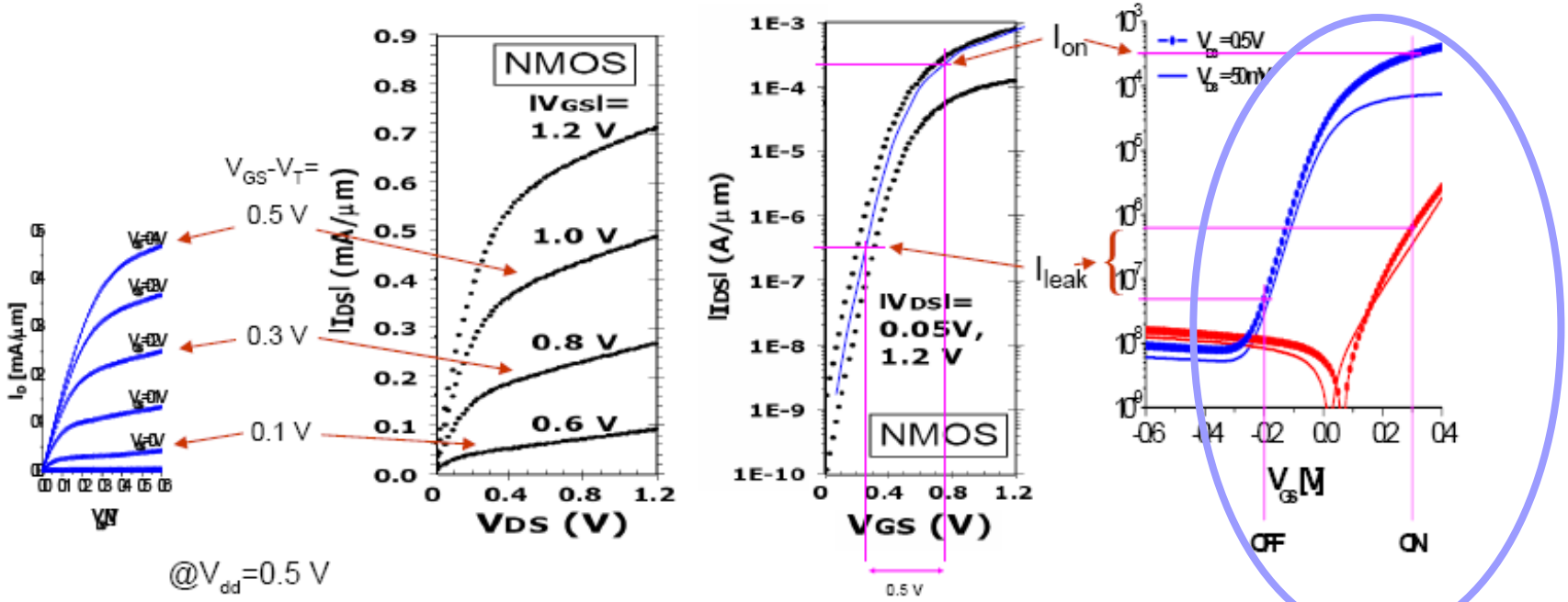


Inventions of GaAs and InGaAs MOSFET's

- 1994
  - novel oxide $Ga_2O_3(Gd_2O_3)$ to effectively passivate GaAs surfaces
  - demonstration of low interfacial recombination velocities using PL
- 1995
  - establishment of accumulation and inversion in p- and n-channels in $Ga_2O_3(Gd_2O_3)$-GaAs MOS diodes with a low D_{it} of 2-3 x 10^{10} cm^{-2} eV^{-1}(IEDM)
- 1996
  - first e-mode GaAs MOSFETs in p- and n-channels with inversion (IEDM)
  - Thermodynamically stable
- 1997
  - e-mode inversion-channel n-InGaAs/InP MOSFET with g_m= 190 mS/mm, and mobility of 470 cm^2/Vs (DRC, EDL)
- 1998
  - d-mode GaAs MOSFETs with negligible drain current drift and hysteresis (IEDM)
  - e-mode GaAs MOSFETs with improved drain current (over 100 times)
  - Dense, uniform microstructures; smooth, atomically sharp interface; low leakage currents
- 1999
  - GaAs power MOSFET
  - Single-crystal, single-domain Gd_2O_3 epitaxially grown on GaAs
- 2000
  - demonstration of GaAs CMOS inverter
- 2001-2002
  - Design of high-speed and high-power devices; reliability of devices

Comparison with 65 nm CMOS

Intel's 65 nm low-power CMOS (IEDM '05)



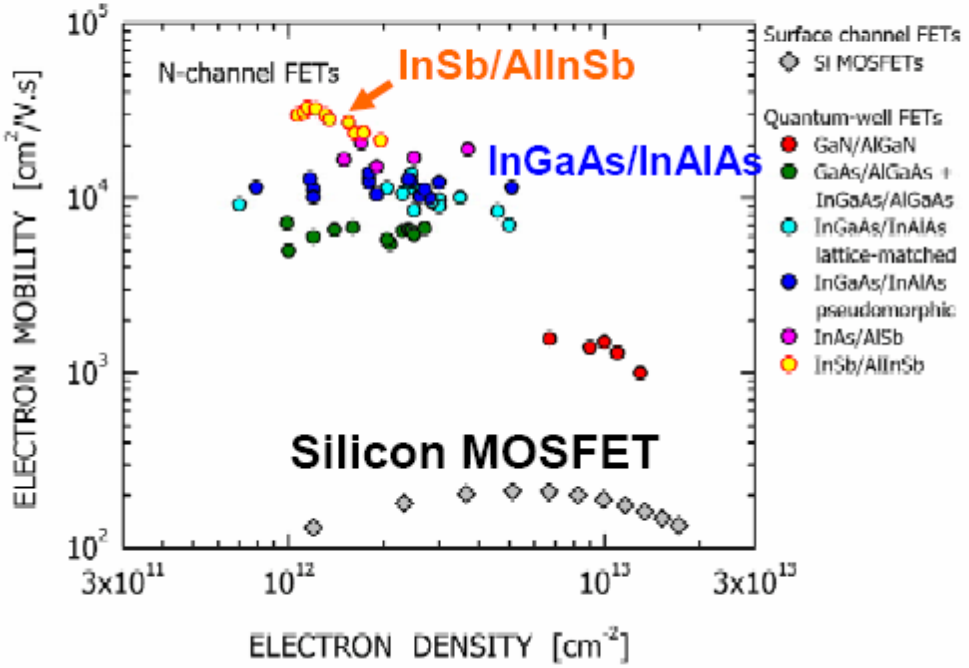
	L_g (nm)	I_{on} (mA/mm)	I_{leak} (nA/mm)	S (mV/dec)	DIBL (mV/V)
InGaAs HEMT	60	320	330	70	44
65 nm CMOS (low power)	55	220	330	90	80

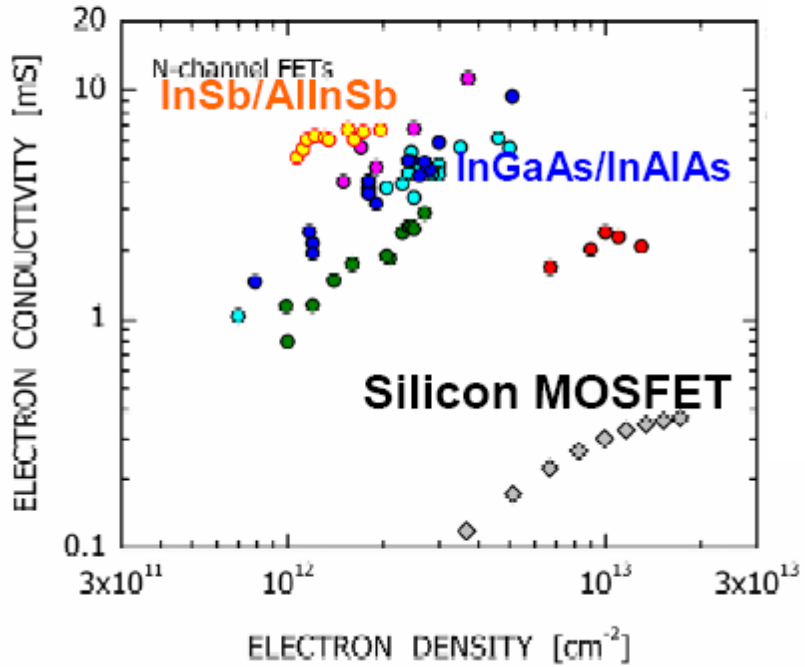
For the same I_{leak}, 60 nm InGaAs HEMT yields 45% more I_{ON} than 65 nm CMOS

J. A. del Alamo, D.-H. Kim, and N. Waldron, **Intel III-V CMOS Conference, Sept. 9, 2006**

A III-V MOS will make I_{on}/I_{off} ratio to $>10^7$, acceptable in the IC industry

Why III-V Research for Future Logic Applications?

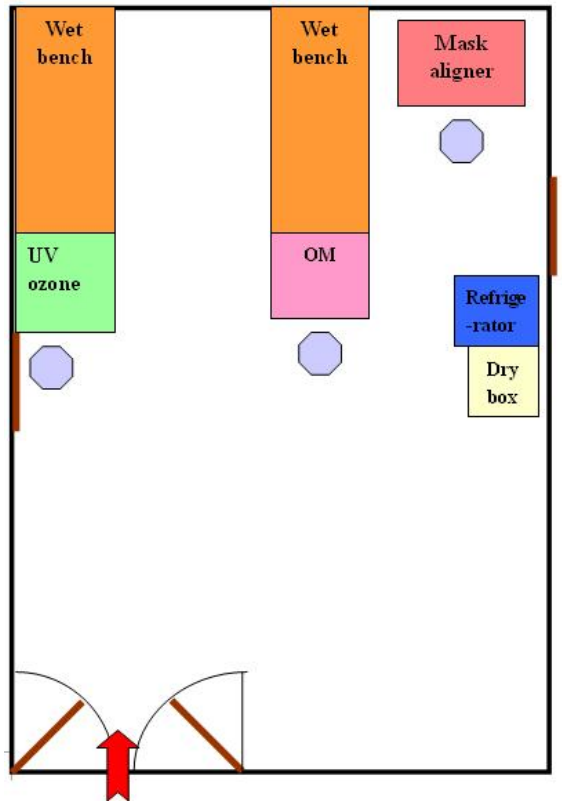


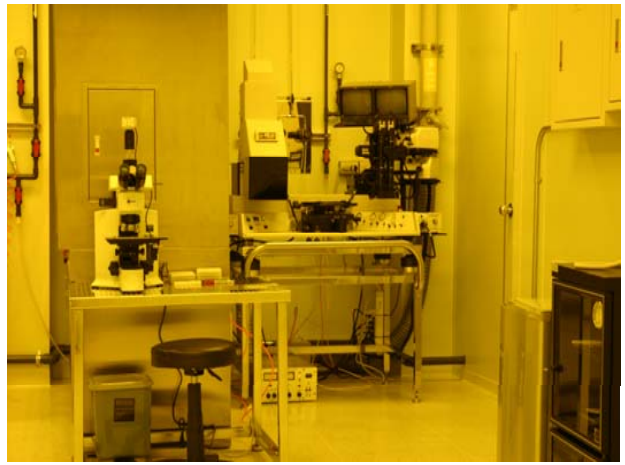


- III-V has been used in commercial communication & optoelectronics products for a long time
- III-V quantum-wells show ~100X higher electron mobility and ~20X higher electron conductivity than Si ➔ [potentially high-speed + low-power]
- Top-down patterning as opposed to bottom-up chemical synthesis
- III-V will NOT replace Si; it will need to be integrated onto Si

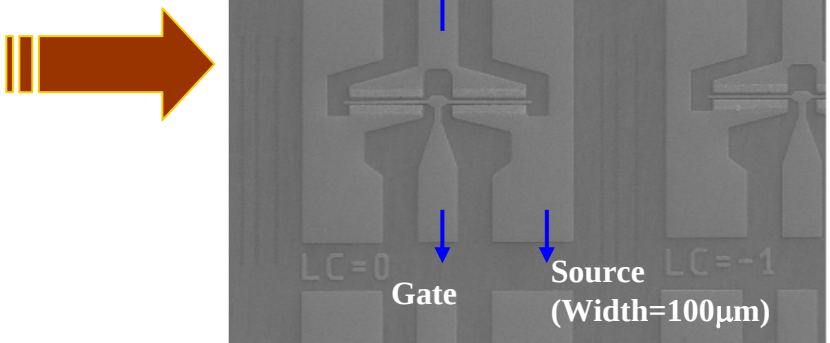
R. Chau
Intel Senior Fellow
2006 DRC

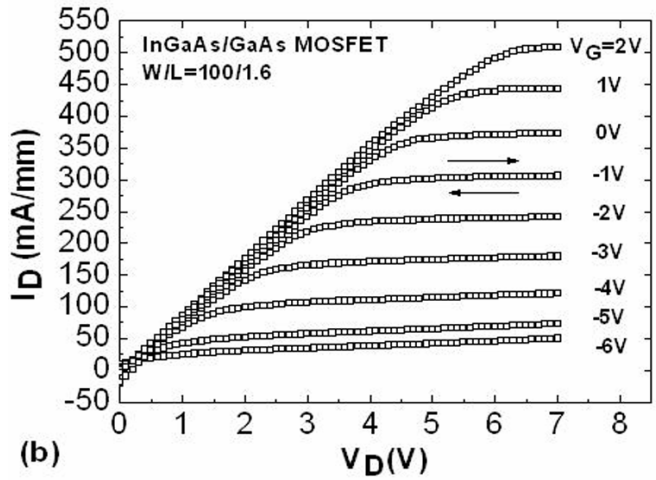
III-V Nano Electronics Processing Lab





- **ABM mask aligner →** sub-micro gate length capability
- **UV-ozone →** surface cleaning
- **Olympus OM→** image catch and sub-micro measurement capability
- **ULVAC ICP-RIE →** dry etch of metal gates (***move in soon)***





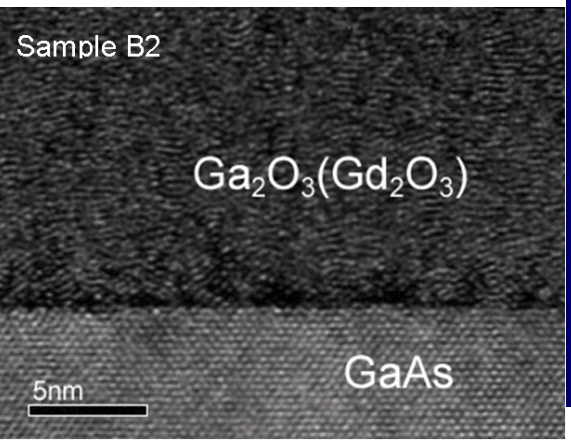
$Ga_2O_3(Gd_2O_3)$ and JVD (MAD) Si_3N_4 on InGaAs

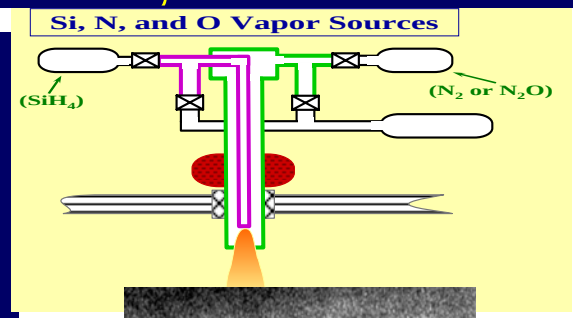
Intel J. F. Zheng, W. Tsai, Natl Tsinghua- M. Hong, J. Kwo, Yale – T.P. Ma

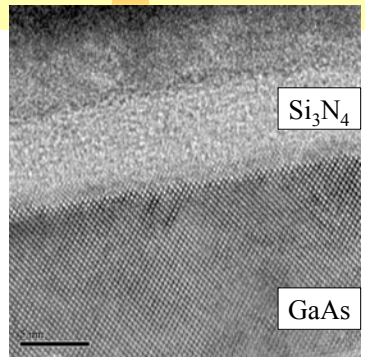
GGG Stable up to 800C for process integration

A new dual dielectric approach:

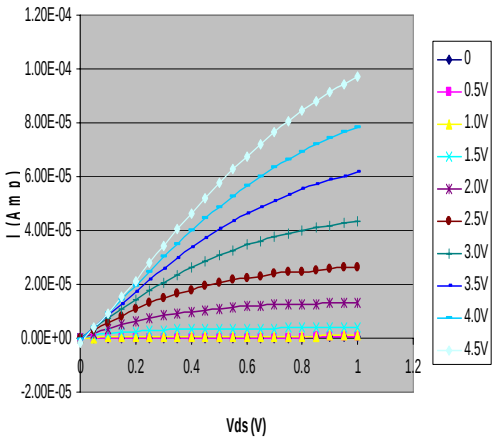
1. GGG dielectric is part of the MBE channel grown – unpin Fermi level
2. A second dielectric can be high-k to reduce EOT toward few nm
3. Principle of proof dual dielectric approach with 5nm EOT GGG and trap less JVD (MAD) Si_3N_4 (after high temperature PDA)

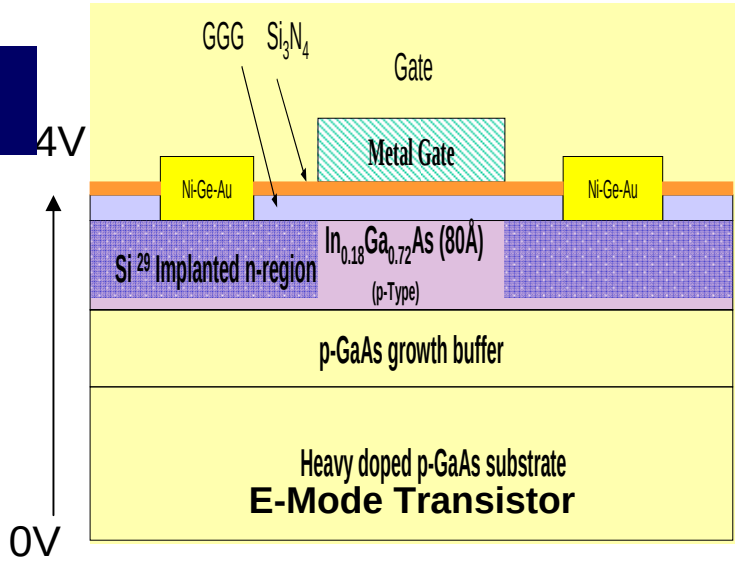




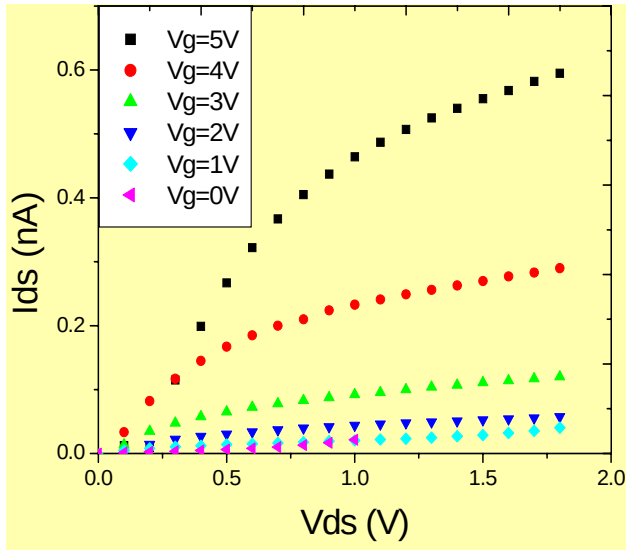


Enhancement Mode with inversion using GGG

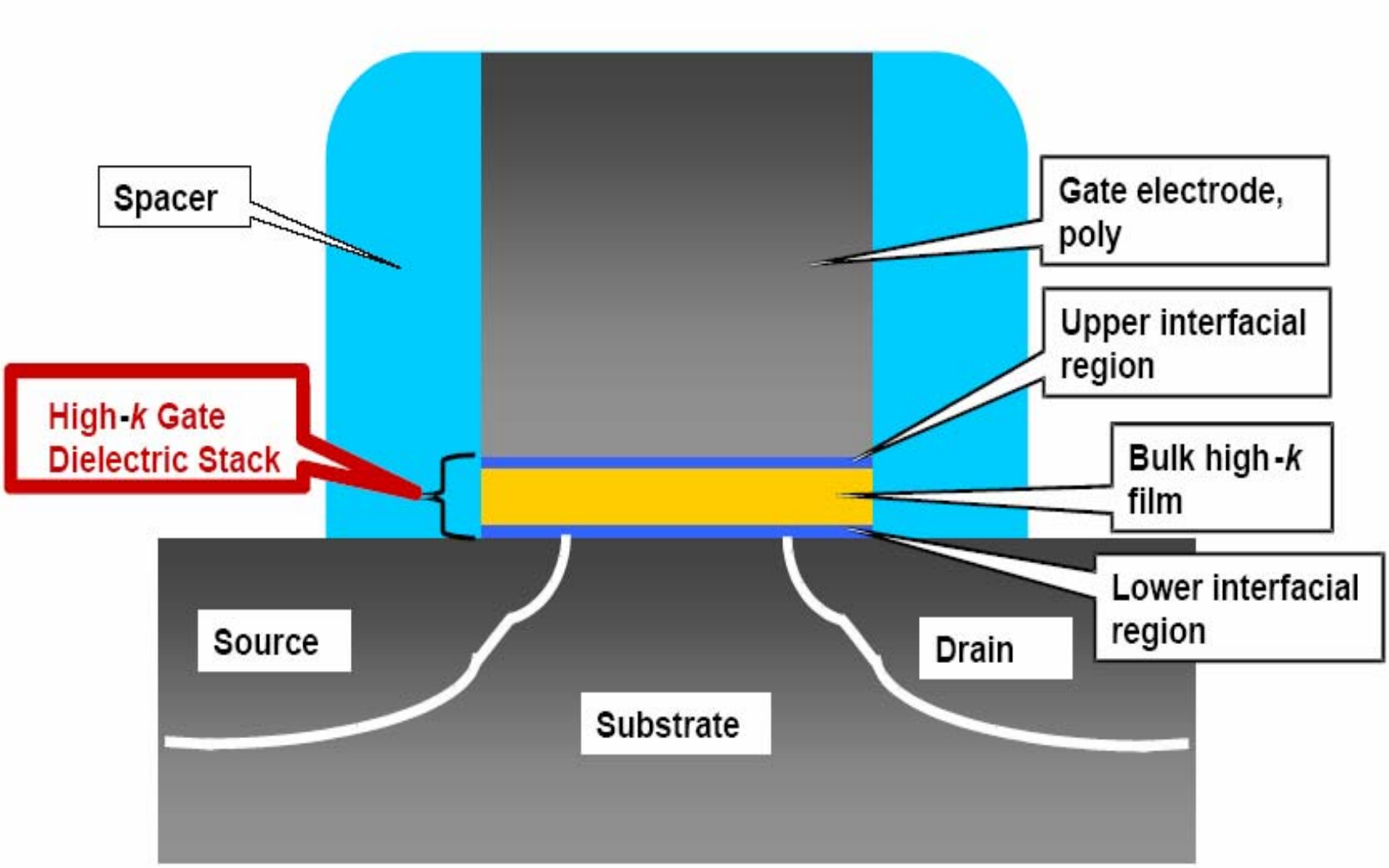




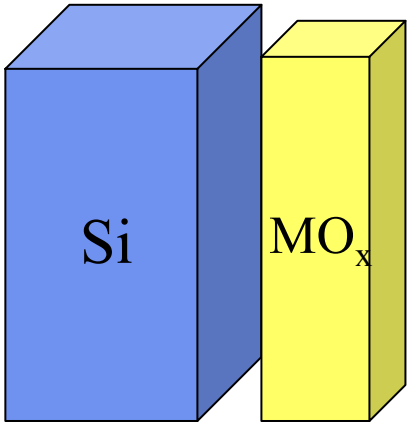
Enhancement Mode with inversion using Si_3N_4



High κ Gate Dielectric MOSFET



Fundamental Materials Selection Guidelines



$Si + MO_x \rightarrow M + SiO_2$

$Si + MO_x \rightarrow MSi_2 + SiO_2$

$Si + MO_x \rightarrow MSiO_x + SiO_2$

- Thermodynamic stability in contact with Si to 750ºC and higher. **(Hubbard and Schlom)** **Alkaline earth oxide, IIIB, IVB oxide and rare earth oxide**
- Dielectric constant, band gap, and conduction band offset
- Defect related leakage, substantially less than SiO_2 at $t_{eq} < 1.5$ nm
- Low interfacial state density $D_{it} < 10^{11}\ eV^{-1}cm^{-2}$
- Low oxygen diffusivity
- Crystallization temperature >1000°C

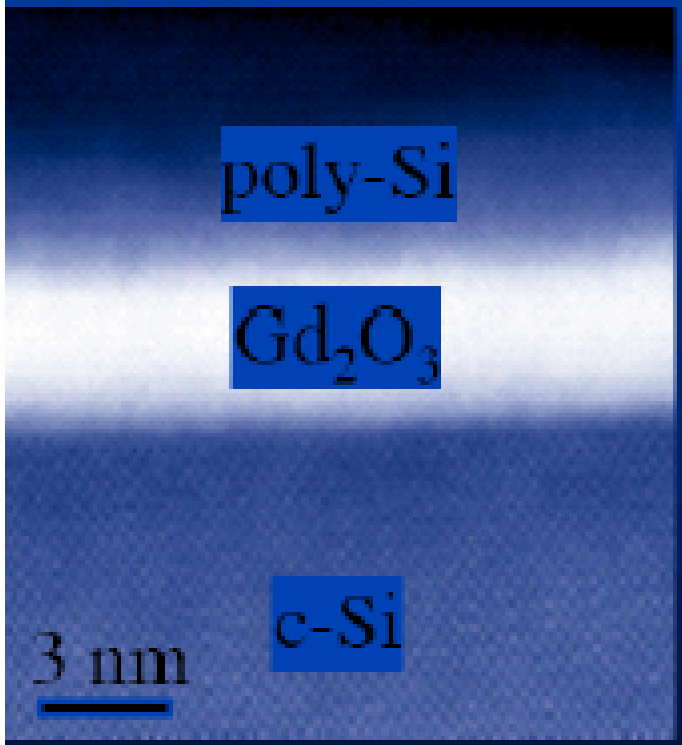
Assessing Thermodynamic Stability

Gate Dielectric Material

Silicon

Ideal "Gedanken" Interface

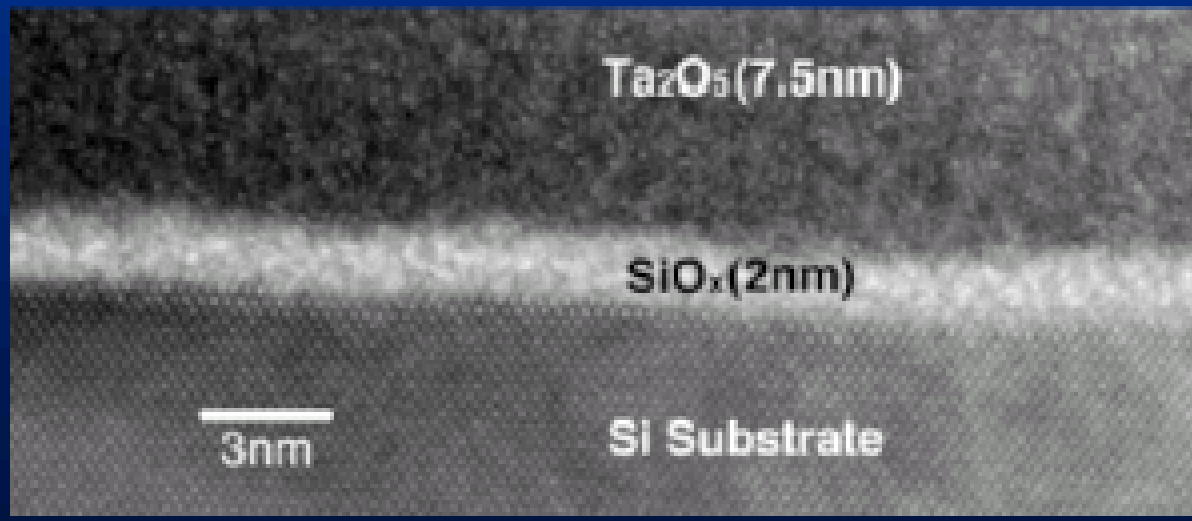
Stable Interface



TEM by David A. Muller

J. Kwo *et al.*, J. Appl. Phys. 89 (2001) 3920.

Unstable Interface



TEM by Don J. Werder

G.B. Alers *et al.*, Appl. Phys. Lett. 73 (1998) 1517.

Electrical Properties of the High κ Gate Dielectrics

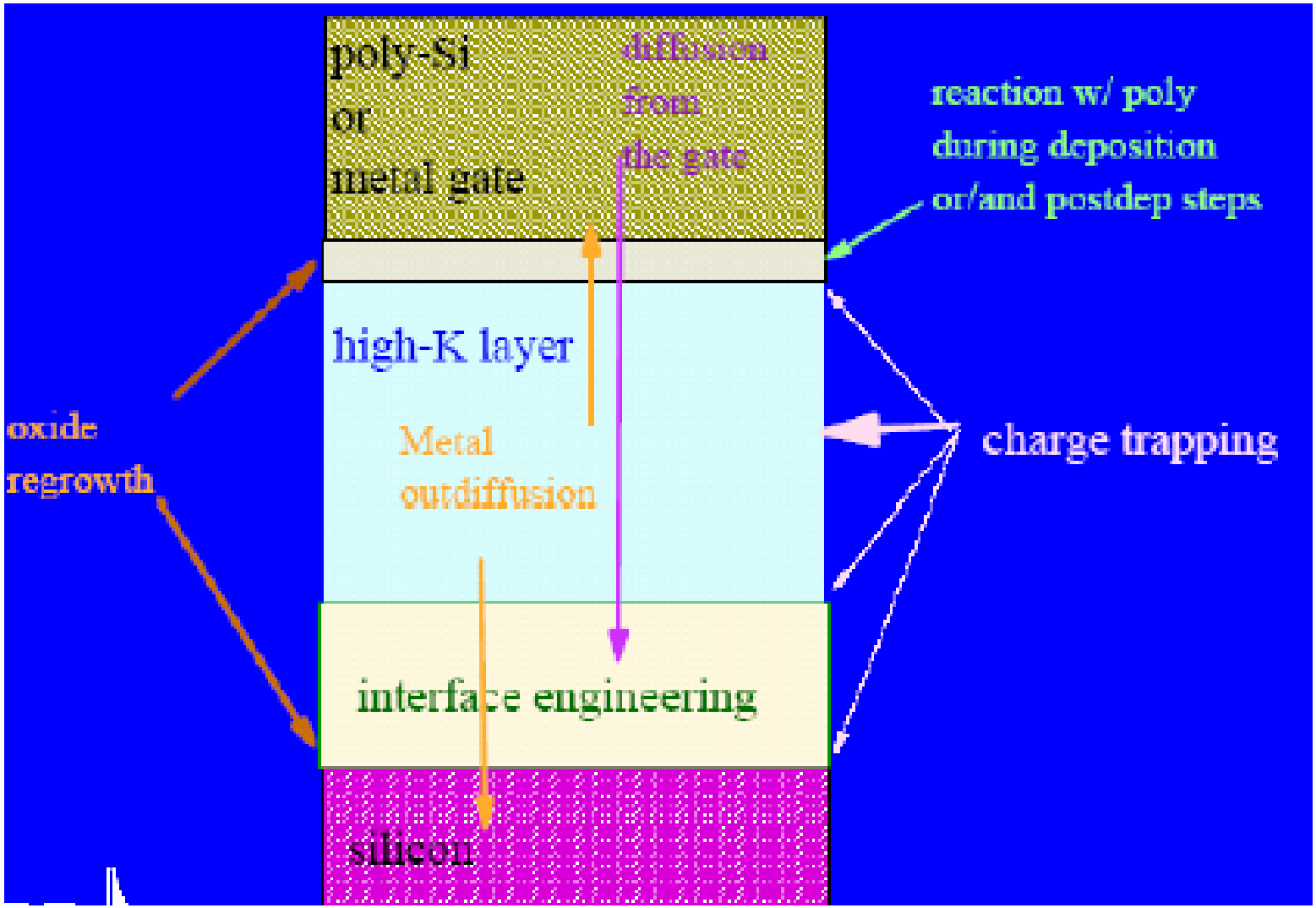
Good News !!

Low electrical leakage is common, EOT under 1.2-1.4 nm

Major problems :

- High interfacial state density
- Large trapped charge
- Low channel mobility
- Electrical stability and reliability

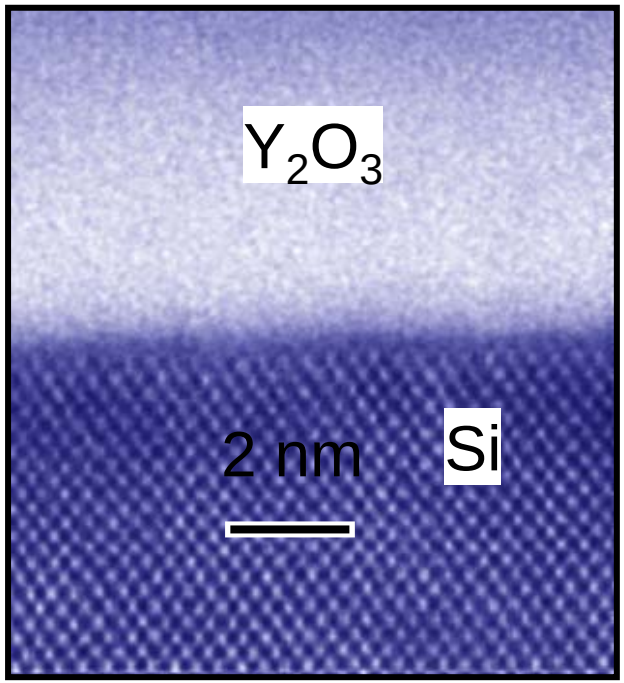
Some Major Issues in High κ Gate Stacks



In-situ UHV integrated functional system

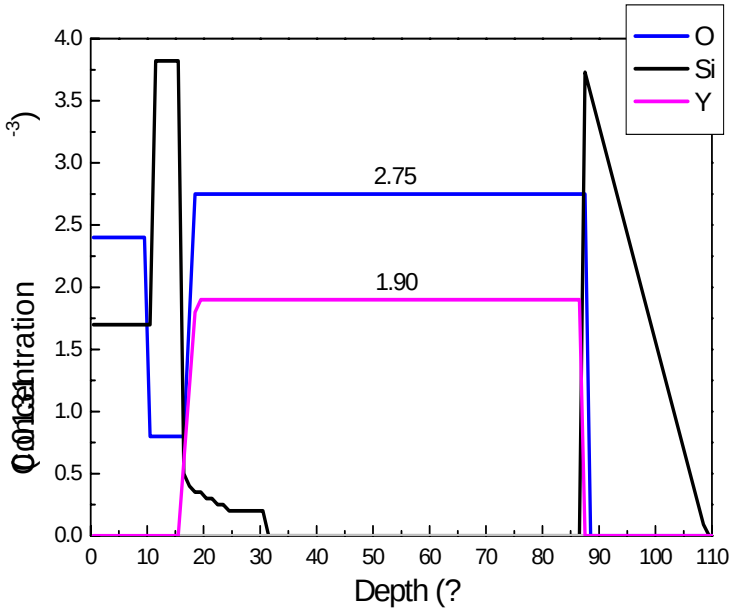
The First Abrupt Y_2O_3/Si Interface

STEM Cross Sectional Images



(Thick cross section)

Medium Energy Ion Scattering
With Rutgers University



Amorphous Si/Y_2O_3/Crystalline-Si

NOVEL GATE DIELECTRICS FOR III-V SEMICONDUCTORS

How to passivate GaAs surface? **Previous efforts over thirty five years !**

❖ **Previous Efforts**

- Anodic, thermal, and plasma oxidation of GaAs
- Wet or dry GaAs surface cleaning followed by deposition of various dielectrics

Growth using single chamber

- AlGaAs doped with O or Cr, Cho and Cassey 1978
- Native oxides or Al2O3 on GaAs during the same growth, i.e. introduction of oxygen in III-V MBE chamber, Ploog et al 1979
- ZnSe (lattice constant of 5.67Å and a E_g 2.7 eV) on GaAs, Yao et al, 1979
- Si on InGaAs or GaAs, IBM at Zurich 1990 (?) and Morkoc et al, 1996

❖ **Our Breakthrough** Growth using multiple chambers

- Novel gate oxides $Ga_2O_3(Gd_2O_3)$ and Gd_2O_3 in-situ deposited by e-beam evaporation with low D_{it}
- Have applied to GaAs, InGaAs, AlGaAs, InP, GaN, and Si

THE KEY is to clean GaAs surface and to identify a dielectric being thermodynamically and electronically stable, and showing low D_{it} with GaAs.

NOVEL DIELECTRICS FOR III-V SEMICONDUCTORS

Effective Passivation of GaAs

- **GaAs MOSFET**
  - **Advantages**
    - inherent higher electron mobility and semi-insulating GaAs substrates, comparing with Si-based MOSFET
      - Rich band gap engineering in compound semiconductors
    - low power consumption and circuit simplicity of CMOS, comparing with GaAs MESFET, HEMT
  - **Applications**
    - new generation of digital GaAs IC's of high speed and low power for communication and computer industries
- Other electronic applications
  - High power devices in MESFET, HEMT, and high speed devices in HBT
- Laser facet coatings and other photonic applications

Inventions at Bell Labs toward GaAs MOSFET's

- 1994
  - novel oxide $Ga_2O_3(Gd_2O_3)$ to effectively passivate GaAs surfaces
  - demonstration of low interfacial recombination velocities using PL
- 1995
  - establishment of accumulation and inversion in p- and n-channels in $Ga_2O_3(Gd_2O_3)$-GaAs MOS diodes with a low D_{it} of 2-3 x 10^{10} cm^{-2} eV^{-1}(IEDM)
- 1996
  - first e-mode GaAs MOSFETs in p- and n-channels with inversion (IEDM)
  - Thermodynamically stable
- 1997
  - e-mode inversion-channel n-InGaAs MOSFET with g_m= 190 mS/mm, and mobility of 470 cm^2/Vs (DRC, EDL)
- 1998
  - d-mode GaAs MOSFETs with negligible drain current drift and hysteresis (IEDM)
  - e-mode GaAs MOSFETs with improved drain current (over 100 times)
  - Dense, uniform microstructures; smooth, atomically sharp interface; low leakage currents
- 1999
  - GaAs power MOSFET
  - Single-crystal, single-domain Gd_2O_3 epitaxially grown on GaAs
- 2000
  - demonstration of GaAs CMOS inverter
- 2001-2002
  - Design of high-speed and high-power devices; reliability of devices

ULTRAHIGH VACUUM DEPOSITION OF OXIDES

Initial thinking: to attain Ga_2O_3 film for passivation

High-purity single crystal $Ga_5Gd_3O_{12}$ (GGG) source

Evaporation (sublime) by e-beam

Gd_2O_3 ionic oxide
T_m > 4000K

Ga_2O_3 more covalent oxide
T_m ~ 2000K

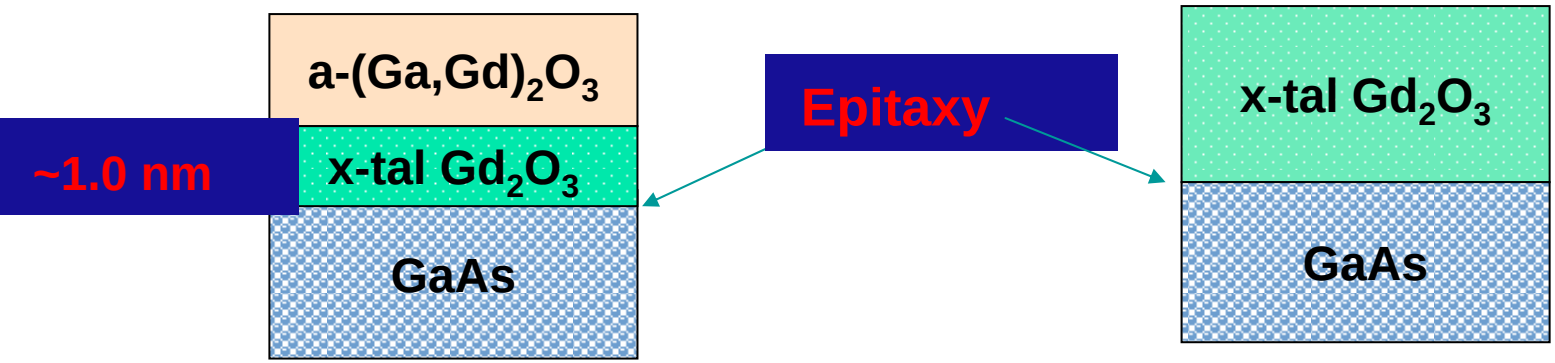
Ga_2O_3 evaporated mostly, and formed amorphous Ga_2O_3 film

Mixed Oxide $(Ga,Gd)_2O_x$

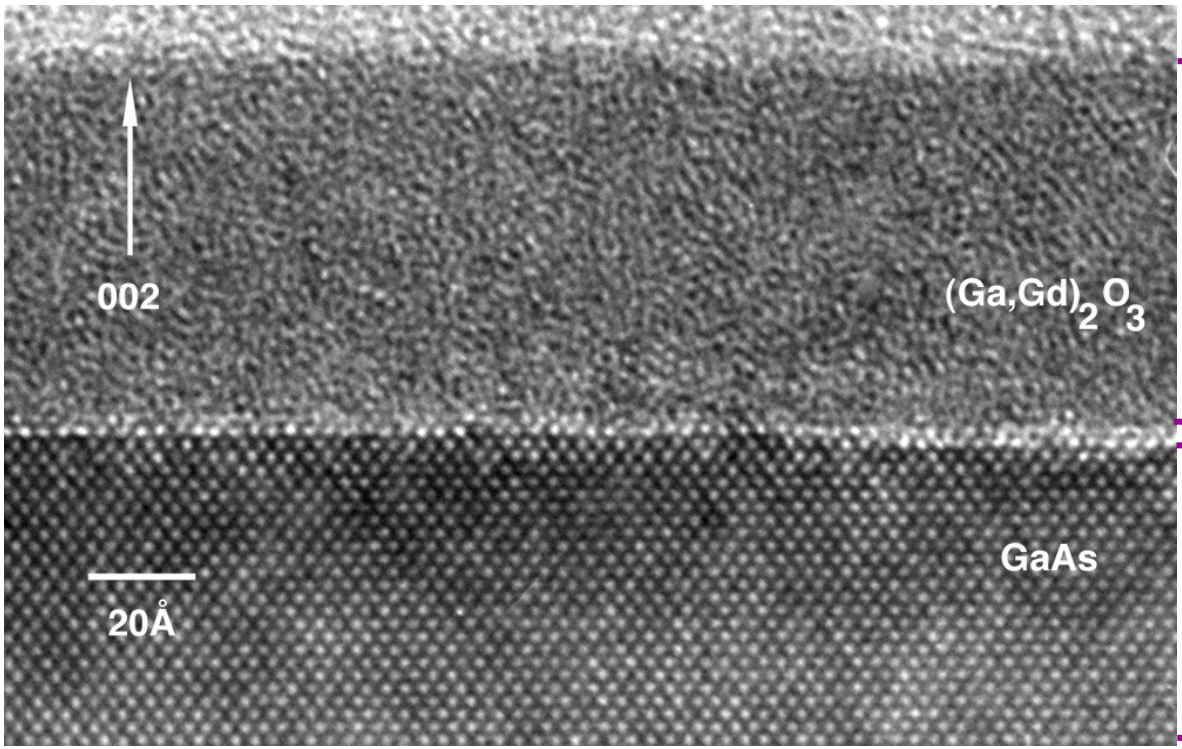
Gd/(Ga+Gd) > 20%
Gd^{+3} stabilize Ga^{+3}

Pure Gd_2O_3 Film

Single domain, epitaxial film in (110) Mn_2O_3 structure



High Resolution TEM of $Ga_2O_3(Gd_2O_3)$ on GaAs



Amorphous region

Some crystalline phase at interface

Single crystal GaAs

Single Domain Growth of (110) Gd_2O_3 Films on (100) GaAs

M. Hong et al, Science 283, pp.1897-1900, 1999

Mn_2O_3 Structure

Gd_2O_3 a= 10.81Å

(110)

[1 $\bar{1}$0]

[001]

3: 4 match

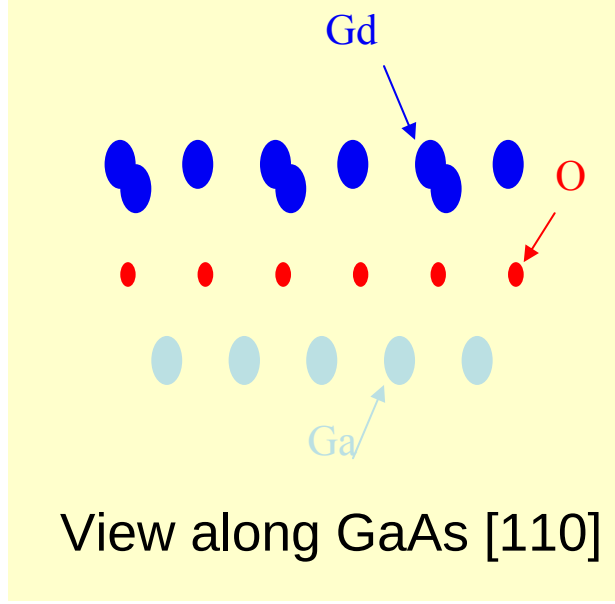
1: 2 match

GaAs a=5.65Å

(100)

[1 $\bar{1}$0]

[110]



View along GaAs [110]

Gd_2O_3 (110) 25Å

[001] [$\bar{1}$ 10] [$\bar{1}$ 11]

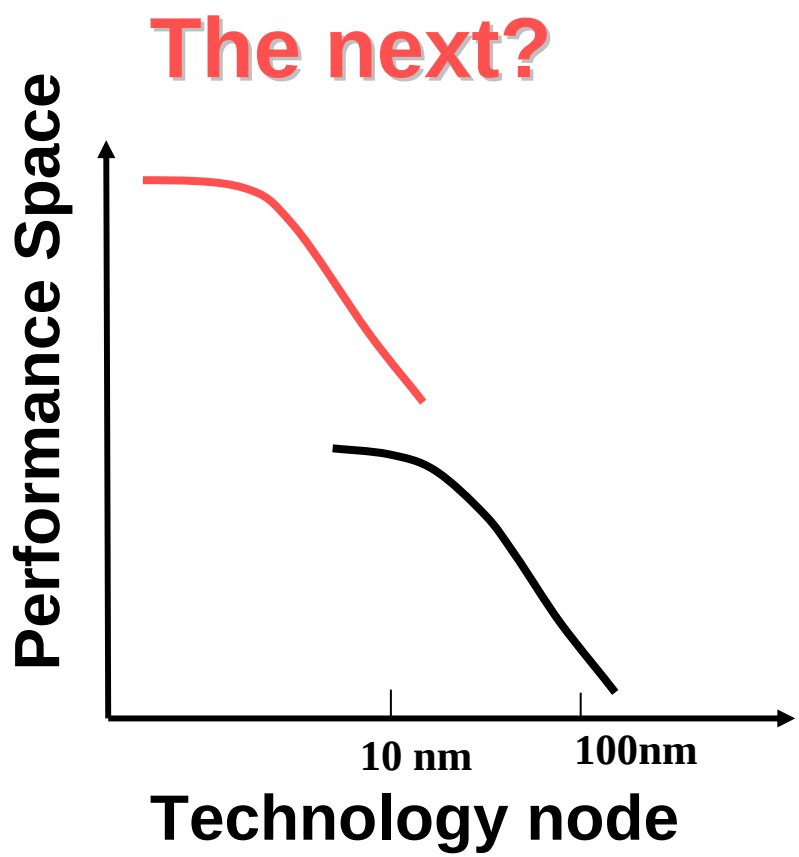
Single crystal Gd_2O_3 on GaAs - Epitaxial interfacial structure

Not a Mn_2O_3 structure at interface
Stacking sequence similar to that of GaAs

- Nature – Materials 2002 Oct issue cover paper
- "New Phase Formation of Gd_2O_3 films on GaAs (100)", J. Vac. Sci. Technol. B 19(4), p. 1434, 2001.
- " Direct atomic structure determination of epitaxially grown films: Gd_2O_3 on GaAs(100) " PRB 66, 205311, 2002 (12 pages)
- A new X-ray method for the direct determination of epitaxial structures, coherent Bragg rod analysis (COBRA)

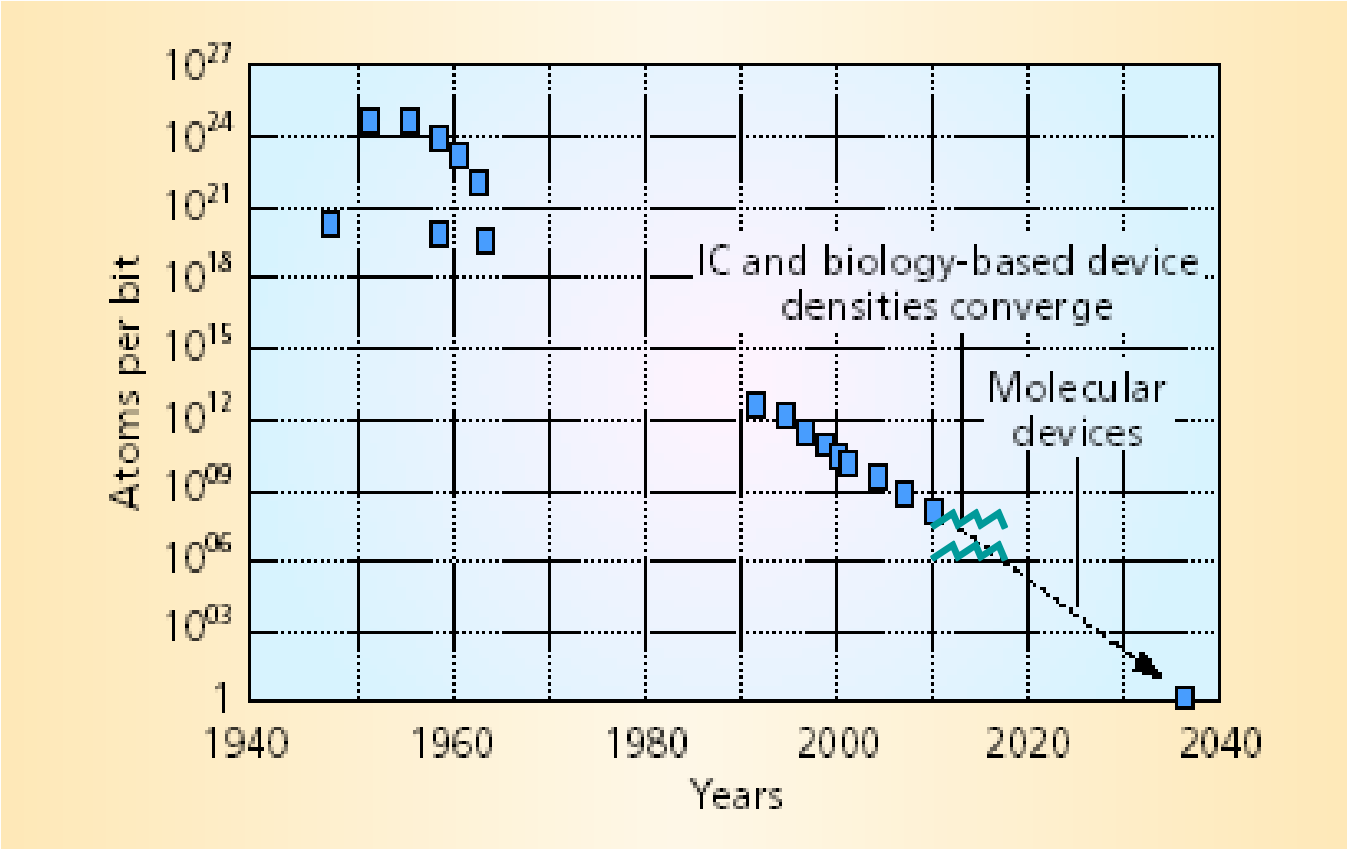
Grand Challenge in Nanoelectronics

- **1968-2003 (G. Moore, ISSCC 2003)**
  - **Transistors increases to 10^8-10^9 transistors/chip**
  - **Price per transistor decreases 7 orders of magnitude**
  - **Power decreases 7 orders of magnitude**
  - **Volume decreases 6-7 orders of magnitude**
  - **"Moore's second law"– increasing cost of manufacture -- Self assembly**



V. V. Zhirnov, D.J.C. Herr: New Frontiers: Self-Assembly and Nanoelectronics. IEEE Computer 34(1): 34-43 (2001)

Storage approaching atomic limit



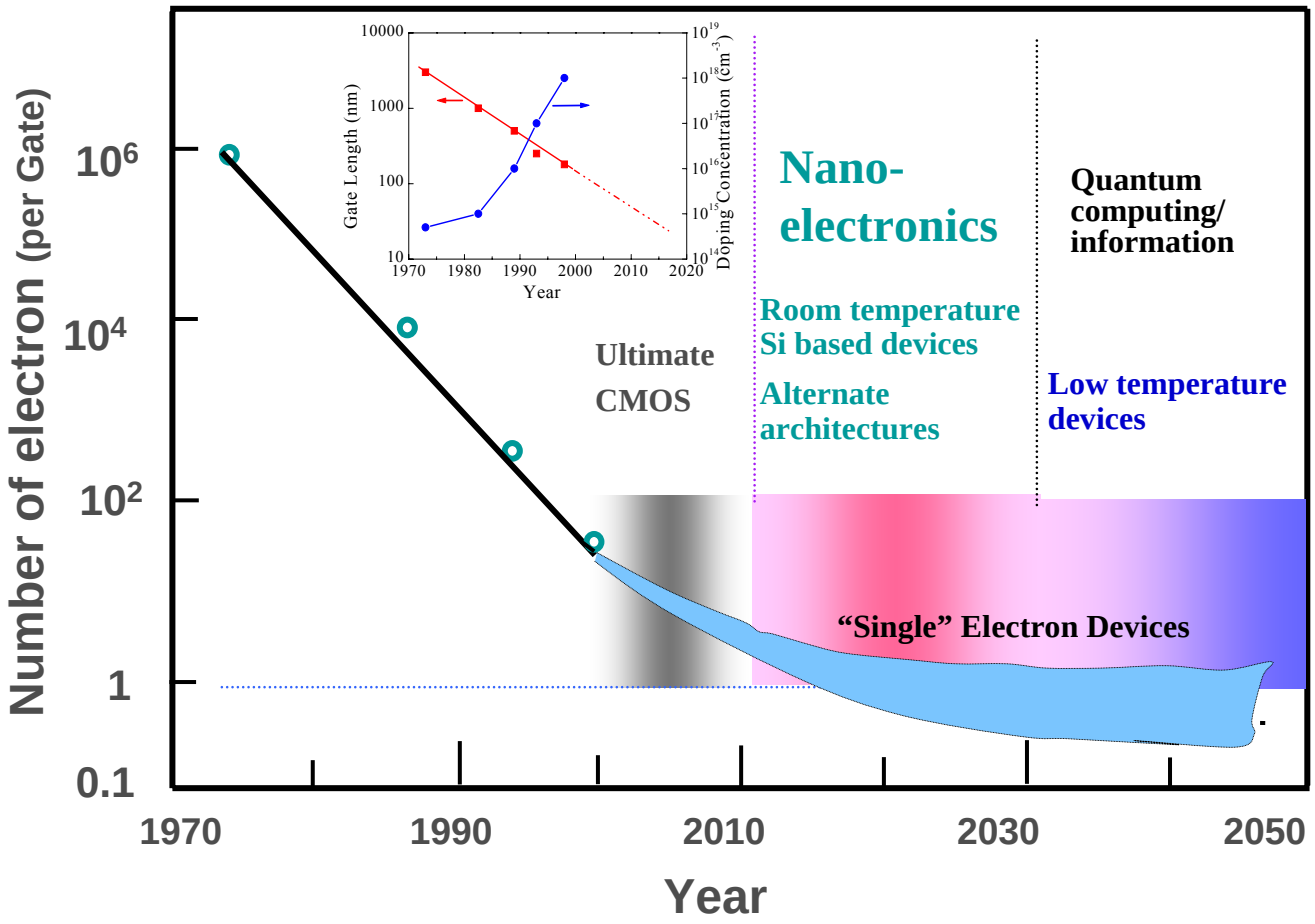
- **Atomic limits**
- **What else can be done?**
- **Associate memory**

V. Zhirnov and D. Herr, Computer, 2001

Nanoelectronics -- Next Generations

Major Issues

- Fewer electrons
- Massive number of interconnects
- Power consumption



Single electron detection made

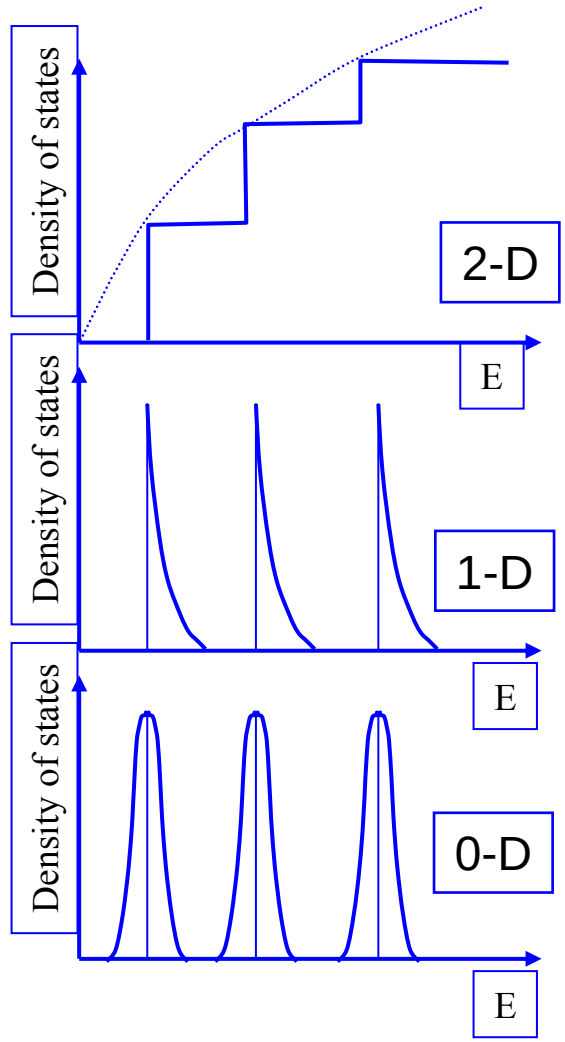
From materials to single electron, spin, etc.

New Materials

- Strained layers (Si and Ge):
  - Changing band structure
  - Increasing mobility

Quantum confinement

- **ID: nanowires**
  - Carbon nanotubes
  - Reducing **phase space for scattering**
  - Density of states
- **0 D quantum dots**
  - Density of states
- **Single atom Devices**
- **Single Spin**
- **Quantum Coherence Phenomena, Devices (and Systems)**
- **Molecular Devices**

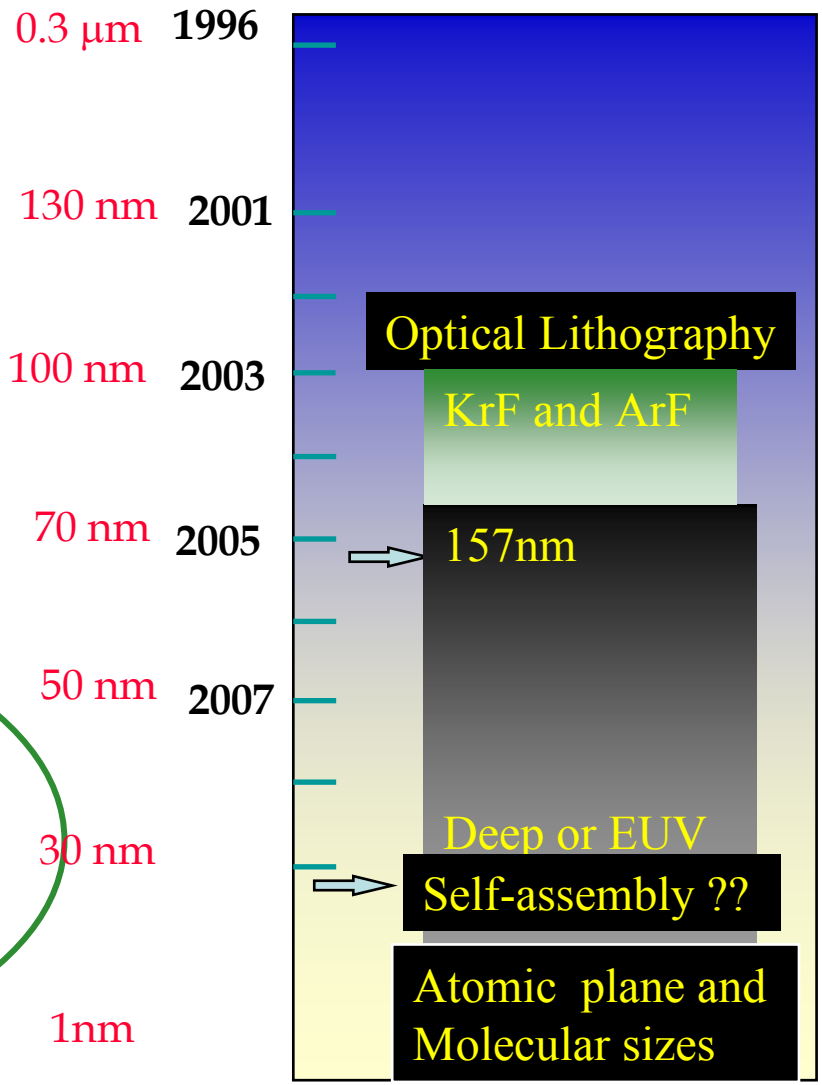


Processing: Fabrication of Nanostructures

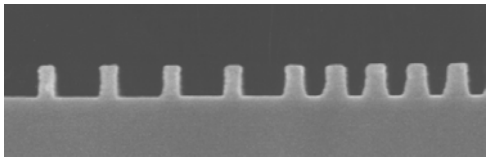
- Conventional techniques (High Throughput)
  - Deep Vacuum uv (13 nm)
  - Immersion lens systems
  - X-ray (200 nm to nm)
  - Projection ebeam
  - Other innovative processes
- low throughput
  - E beam or Nanoprobes

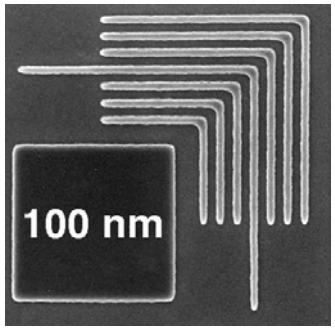
Registration

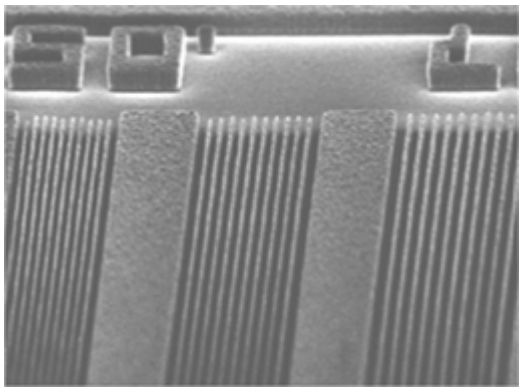
- Template -- Nanostamping
- Self assembly
- Molecular and atomic manipulation or bio engineering



Is EUVL the path to the Future??







¢¢¢¢¢¢!!!

Amazing Chemistry!!

Great Progress but,

$$$$$$$$$$$$$$

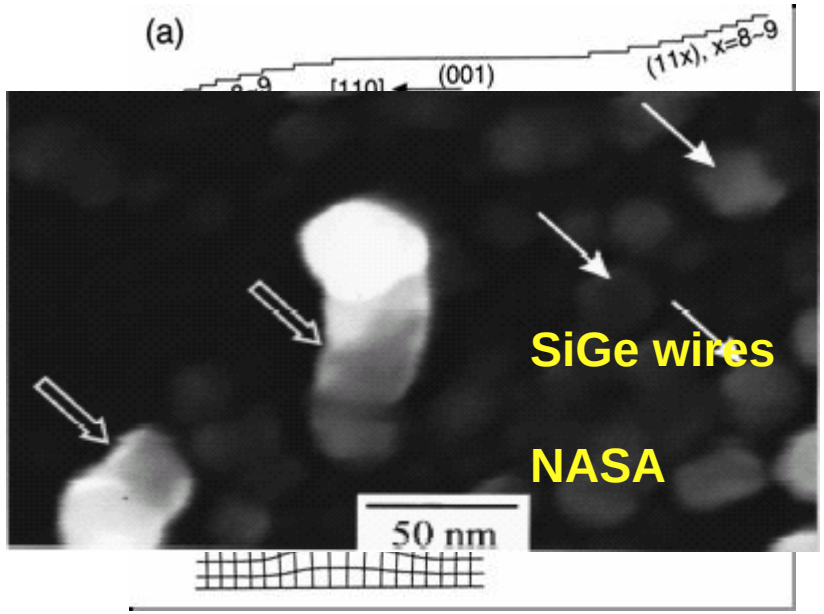
Methods for Self-assembly

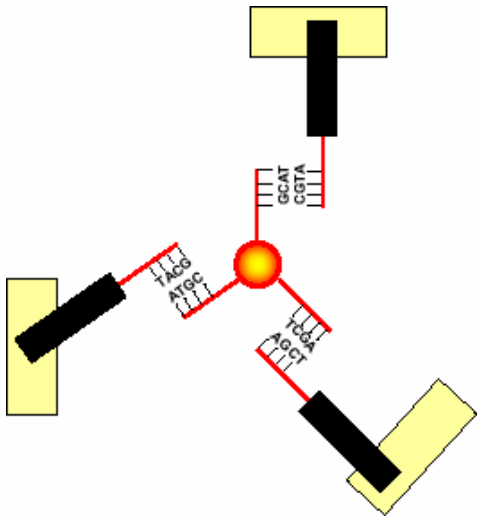
- **Physical self assembly**
  - **MBE, GSMBE, CVD, etc.**
  - Templates: Electrochemical, mechanical, Sol gel, etc.
- **Chemical self assembly**
  - Molecular self assembly, polymer self assembly, protein, DNA, bio-molecular, etc.
  - Colloidal self assembly
- **Bio self assembly**
  - **biochem**
  - **Protein and Virus engineering**
- **User defined surface dip pen**

- **Key Issues:** **Uniform size**
  Controlled placement
- **Directed processes**
  - **Physical mechanisms, Chemical Mechanisms, and Biochemical Processes**

Mechanisms and Principles

- **Physical self assembly**
  - **Mechanical Field – templating, strain, etc.**
  - Use of structured strain
  - Electrical and magnetic (including photon) fields
  - Surface energy – catalyst seeding
- **User defined surface dip pen**
- **Chemical and Bio chemical self assembly**
  - Chemical bonding
  - Conjugating - e.g., triple conjugation of QDs will be achieved at the Y-Junction, while QDs are trapped at the junction



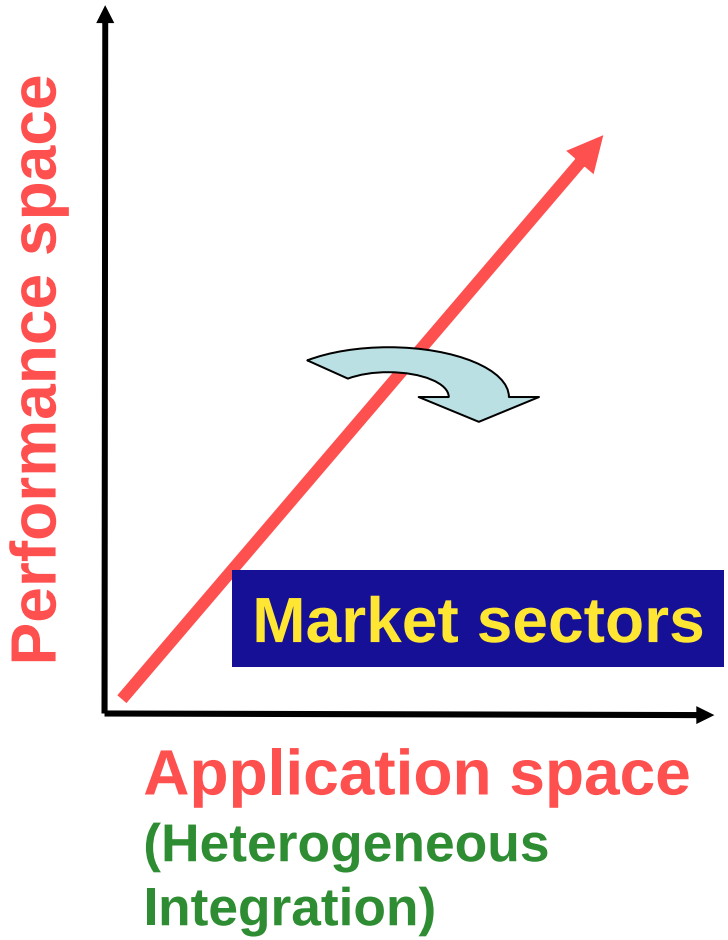


Next Logic Device

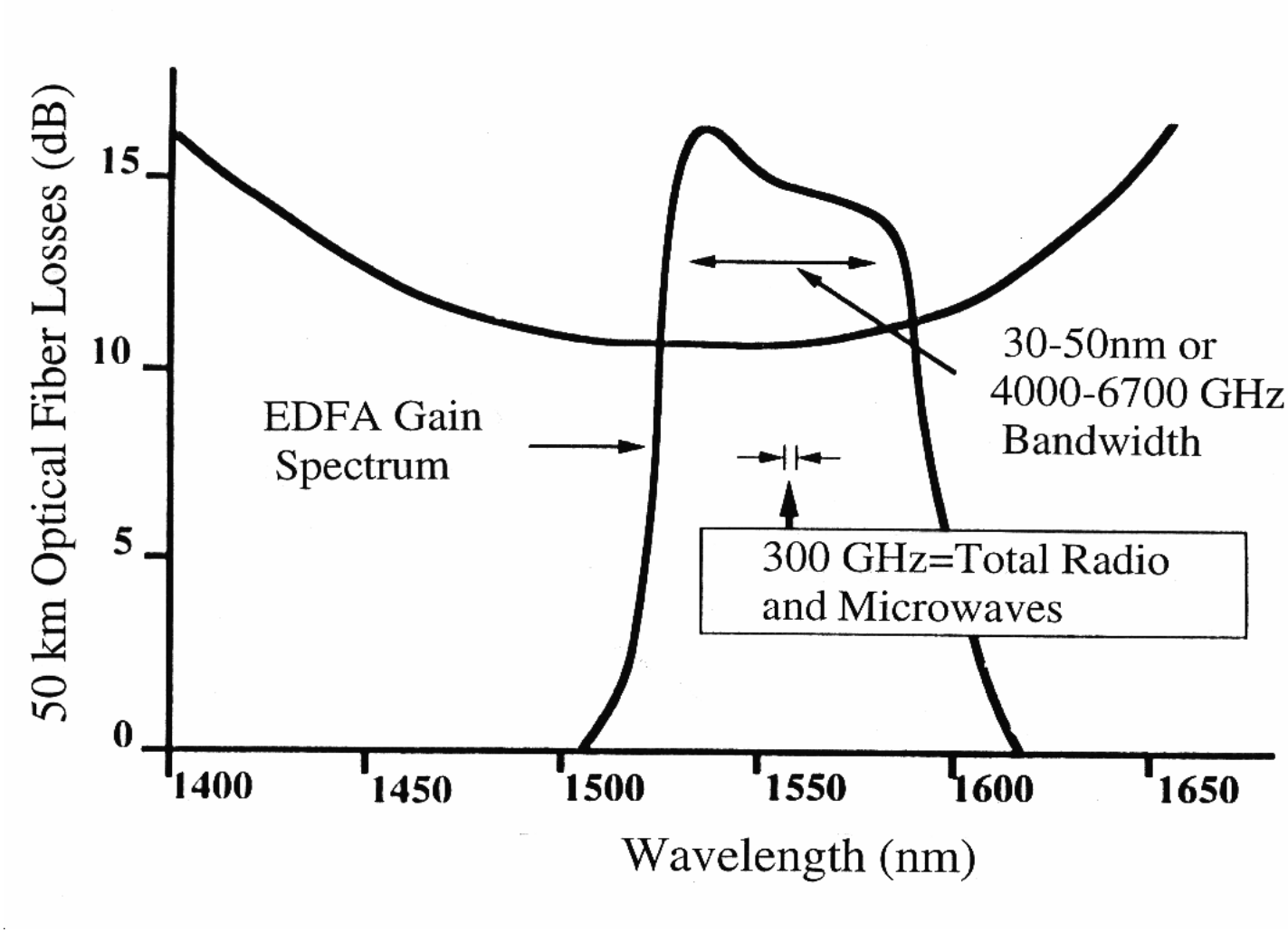
- **To develop Si- based nanoelectronics circuits and architectures**
  - **Needs**
    - **Low Power dissipation per function**
    - **Massively parallel**
    - **Minimize the interconnect**
    - **Low cost fabrication methods – self assembly**
  - **Nanoelectronics Architectures**
    - **Cellular automata-- combination of vertical MOS and single electron device, possibly optical device, etc.**
    - **Neural architecture**
    - **DNA architecture**
- **Interface from Micro to Nano circuits**
  - Develop enabling technologies to use Nano quantum and molecular devices – a few electron buffer amplifiers and circuits:
    approaching to single electron devices to interface to outside world

What else can be put on Si??
in Integrated Nanosystems

- **New nanoelectronics**
  - **Spin as a variable**
- **Ultimate CMOS and beyond**
- **Nano photonics**
- **Molecular devices**
- **Spintronics**
  - **Nanomagnetics**
  - **Coherent wave**
- **Nano bio devices**
- **Sensors and Fluidics; Nano-transducers**
- **Quantum coherence devices (and Systems)**



Our Motivation : Bandwidth Capacity of Optical Fiber



“Photonics” was invented at Bell Labs !

Ralf Menzel

Photonics

Linear and Nonlinear Interactions of Laser Light and Matter

To use laser light in this sense in science, technology and medicine, knowledge from different fields of physics, chemistry and engineering is necessary. Besides conventional optics, which is essential in all laser light applications, a large field of new physical phenomena has to be considered. This book assembles the necessary knowledge ranging from the basic principles of quantum physics to the methods describing light and its linear and nonlinear interactions with matter, to practical hints on how the different types of lasers and spectroscopic and other measuring techniques can be applied. So that the book remains handy and readable, the description focuses on newer concepts in a compressed form. Nevertheless, many examples, tables and figures allow direct access for answering practical questions.

In this book, nonlinear physical processes in which laser photons are used as a tool will be summarized under the term *photonics*. This term was introduced by engineers at the Bell Laboratories to describe the optical analogy of electronic devices in electronic communication technologies; here, photons are the information-carrying particles. But the word is used today to cover nonlinear optics and quantum optics, too.

Springer

Introduction

- **Optical fibers fabricated from silica glass have been the key component of the "*information age*",**

- **Silica has excellent material characteristics**

  Most stable glass formation, Most stable glass against reduction. Thermodynamically easiest to purify

- **Optical losses are at theoretical limit 0.2 dB/km, ideal long haul transmission medium.**

- **Silica fibers have immense data capacity (> 100 Terabit/sec)**

BUT

- Silica glass has high phonon-energy

  Not suitable for radiative transitions, active device applications

- Silica has low non-linearity

  Not suitable for switching device applications

Low-Phonon Energy Glasses for Fiber Devices

Many new low-phonon energy glasses are emerging with significantly superior properties

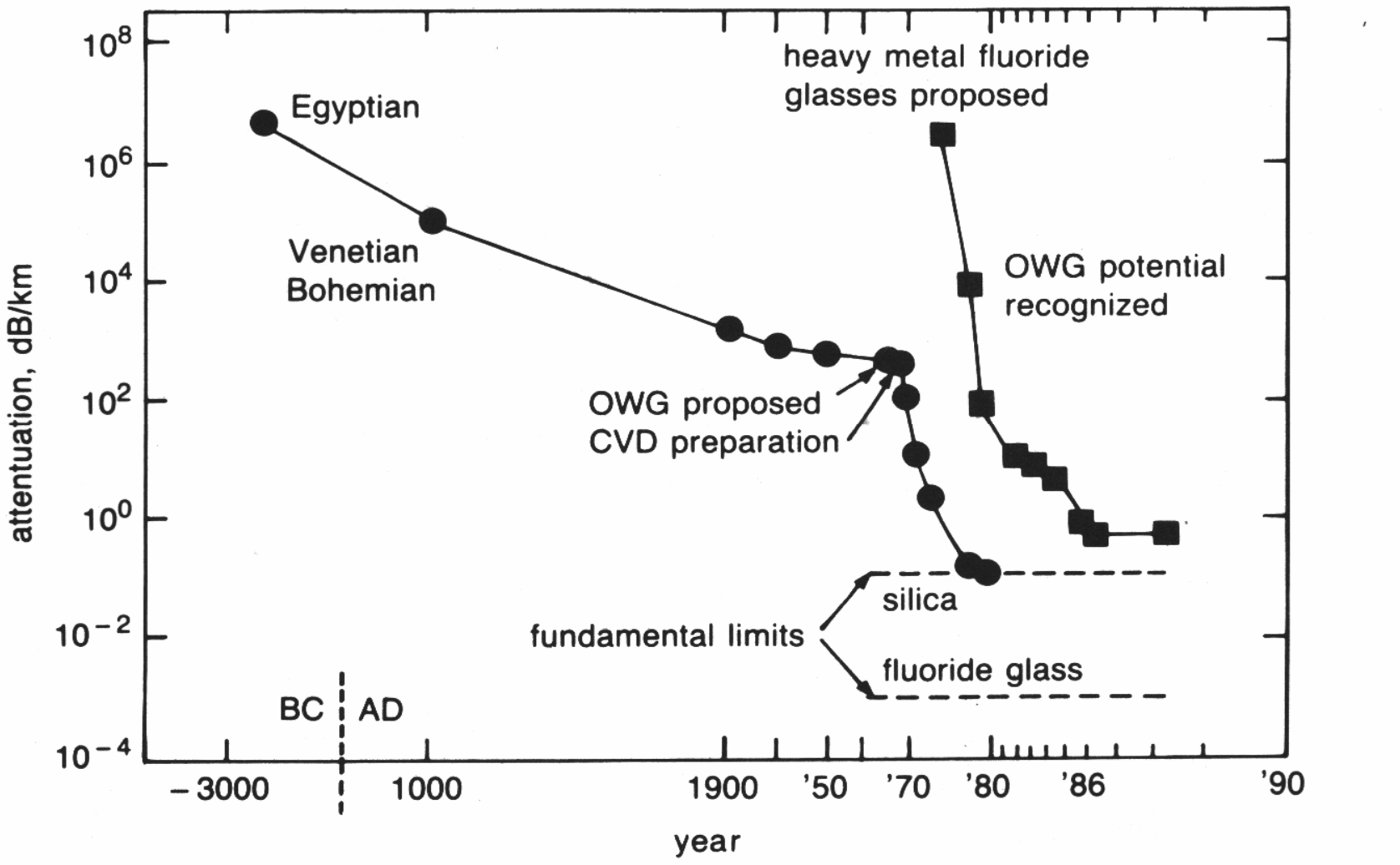
- Transparency up to 20 microns
- Kerr non-linearity can be up to 800 times of silica
- Efficient lasers at many new wavelengths
- Good optical amplifiers for many new bands
- Very-short device lengths possible

BUT

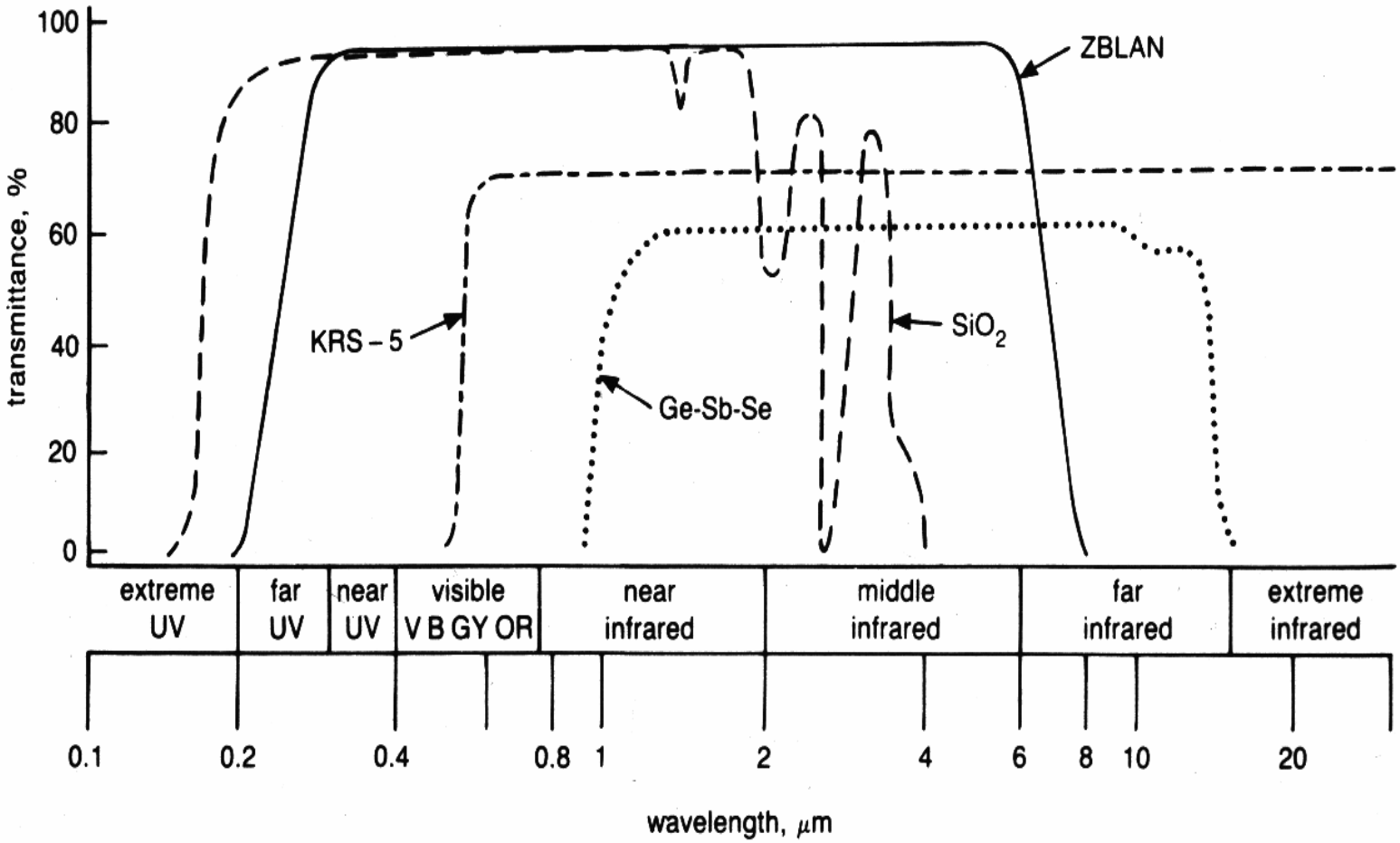
Transparencies of Glasses (0.1-2 dB/mt) are less than ideal

For device lengths < 10 meters, this is perfectly acceptable.

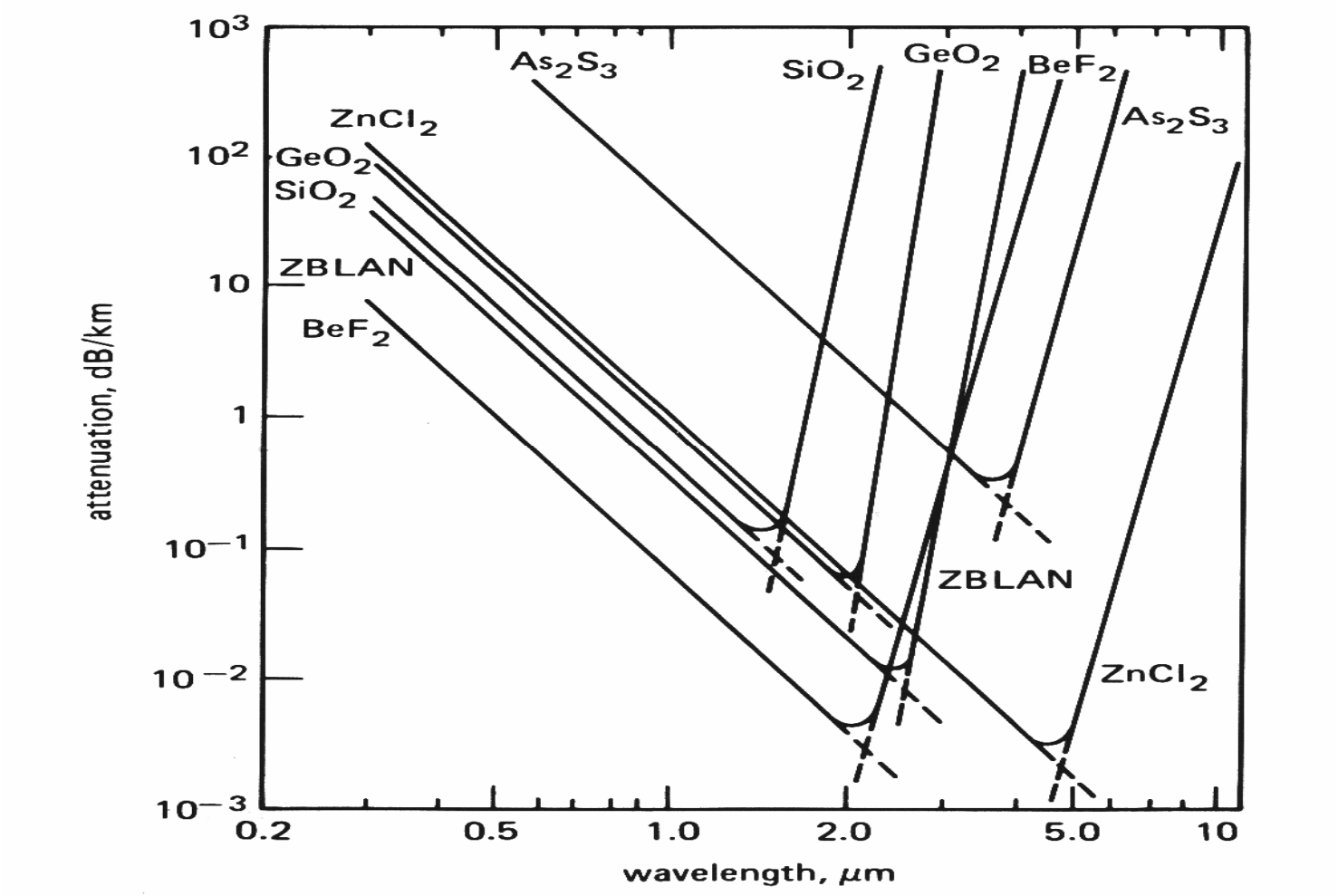
Transparency, historical



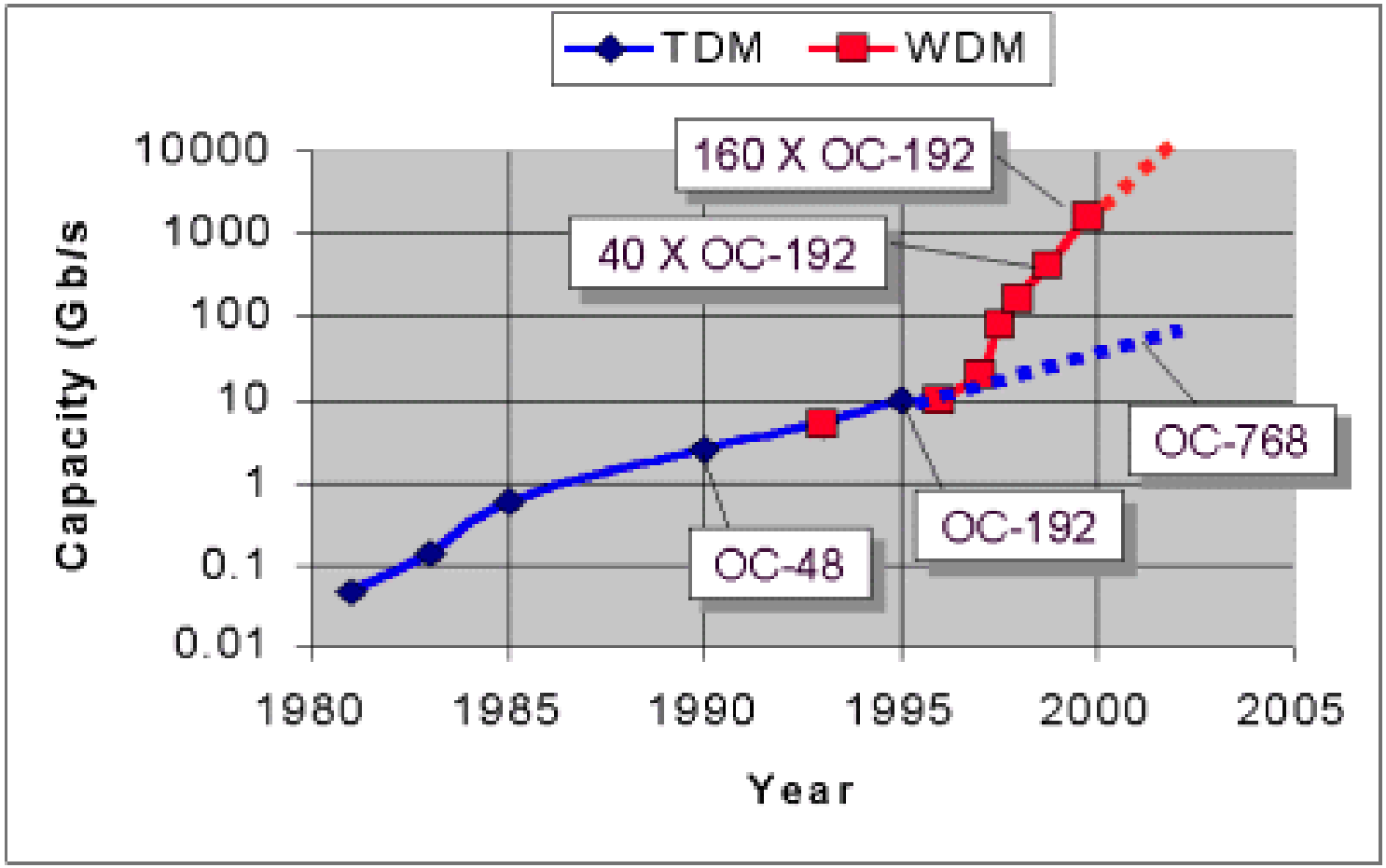
Transparency of Optical Materials



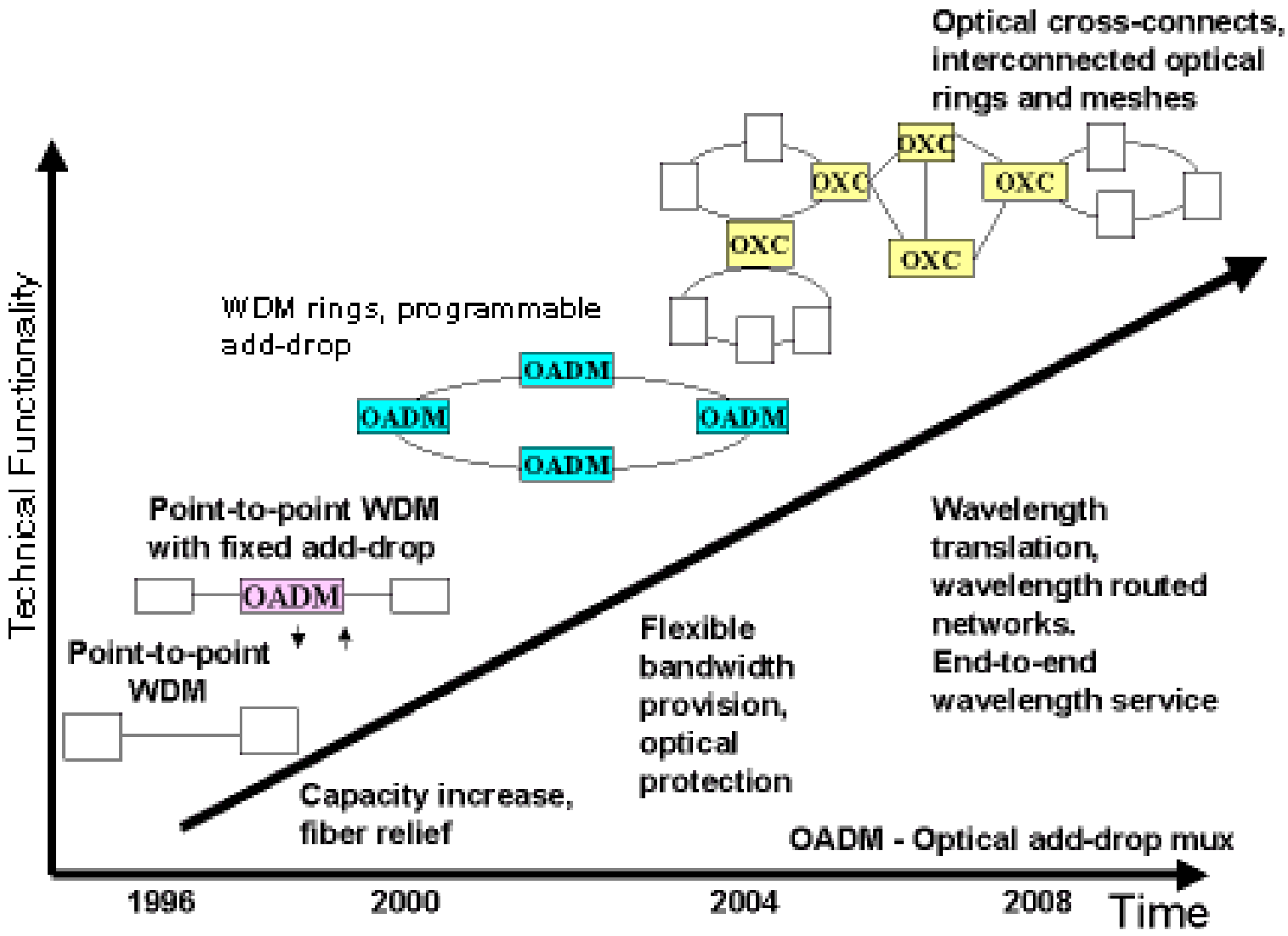
Intrinsic Optical Losses



Capacity : Historical



Evolution of Network Architecture



The Next Generation Lighting Technology - Semiconductor Lighting

Y.S. Liu

Opto-Electronics & Systems Laboratories (OES)

Industrial Technology Research Institute (ITRI)

Taiwan, ROC

YSLiu/Copy Right@ITRI

Semiconductor Lighting

- 發明
- 物理/科技
- 應用/生活
- 產業

YSLiu/Industry Forum/CLEO/PR2003 Copy Right@ITRI

ITRI OES

Major Milestones in Photonics

- *Invention of Light Bulbs (1882)*
  - *Beginning of man-made electrically-generated light*
- *Invention of Coherent Light (1960's)*
  - *Beginning of quantum optics (coherent, collimated ...)*
  - *Invention of transistors(1948)*
- *Nano-photonics (2000s)*
  - *Beginning of a new un-chartered territory e.g. Photonic crystals, QD devices, holey fibers*

光電技術的起源-1880s

光電科技的發展過程中、充滿了突破性技術的發明，因而給人類生活帶來革命性的改變！1882年愛迪生發明白熾燈、這是人類第一次用電產生的光源！這個發明不但是有史以來、人類第一次真正解脫了黑暗的約束、更開創了近代光電科技發展的首頁！

- 劉容生，“奈米科技”，2004

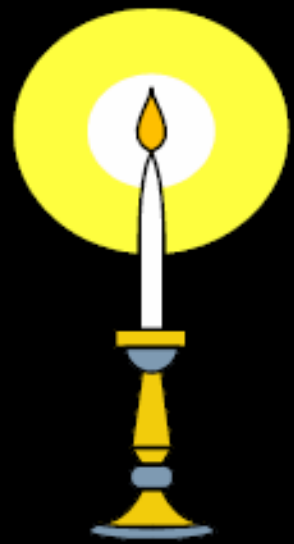
ITRI OES

Let There Be Light

- Genesis

BC- 1880's

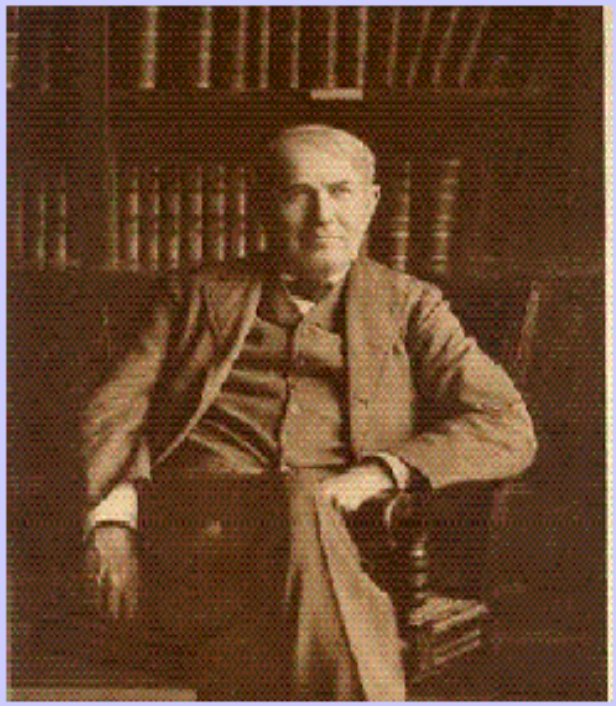
Light :



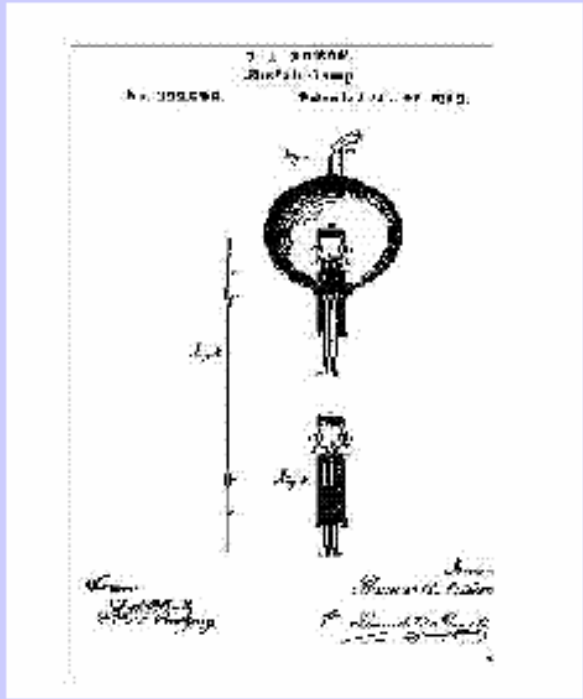
Edison's Lamp - 1882

" We are striking it big in the electric light, better than my vivid imagination first conceived. *Where this thing is going to stop Lord only knows.*"

- Thomas Edison October 1879

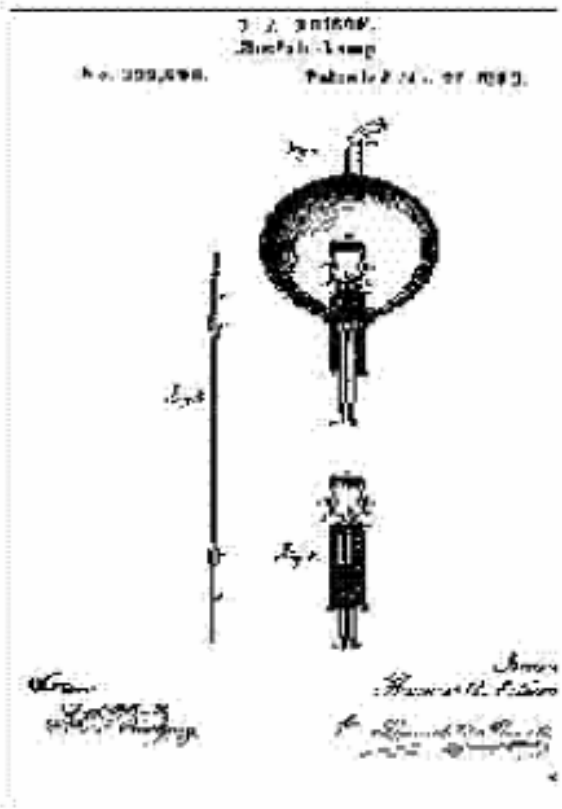


Thomas Edison, 1882



September 4, 1882

Edison's Incandescent Lamp - 1882



September 4, 1882

"The first step is an intuition- and comes with a burst, then difficulties arise. – This thing gives out and then that- 'Bugs' –as such little faults and difficulties are called- show themselves and months of anxious watching. Study and labor are required before commercial success or failure- is certainly reached…. I have the right principle and am on the right tracks, but time, hard ward, and some good luck are necessary too."

- Thomas Edison, describing his inventive process, 1878

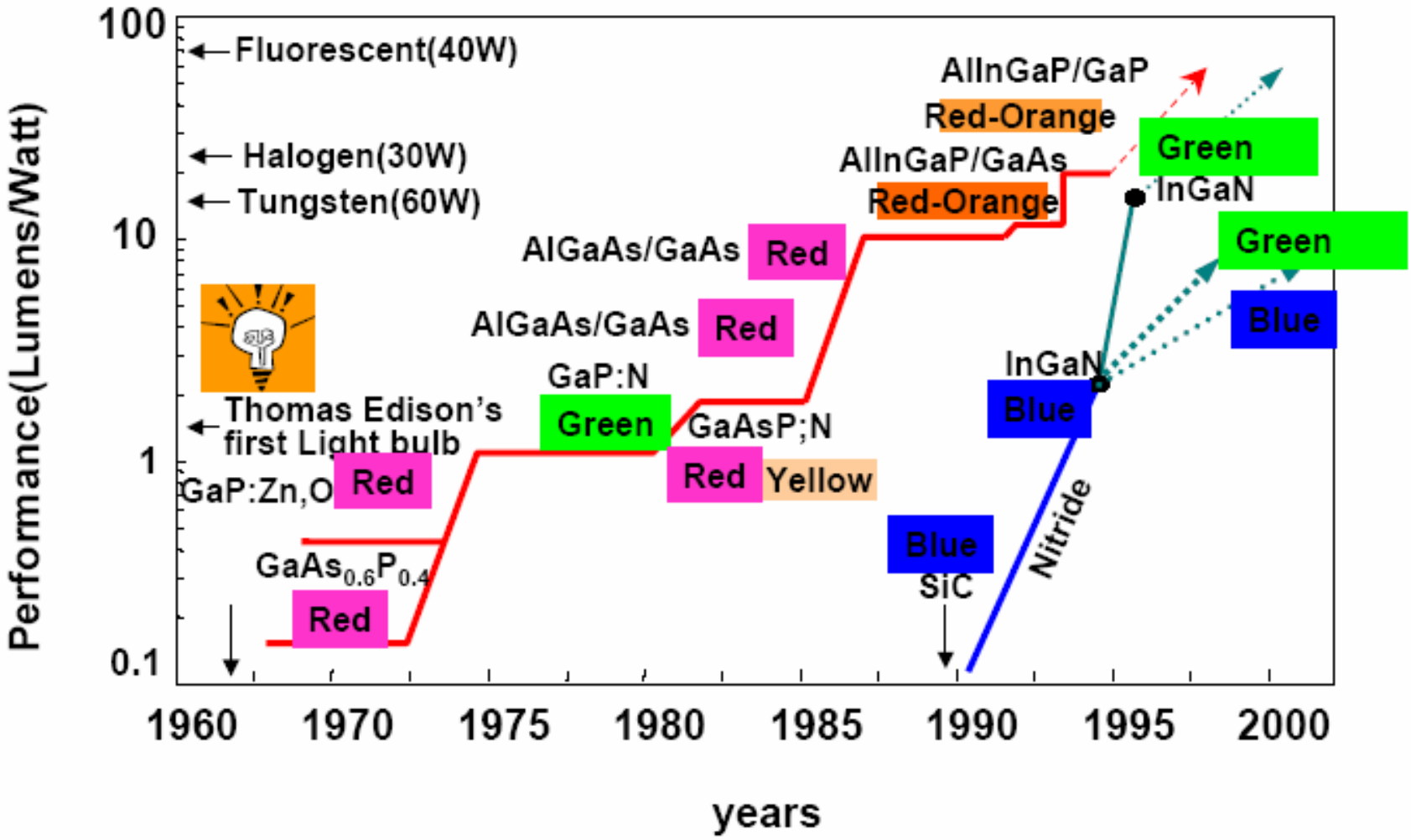
Beginning of Nano-technology - 1900s

1909年愛迪生創設的實驗室來了一位年輕的化學家Irving Langmuir、他繼續做燈炮相關問題的基礎研究、他發現如果把氮及氬氣加到燈炮裏可以大大增長燈炮的壽命! 他還發明了單分子層(mono-layer)的觀念及製作單分子層的工具、Langmuir的研究建立了表面物理科學的基礎、因而得到1932年的諾貝爾獎! 他的研究也可以說是奈米科技研究的開始! 從這些發展、我們可以看出光電科技和奈米科技密切的關聯性!

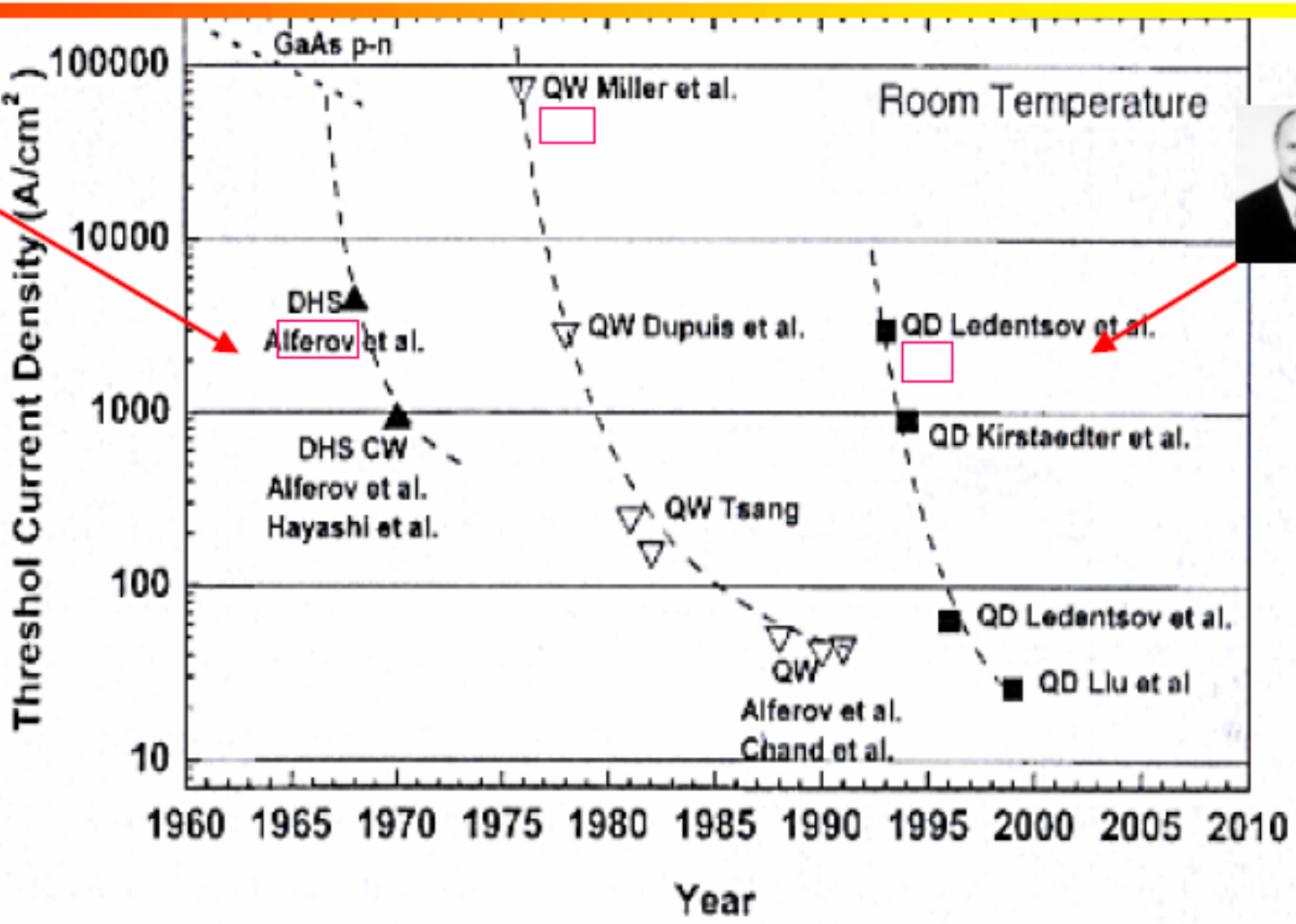
– 劉容生, "奈米科技", 2004

ITRI OES

Incandescence, fluorescence & LED Lights

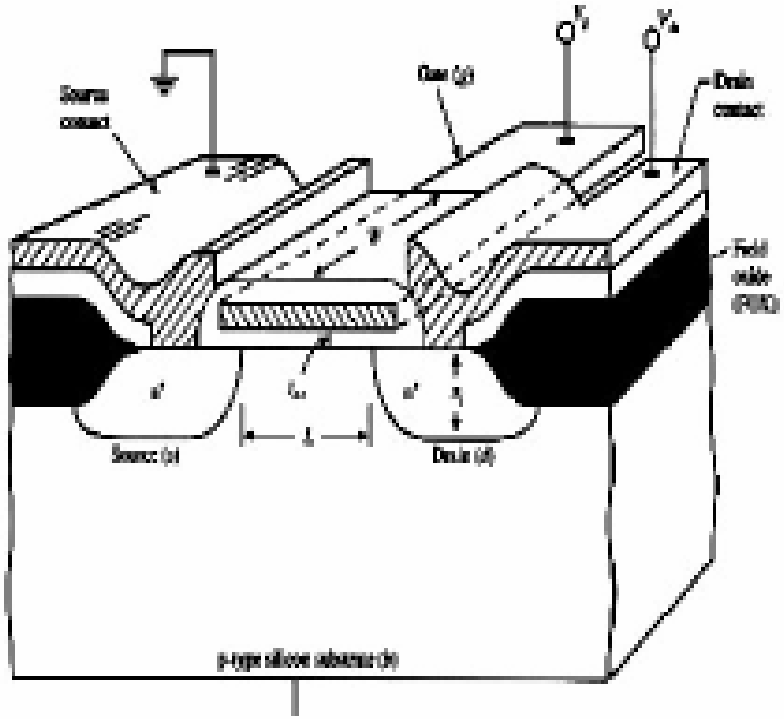


Evolution of Semiconductor Lasers



N. Ledentsov, IEEE J. Select. Topics Quantum Electron., 6, 439, 2000

Metal Oxide Semoconductor (MOS) Transistor



- Speed Increases with Charge Carrying Capacity, Q.

$$Q = CV$$

where $C = \varepsilon / d$ (ε: Dielectric constant; d: Oxide thickness)

- To Increase C:
  - Decrease d
  - Increase ε ($\varepsilon = k\,\varepsilon_0$)

⇒High-k dielectrics

Intel Press Release (11/5/2003) on the high κ gate dielectrics for 45 nm in year 2007.