2011 DRC Short Course

50 years of development of oxides on III-V. Is *in-situ* process the best choice?

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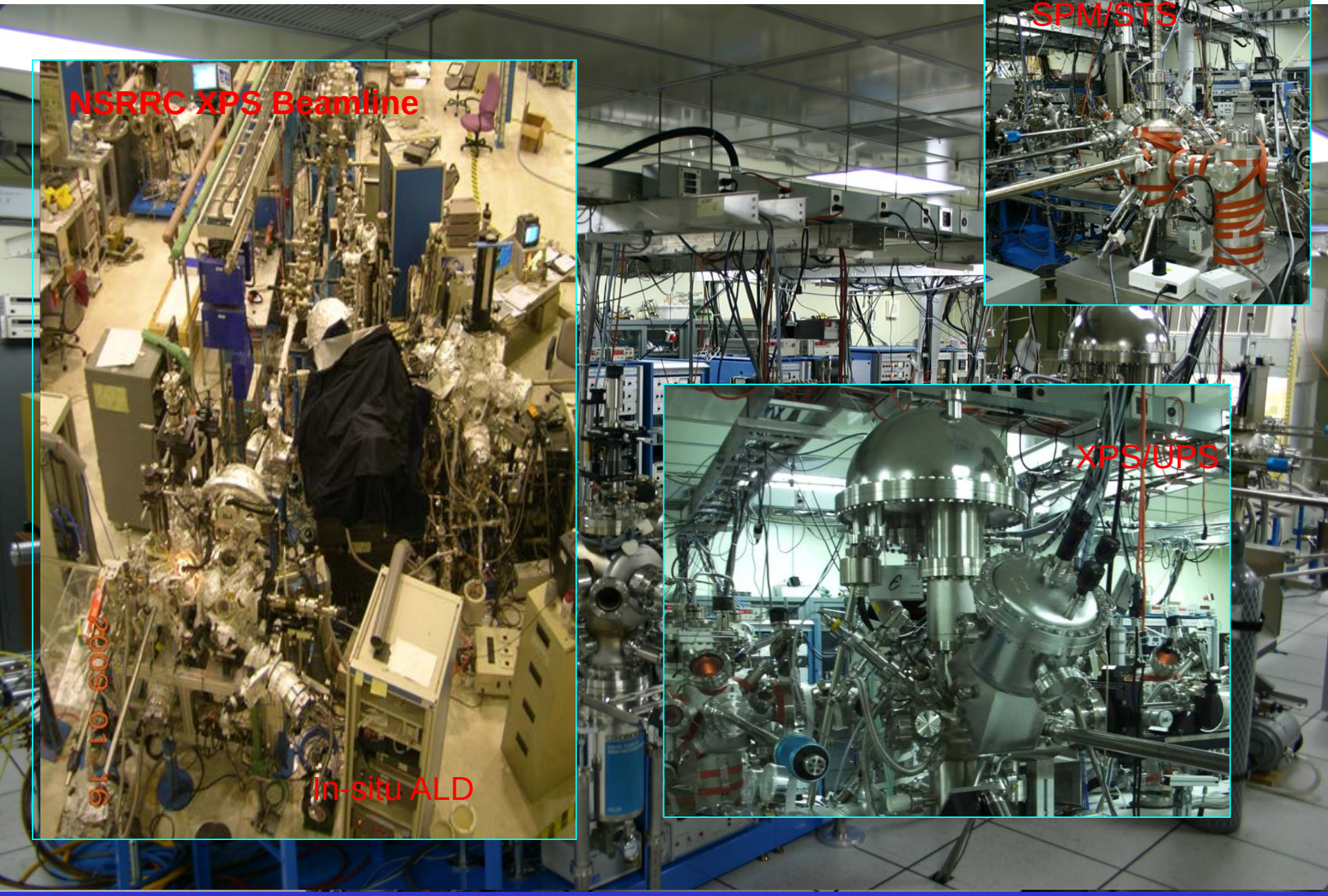

NSRRC XPS Beamline
SPM/STS
XPS/UPS
In-situ ALD

- MBE – *compound semiconductor growth* – A. Y. Cho (National Medal of Science 1993 and National Medal of Technology 2007)

- MBE – *metal and oxide growth* – J. Kwo (first in discovering anti-ferromagnetic coupling through non-magnetic layer in magnetic superlattices PRL's 1985 – 1986)

Frank Shu, UC University Professor and former President of Tsing Hua Univ.

Fundamental requirements for high κ's + metal gates on InGaAs (or any channels) for technology beyond Si CMOS

- ✓ EOT < 1 nm
- ✓ Interfacial density of states $D_{it} \leq 10^{11}$ cm^{-2} eV^{-1}
- ✓ Self-aligned process
  - High-temperature thermodynamic stability
- ✓ Low parasitic
  - Ohmic contacts and sheet resistance
- ✓ Integration with Si

GaAs passivation (efforts since 1960)

Previous ex-situ Efforts (see M. Hong, C. T. Liu, H. Reese, and J. Kwo, in *Encyclopedia of Electrical and Electronics Engineering, edited by J. G. Webster (Wiley, New York,* 1999), Vol. 19, pp. 87–100, and *Physics and Chemistry of III–V Compound Semiconductor Interfaces, edited* C. W. Wilmsen (Plenum, New York, 1985).

Anodic, thermal, and plasma oxidation of GaAs

Wet or dry GaAs surface cleaning followed by deposition of various dielectric materials

➢ **Previous *in-situ* Efforts**

Growth using single chamber

- AlGaAs doped with O or Cr, Cho and Cassey 1978
- native oxides or Al_2O_3 on GaAs during the same growth, i.e. introduction of oxygen in III-V MBE chamber, Ploog et al 1979
- ZnSe (a_0 of 5.67 Å and a direct energy gap of 2.7 eV) on GaAs, Yao et al, 1979
- Si on InGaAs or GaAs, IBM at Zurich 1990 (?) and Morkoc et al, 1996

❖ **Our Breakthrough Growth using two chambers**

- $Ga_2O_3(Gd_2O_3)$, Ga_2O_{3-x}, MgO, SiO_2, Al_2O_3 on GaAs using two growth chambers, Hong et al, 1994
- Have been applied to GaAs, InGaAs, GaN, and Si

Do we need a new methodology for GaAs passivation?

Green and Spicer, *Stanford Univ. :* JVST A11(4), 1061, 1993

Sulfur passivation –Sandroff et al, Bell Labs: APL51, 33, 1987
Sb passivation – Cao et al, Stanford: Surf. Sci. 206, 413, 1988

"A new methodology for passivating compound semiconductors is presented in which two over-layers are used. In this approach, the first layer defines the surface electronically and the second provides long term protection."

Is it possible to have InGaAs MOS and Ge MOS, similar to SiO_2/Si, to achieve a low D_{it}, a low J, thermal stability at high temp. (>850 and 500℃), without any interfacial passivation layers (IPLs)?

YES!!!

"MBE - enabling technology beyond Si CMOS", (invited talk) J. Kwo, M. Hong, et al, J. Crystal Growth 323 511 (2011).
"InGaAs and Ge MOSFETs with high k dielectrics" (invited talk), J. Kwo, M. Hong, et al, Microelectronic Engineering **88**, 336 (2011)

S, Sb, Si, Ge as IPLs for InGaAs MOS
GeON, GeO_2, Si as IPLs for Ge MOS

Pioneering work of GaAs and InGaAs MOSFET's using $Ga_2O_3(Gd_2O_3)$ at Bell Labs without 2 overlayers

- 1994
  - novel oxide $Ga_2O_3(Gd_2O_3)$ to effectively passivate GaAs surfaces
- 1995
  - establishment of accumulation and inversion in p- and n-channels in $Ga_2O_3(Gd_2O_3)$-GaAs MOS diodes with a low D_{it} of 2-3 x 10^{10} cm^{-2} eV^{-1}(IEDM)
- 1996
  - first e-mode GaAs MOSFETs in p- and n-channels with inversion (IEDM)
  - Thermodynamically stable
- 1997
  - e-mode inversion-channel n-InGaAs/InP MOSFET with g_m= 190 mS/mm, Id = 350 mA/mm, and mobility of 470 cm^2/Vs (DRC, EDL)
- 1998
  - d-mode GaAs MOSFETs with negligible drain current drift and hysteresis (IEDM)
  - e-mode GaAs MOSFETs with improved drain current (over 100 times)
  - Dense, uniform microstructures; smooth, atomically sharp interface; low leakage currents
- 1999
  - GaAs power MOSFET
  - Single-crystal, single-domain Gd_2O_3 epitaxially grown on GaAs
- 2000
  - demonstration of GaAs CMOS inverter

- "Use of Hybrid Reflectors to Achieve Low Thresholds in All MBE Grown Vertical Cavity Surface Emitting Laser Diodes", R. J. Fischer, K. Tai, **M. Hong**, and A. Y. Cho, IEEE IEDM, 861, Washington, D.C., Dec.3-6, 1989; J. Vac. Sci. Technol. B8, p.336, 1990.
- "Array Operation of GaAs/AlGaAs Vertical Cavity Surface Emitting Lasers", K. Tai, Y.H. Wang, J.D. Wynn, **M. Hong**, R. J. Fischer, J.P. Mannaerts, and A.Y. Cho, ***CLEO/IQEC'90***, Anaheim, Ca, May 21-25, 1990.
- "MBE Growth and Properties of Fe_3(Al,Si) on GaAs(100)", M. Hong, H. S. Chen, J. Kwo, A. R. Kortan, J. P. Mannaerts, B. E. Weir, and L. C. Feldman, J. Crystal Growth, V.111, 984, 1991.
- "Vertical Cavity Top-Surface Emitting Lasers with Thin Ag Mirrors and Hybrid Reflectors", M. Hong, L. W. Tu, J. Gamelin, Y. H. Wang, R. J. Fischer, E. F. Schubert, K. Tai, G. Hasnain, J. P. Mannaerts, B. E. Weir, J. D. Wynn, R. F. Kopf, G. J. Zydzik, and A. Y. Cho, J. Crystal Growth 111, 1071, 1991.
- "In-Situ Non-Alloyed Ohmic Contacts to p-GaAs", M. Hong, D. Vakhshoori, J. P. Mannaerts, F. A. Thiel, and J. D. Wynn, J. Vac. Sci. Technol. 12 (2), p.1047, 1994.
- "New Frontiers of Molecular Beam Epitaxy with In-Situ Processing", M. Hong, invited paper for the 1994 International MBE Conference and published in J. Crystal Growth V.150, pp.277-284, 1995.
- "X-Ray Scattering Studies of the Interfacial Structure of Au/GaAs", D. Y. Noh, Y. Hwu, H. K. Kim, and M. Hong, Phys. Rev. B51 (7), p.4441, 1995.

Background leading to unpin surface Fermi level in III-V compound semiconductors

- Late 1980s to early 1990s, problems in then AT&T's pump lasers (980 nm) for undersea optical fiber cable (trans-Atlantic)
- Semiconductor facet (HR, AR) coating
  - Reducing defects between InGaAs (GaAs) and coating dielectrics
- Passivation of the facets
- Electronic passivation much more stringent than optical passivation
  - (110) vs (100) of InGaAs (GaAs)

ULTRAHIGH VACUUM DEPOSITION OF OXIDES

M. Hong et al, JVST B14 2297 (1996); J. Kwo et al, APL 75 1116 (1999); M. Hong et al, APL 76 312 (2000)

Initial thinking: to attain Ga_2O_3 film for passivation

High-purity single crystal $Ga_5Gd_3O_{12}$ (GGG) source

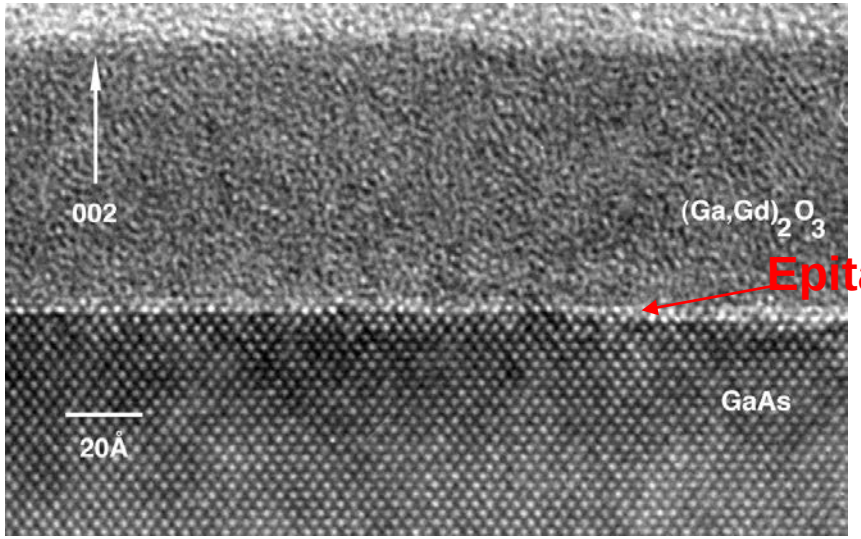
Evaporation (sublime) by e-beam

Gd_2O_3 ionic oxide
T_m > 4000K

Ga_2O_3 more covalent oxide
T_m ~ 2000K

Ga_2O_3 evaporated mostly, and formed amorphous Ga_2O_3 film

High Resolution TEM of $Ga_2O_3(Gd_2O_3)$ on GaAs

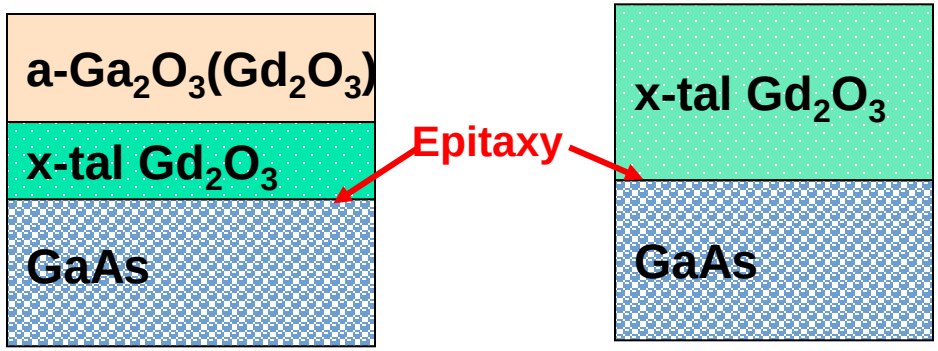


Mixed Oxide $Ga_2O_3(Gd_2O_3)$

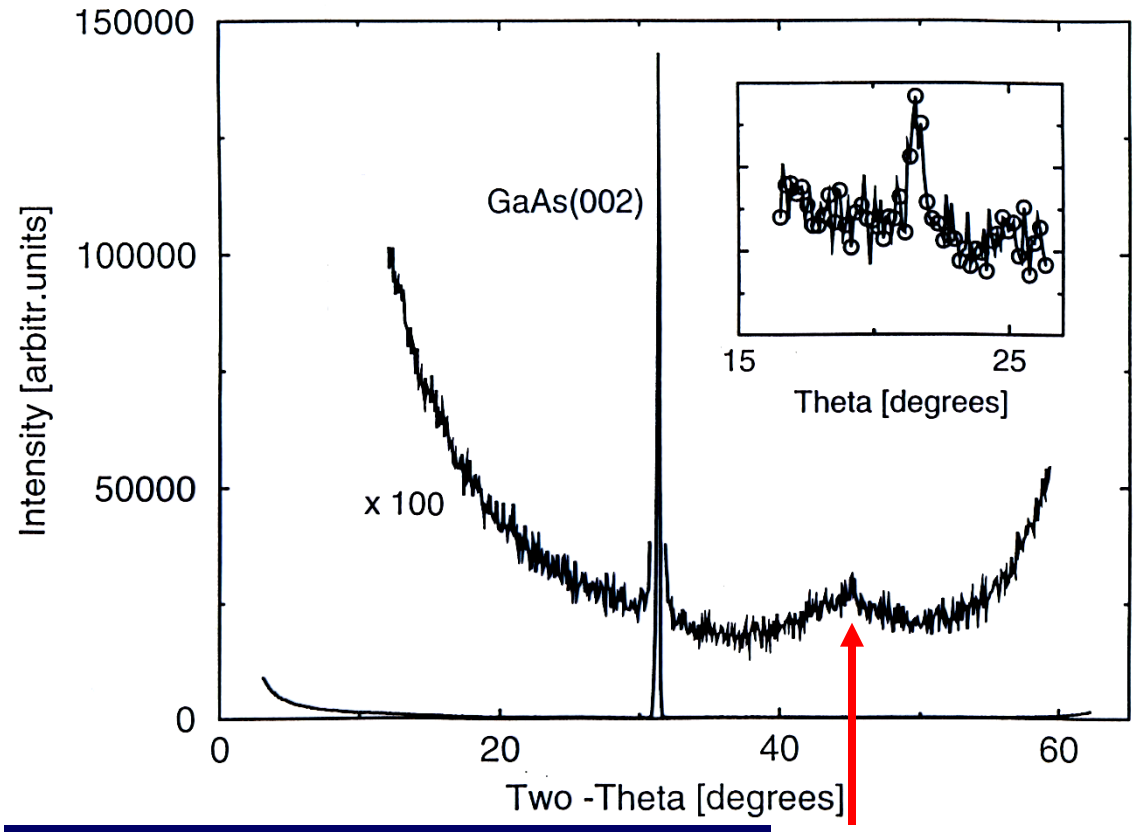
Gd/(Ga+Gd) > 20%
Gd^{+3} stabilize Ga^{+3}

Pure Gd_2O_3 Film

Single domain, epitaxial film in (110) Mn_2O_3 structure



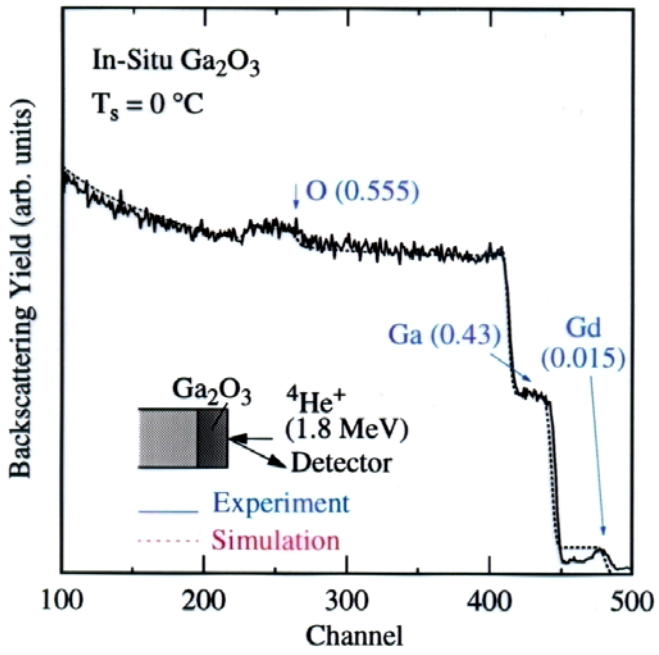
Initial growth of $Ga_2O_3(Gd_2O_3)$ 1.1 nm thick

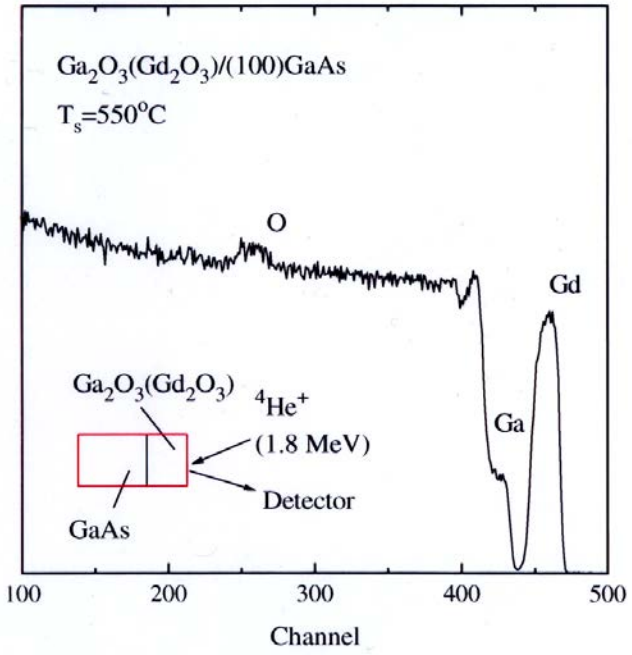


X-ray diffraction of normal scan and rocking curve

In-situ RHEED pattern showing a single crystal growth

Growth of $Ga_2O_3(Gd_2O_3)$ films using e-beam evaporation from $Ga_5Gd_3O_{12}$ target – RBS studies





Identified the essential role of Gd_2O_3 Kwo et al, APL 75 1116 (1999)

The Gd/(Ga+Gd) ratio needs to be greater than 20%

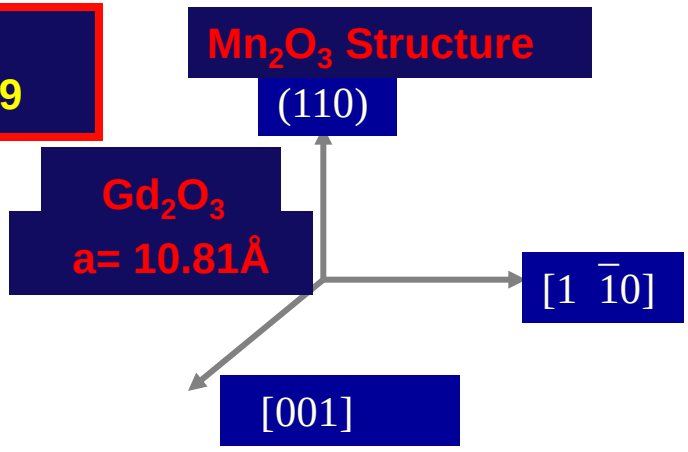
The electropositive Gd^{+3} may stabilize Ga^{+3} in the film

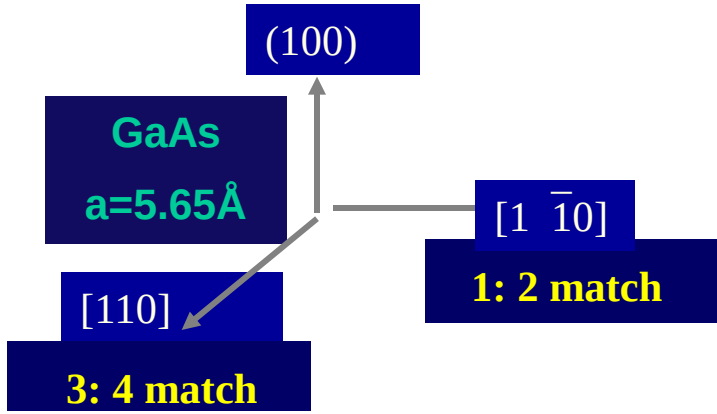
"Low D_{it} thermodynamically stable Ga_2O_3-GaAs interfaces: fabrication, characterization, and modeling", M. Passlack, M. Hong, J. P. Mannaerts, J. Kwo, R. L. Opila, S. N. G. Chu, N. Moriya, and F. Ren, IEEE TED, 44 No. 2, 214-225, 1997.

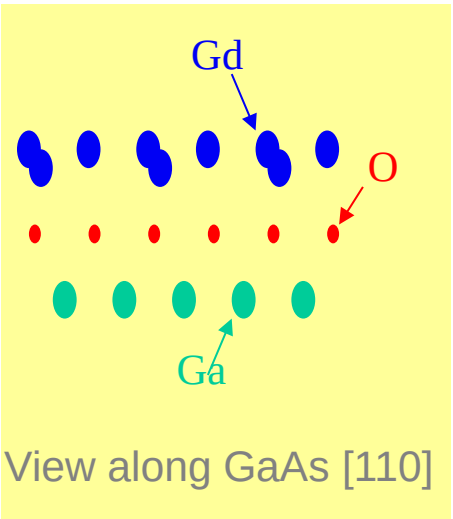
"Novel $Ga_2O_3(Gd_2O_3)$ passivation techniques to produce low D_{it} oxide-GaAs interfaces", M. Hong, J. P. Mannaerts, J. E. Bowers, J. Kwo, M. Passlack, W-Y. Hwang, and L. W. Tu, J. Crystal Growth, 175/176, pp.422-427, 1997.

Pioneer Work : Single Crystal Gd_2O_3 Films on GaAs

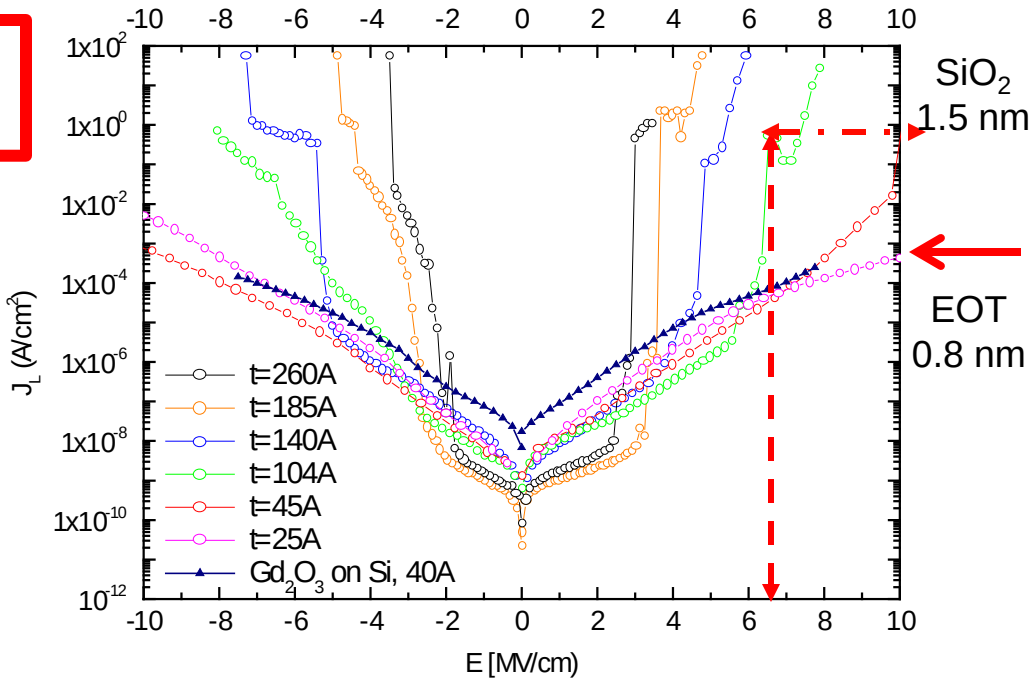
M. Hong, J. Kwo et al, Science 283, p.1897, 1999







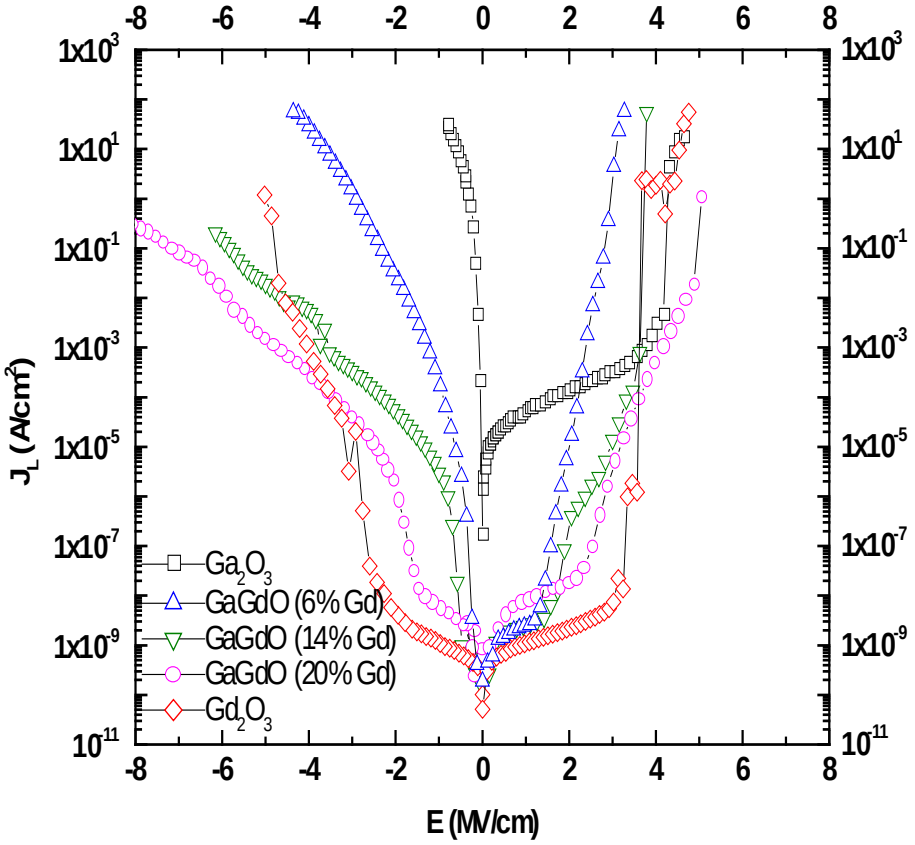
Low D_{it}'s and low J_L



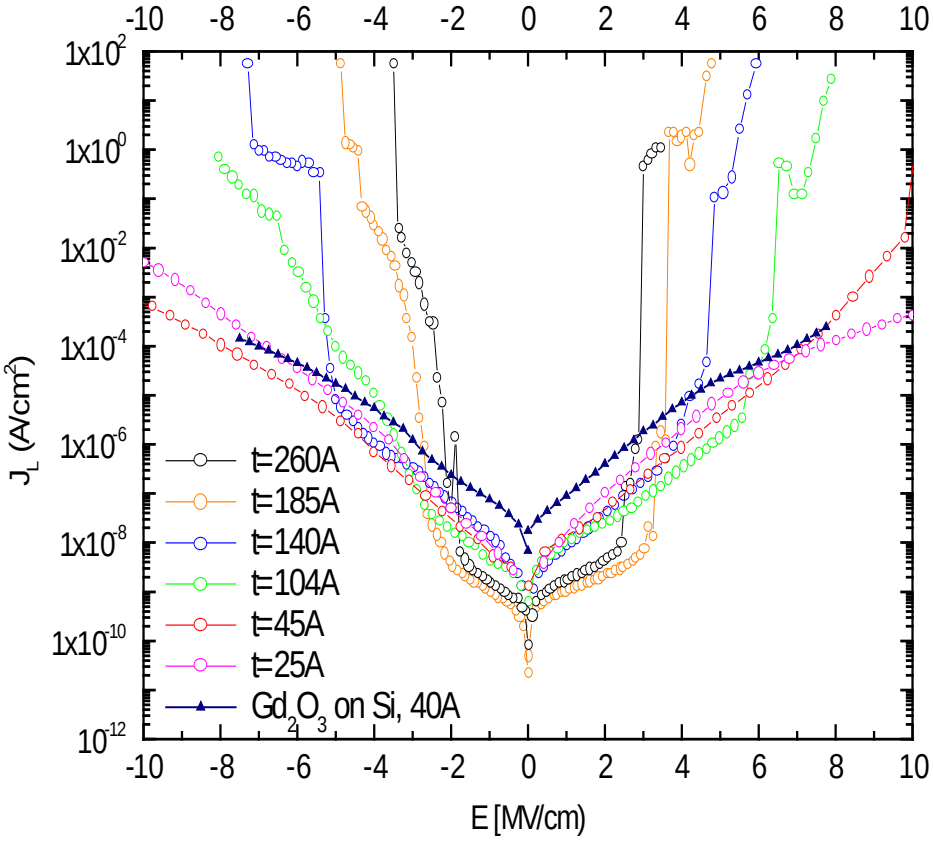
Gd_2O_3 (110) 25Å

J. Kwo et al, APL 75 1116 (1999)

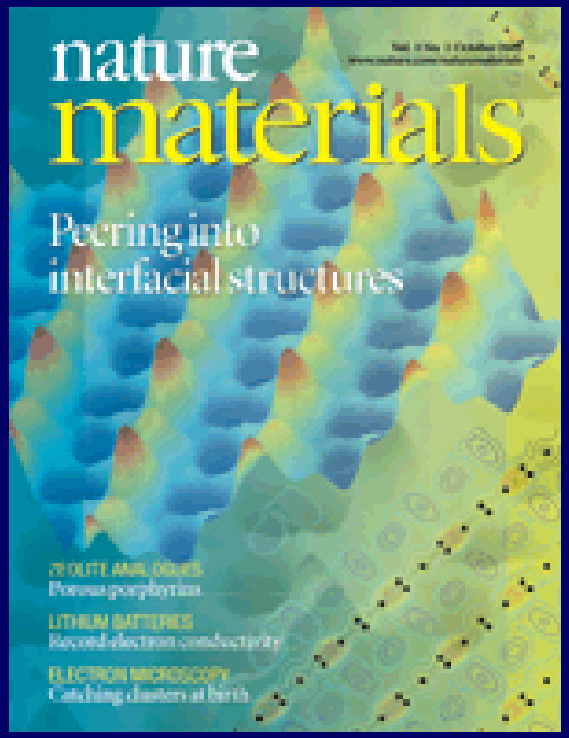
Gd Composition Dependence of Electrical leakage of GGG on GaAs



Thickness Dependence of Electrical Leakage of Gd_2O_3 on GaAs

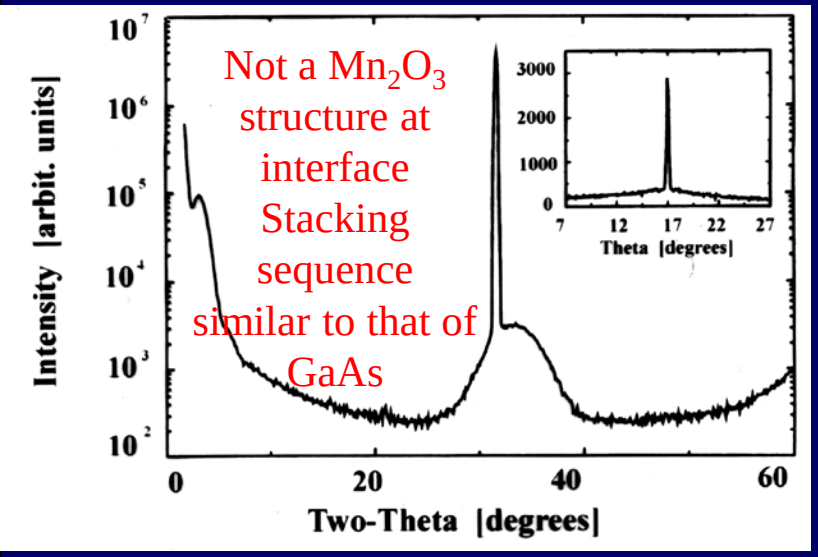


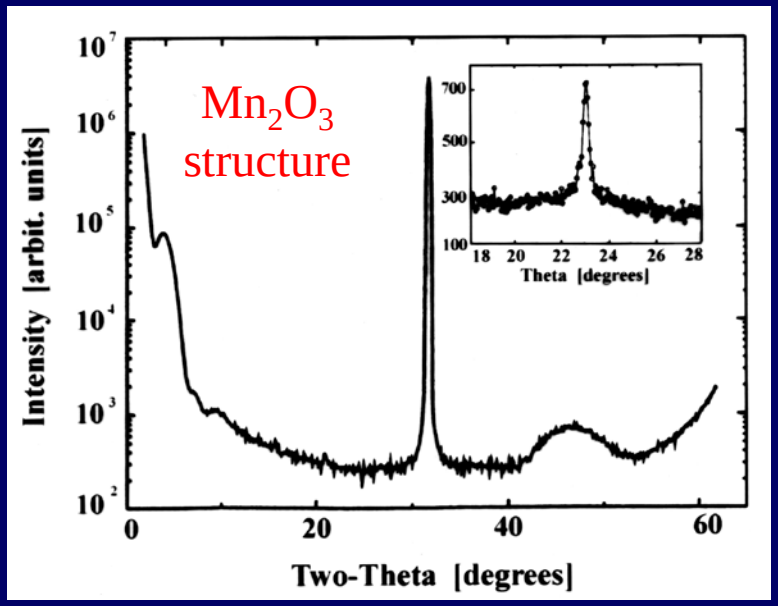
Single crystal Gd_2O_3 on GaAs - Epitaxial interfacial structure



- "New Phase Formation of Gd_2O_3 films on GaAs (100)", J. Vac. Sci. Technol. B 19(4), p. 1434, 2001.
- " Direct atomic structure determination of epitaxially grown films: Gd_2O_3 on GaAs(100) " PRB 66, 205311, 2002
- A new X-ray method for the direct determination of epitaxial structures, coherent Bragg rod analysis (COBRA)

→ Nature – Materials 2002 Oct issue cover paper



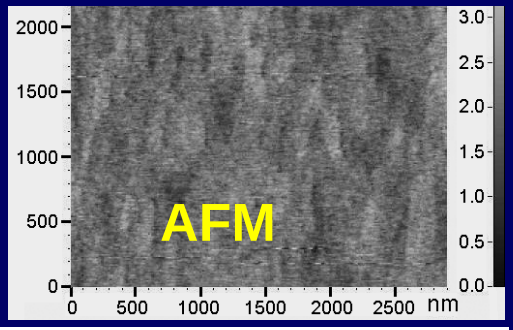


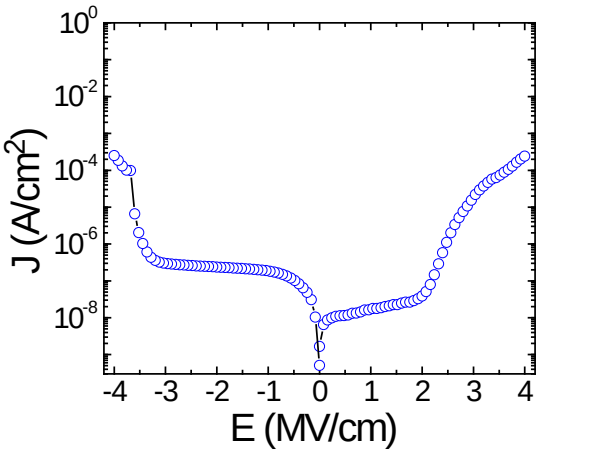
CET (EOT), D_{it} and *thermal stability at high Temp* in high κ's on *InGaAs, Ge, and GaN*

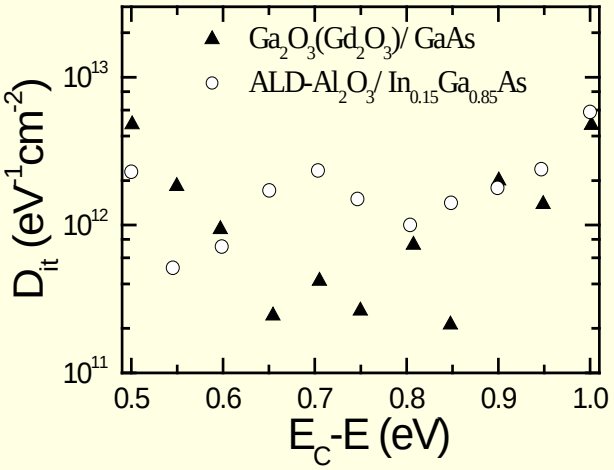
High κ's: single crystals, amorphous

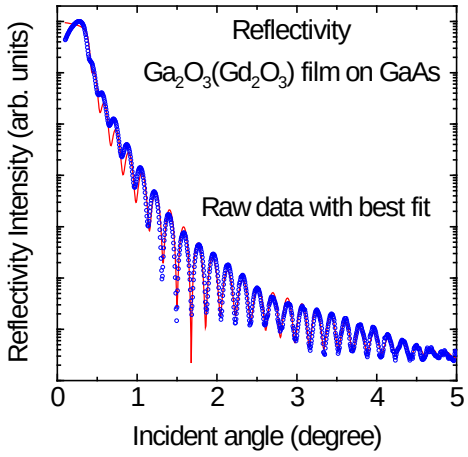
MBE-$Ga_2O_3(Gd_2O_3)$
MBE-HfAlO/HfO_2
MBE-Gd_2O_3, Y_2O_3, Al_2O_3, HfO_2
ALD-Al_2O_3, HfO_2
ALD+MBE

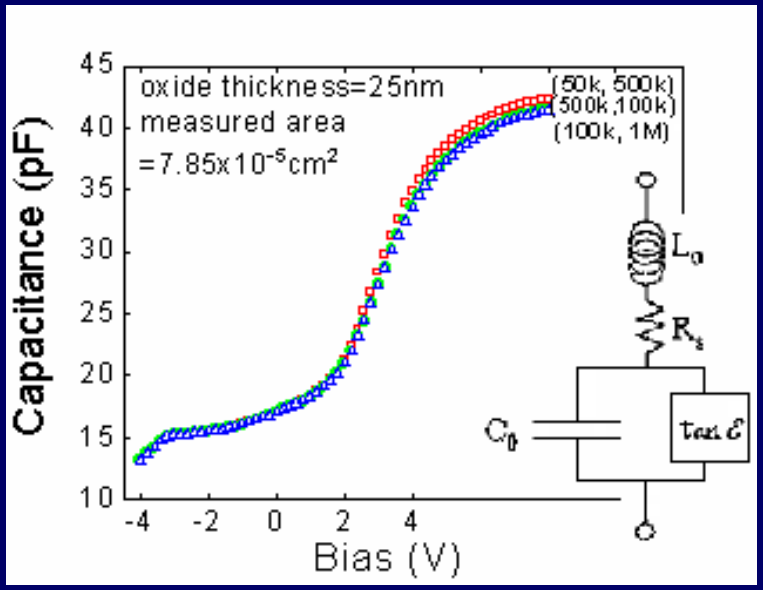
$Ga_2O_3(Gd_2O_3)$/GaAs under high temperature annealing in UHV and non-UHV



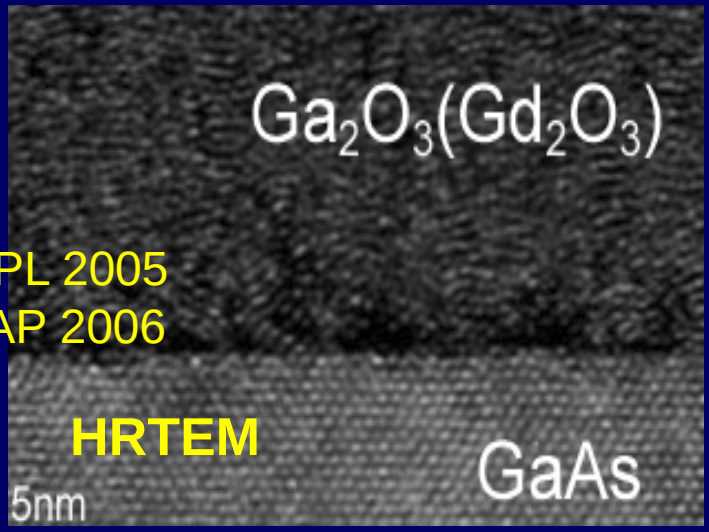




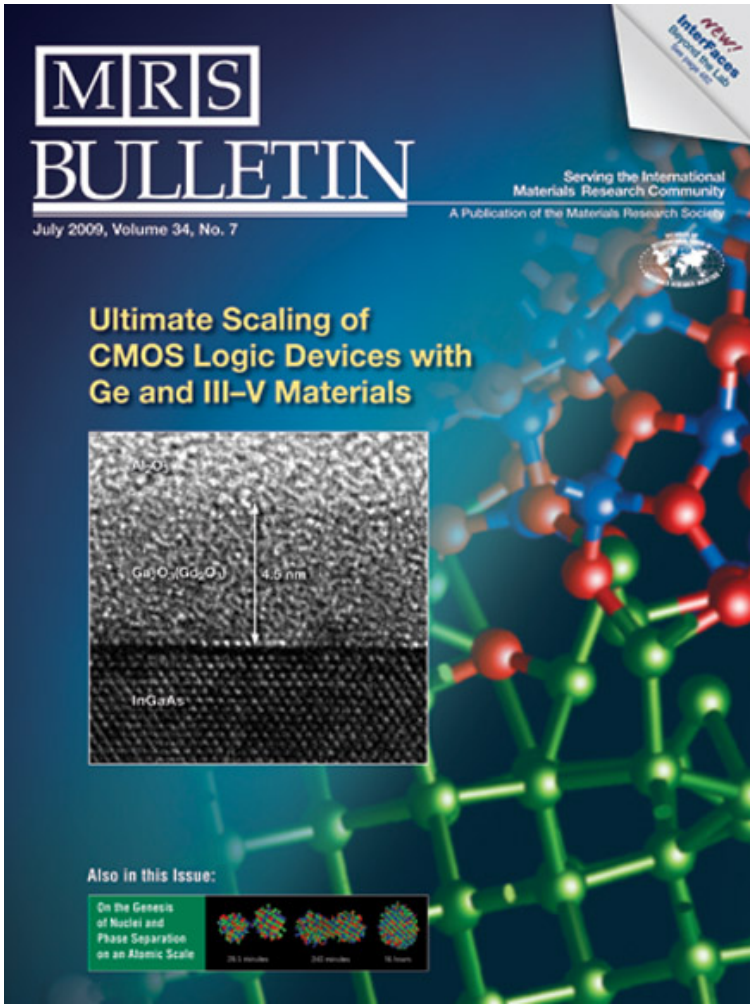


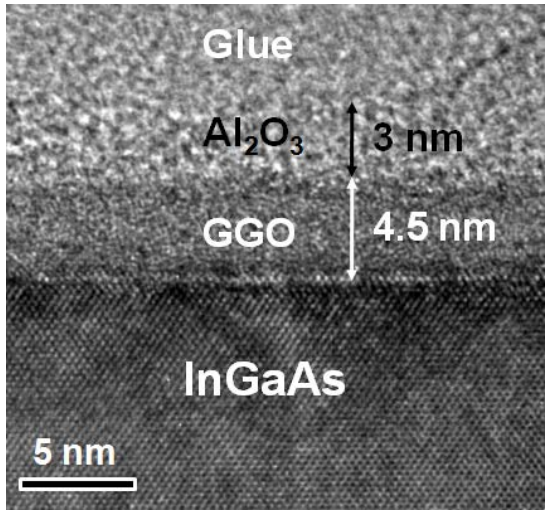


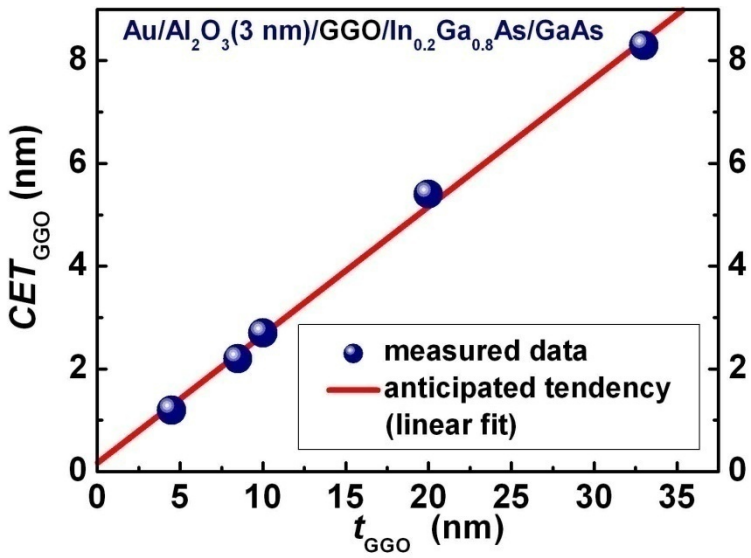
Y. L.Huang et al, APL 2005
C. P. Chen et al, JAP 2006



MRS Bulletin, July 2009

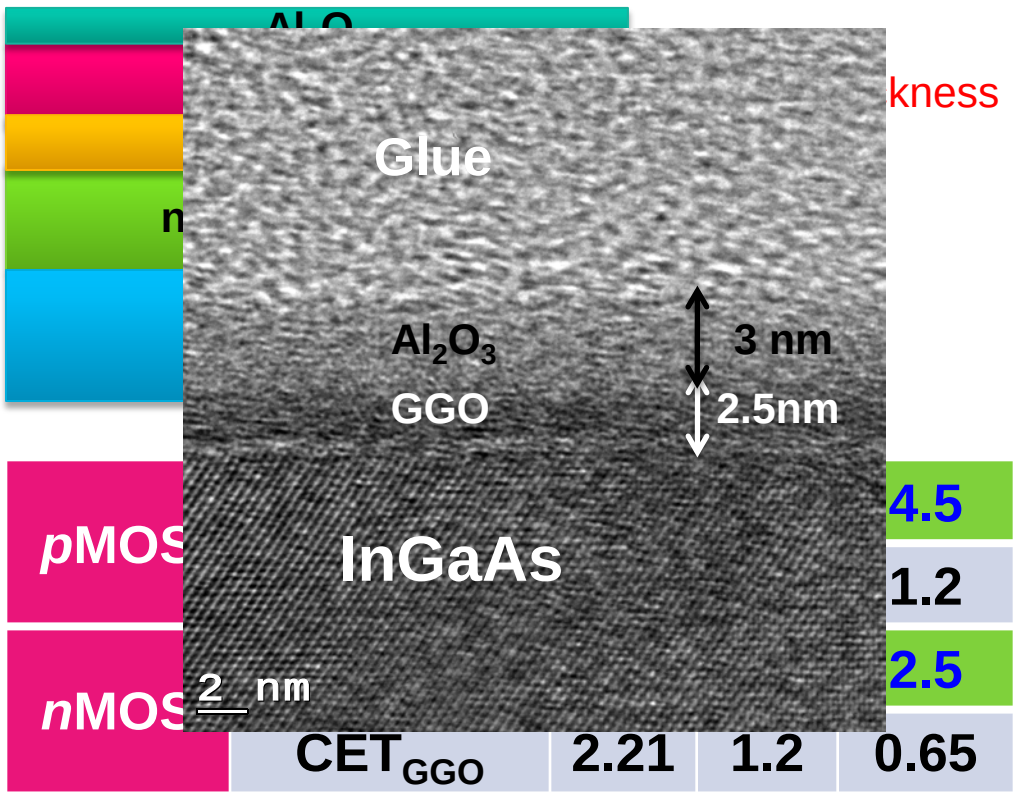


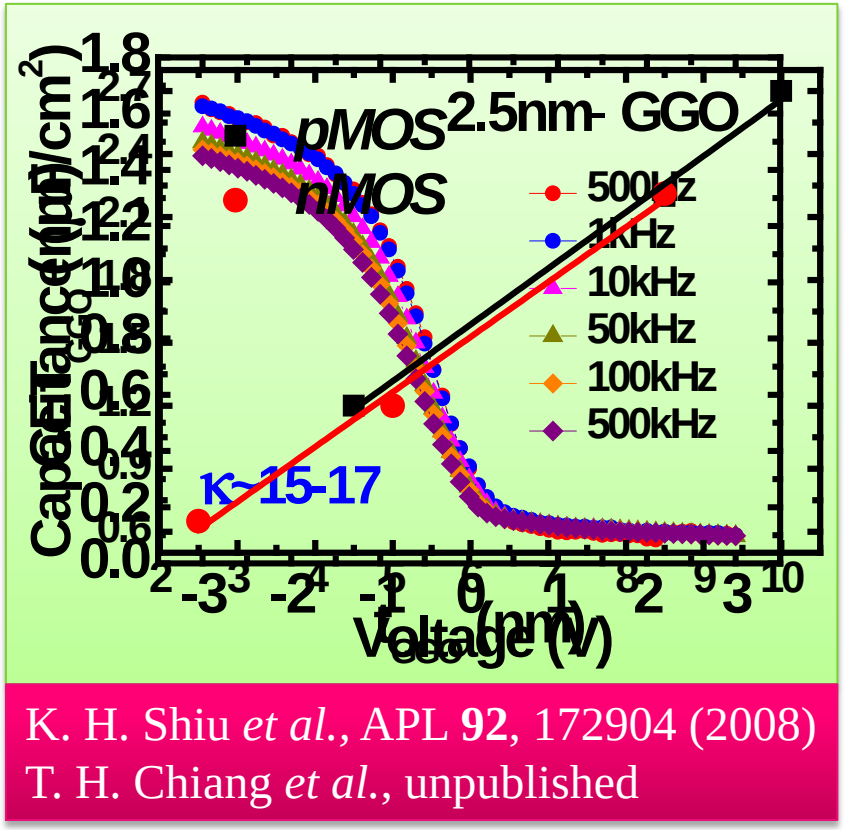




Cover Image & Theme Article – "*InGaAs Metal Oxide Semiconductor Devices with $Ga_2O_3(Gd_2O_3)$ High-κ Dielectrics for Science and Technology beyond Si CMOS*", M. Hong, J. Kwo, T. D. Lin, and M. L. Huang, MRS Bulletin **34**, 514 July 2009.

GGO Scalability and Thermal Stability



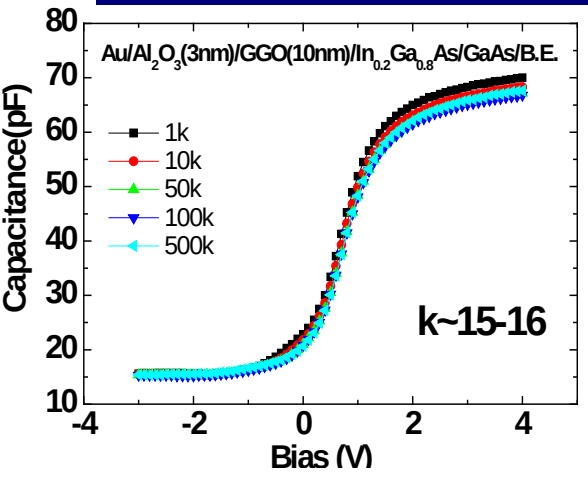


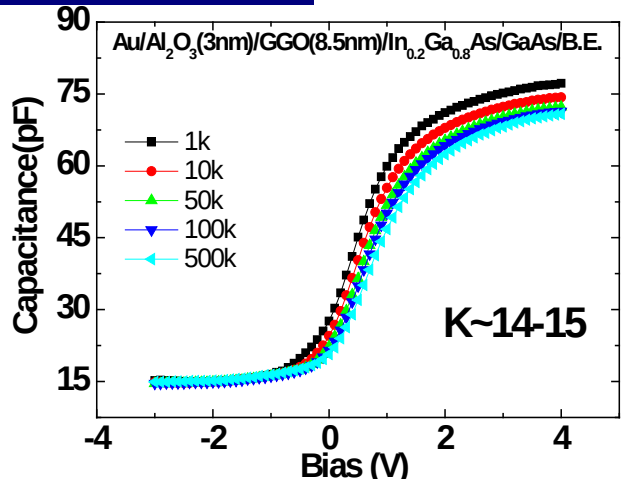
K. H. Shiu *et al.*, APL **92**, 172904 (2008)
T. H. Chiang *et al.*, unpublished

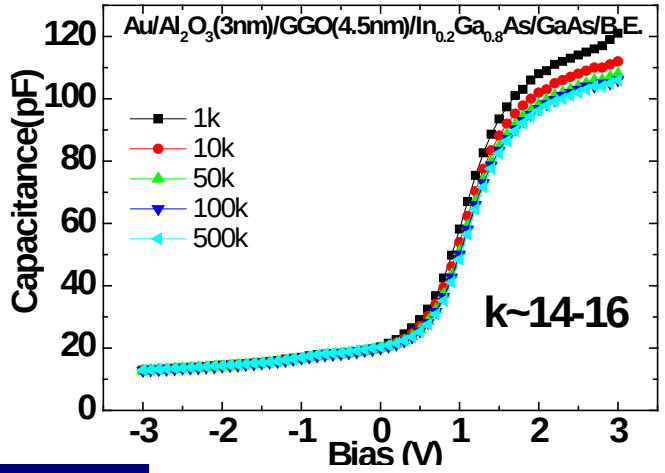
- Al_2O_3 capping effectively minimized absorption of moisture in GGO
- GGO (2.5nm) dielectric constant maintains ~15 (CET~7Å)
- D_{it}'s ~ low $10^{11}(cm^{-2}eV^{-1})$ range even subjected to 850°C annealing (Conductance Method)

C-V Characteristics – GGO/$In_{0.2}Ga_{0.8}As$

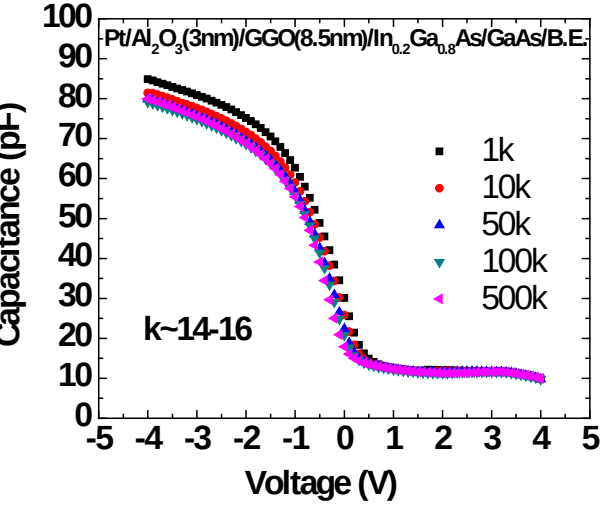
K. H. Shiu et al, APL 92, 172904 (2008)

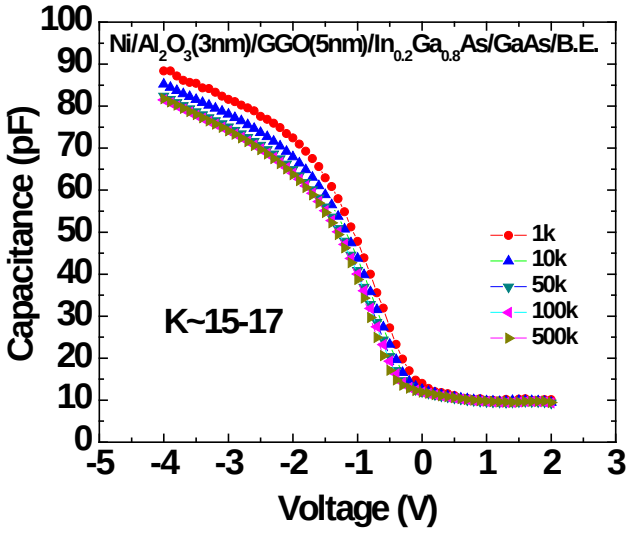


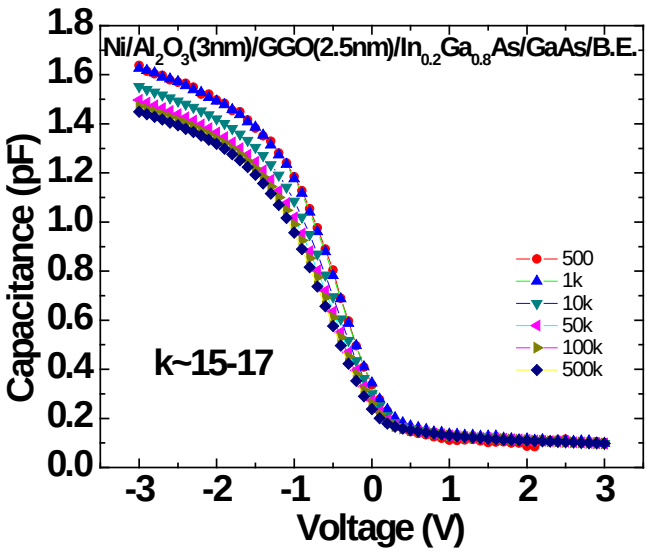




T. H. Chiang et al, National Tsing Hua University (unpublished)

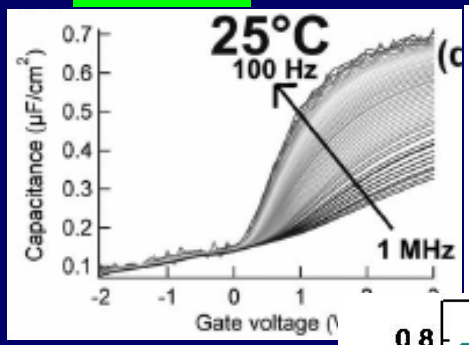


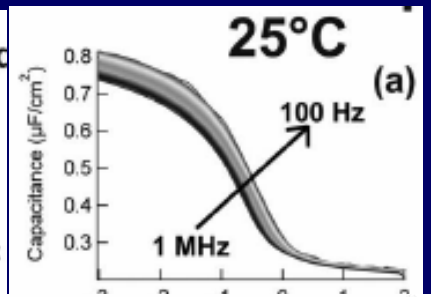


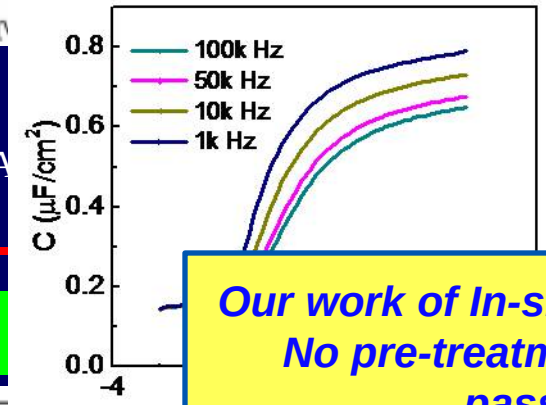


State-of-the-art work of ALD Al_2O_3/GaAs

IMEC $(NH_4)_2S$ treated GaAs

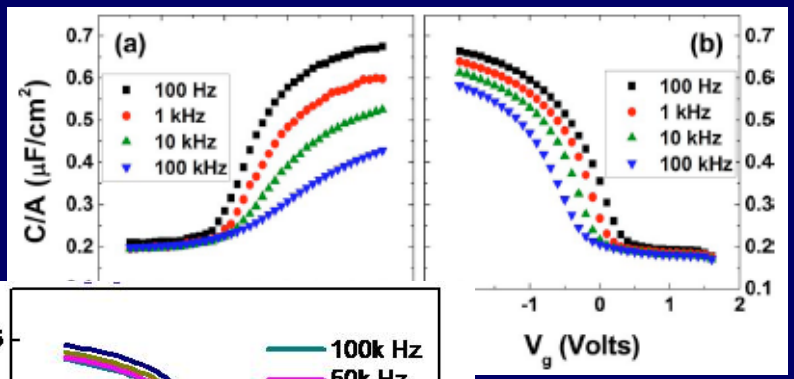


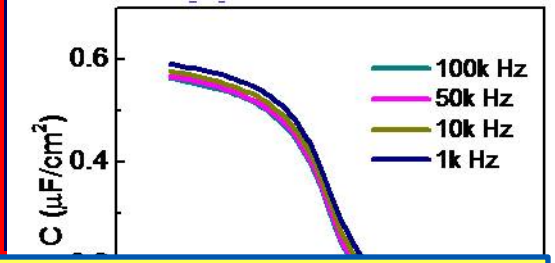




G. Brammertz, et al. A

U.T.Dallas NH_4OH treated GaAs

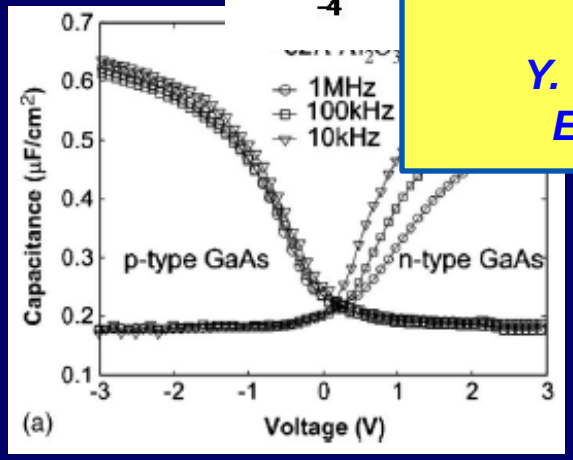




ys. Lett. **93**, 113506 (2008)

Our work of In-situ ALD + MBE Al_2O_3/GaAs
No pre-treatments and no interfacial passivation layers
Y. H. Chang, et al, Microelectronic Engineering 88, 440–443 (2011)

U.T. Austin

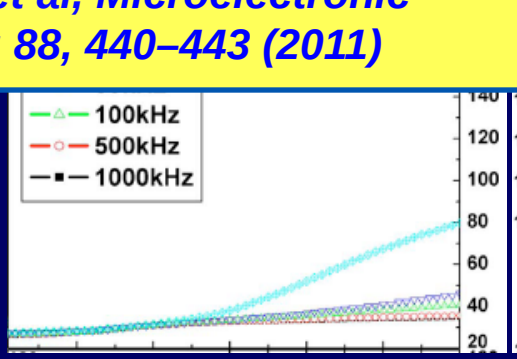


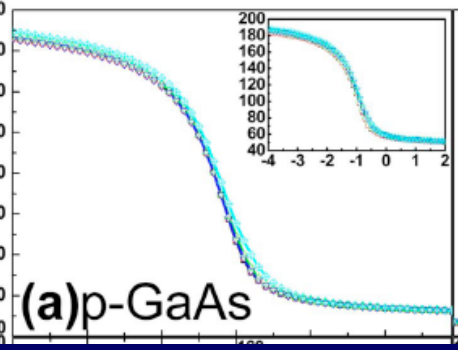
D. Shahrjerdi, et al. Appl. Phys. Lett. **92**, 203505 (2008)

MIT

$_3$ treated,

rowth with **TMA/IPA**

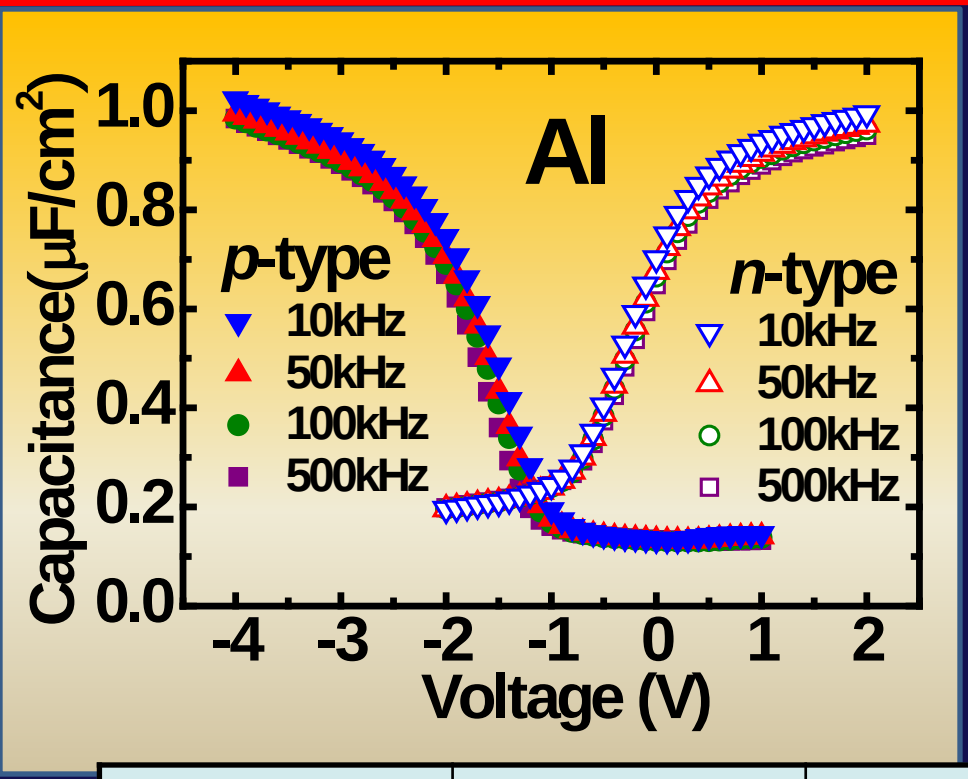


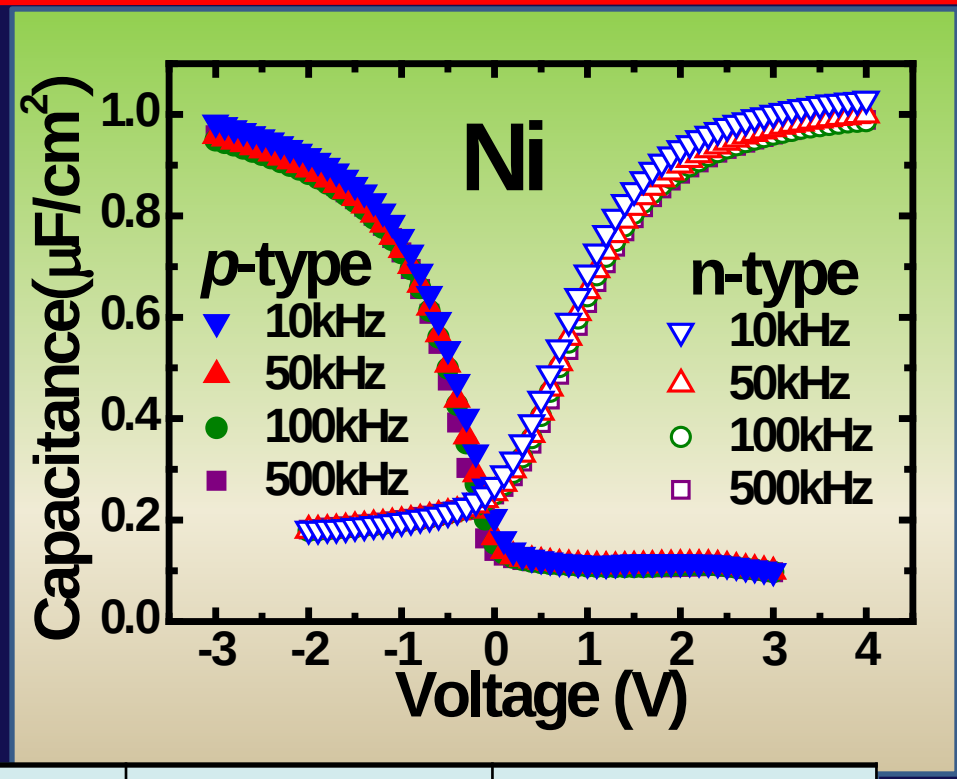


C.-W. Cheng, et al. Appl. Phys. Lett. **95**, 082106 (2009)

CV Characteristics of $Al_2O_3/GGO/In_{0.2}Ga_{0.8}As$

Y. D. Wu *et al.*, ***JVST B 28(3), C3H10 (2010)***

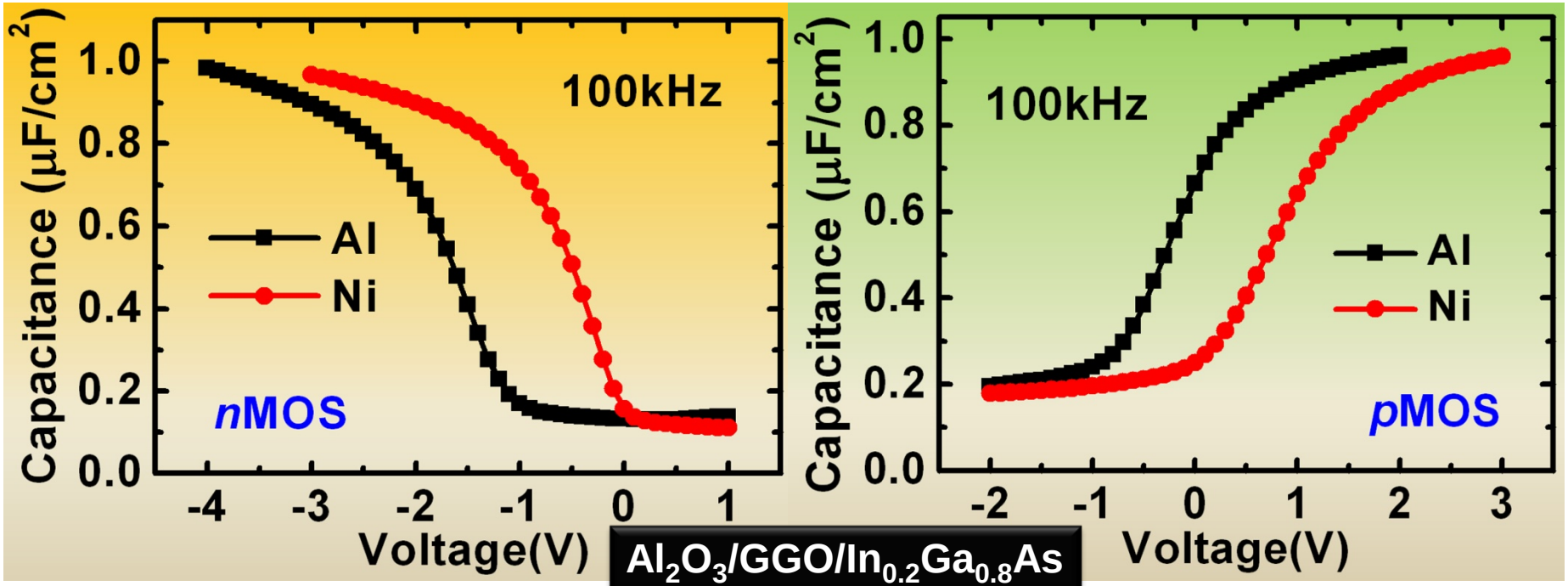




Gate	Substrate	κ value	C_{FB}(F/cm^2)	Dispersion (10k-500k)
Al	p-type	15-17	0.38	2.6%
Al	n-type	14-16	0.69	4.4%
Ni	p-type	14-16	0.37	3.5%
Ni	n-type	14-17	0.69	4.2%

NAM

Metal-work-function dependent flat-band voltages

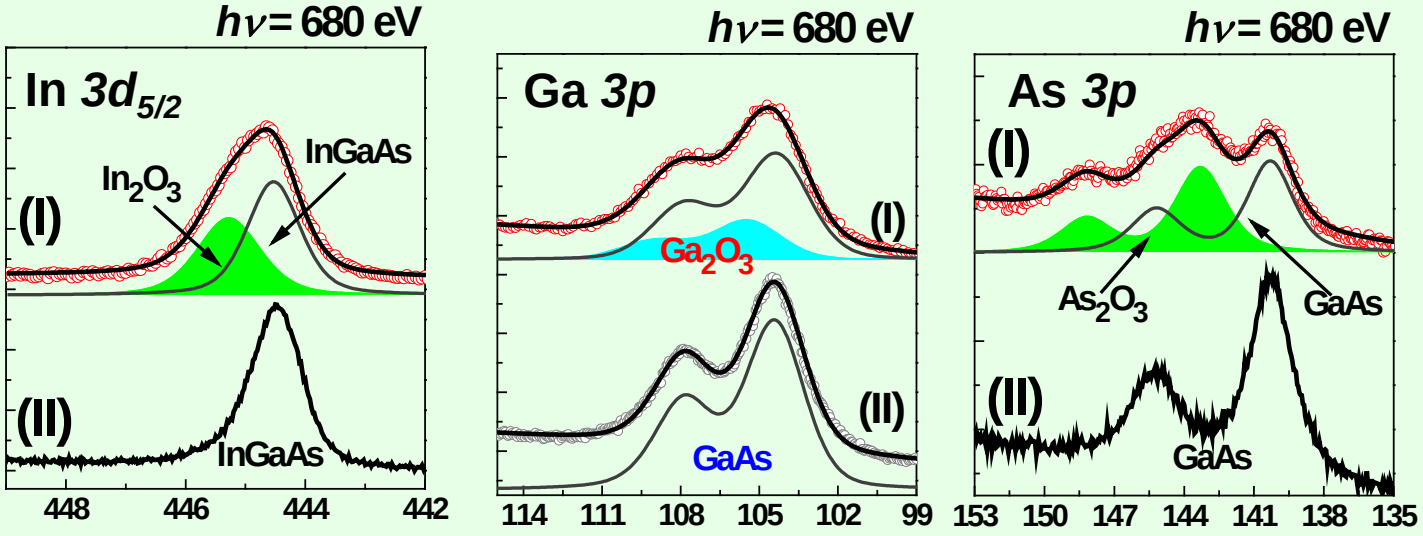


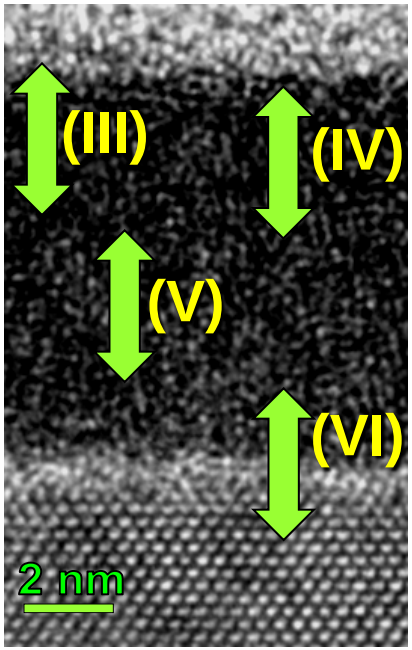
*n*MOS						
Gate metal	**ϕ_m (volt)**	**C_{fb} (μF/cm²)**	**V_{fb} (volt)**	**ΔV_{fb} (volt)**	**Dispersion (10-500kHz)**	**V_{th} (volt)**
Al	4.16±0.1	0.38	-1.42	-0.29±0.1	2.6%	0.04
Ni	5.19±0.15	0.37	-0.32	-0.22±0.15	3.5%	1.15
***p*MOS**						
Gate metal	**ϕ_m (volt)**	**C_{fb} (μF/cm²)**	**V_{fb} (volt)**	**ΔV_{fb} (volt)**	**Dispersion (10-500kHz)**	**V_{th} (volt)**
Al	4.16±0.1	0.69	0.05	0.17±0.1	4.4%	-1.94
Ni	5.19±0.15	0.69	1.12	0.21±0.15	4.2%	-0.88

Y. D. Wu *et al.*, ***JVST B 28(3), C3H10 (2010)***

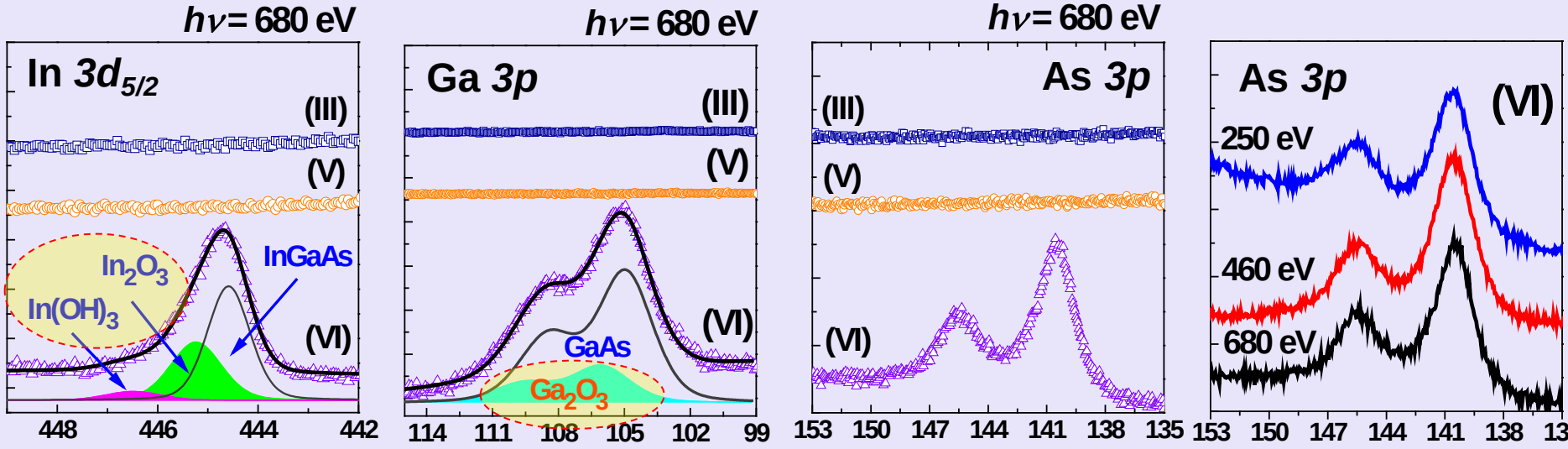
Depth profile of ALD-HfO_2/$In_{0.15}Ga_{0.85}As$: SR-XPS

Native oxide/$In_{0.15}Ga_{0.85}As$





8nm-HfO_2/$In_{0.15}Ga_{0.85}As$

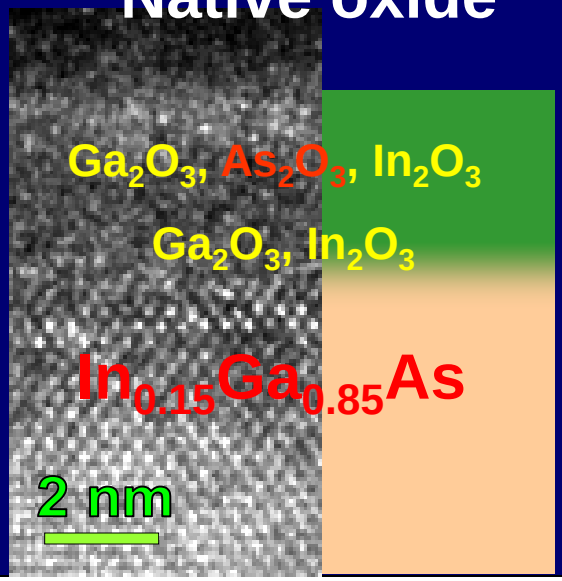


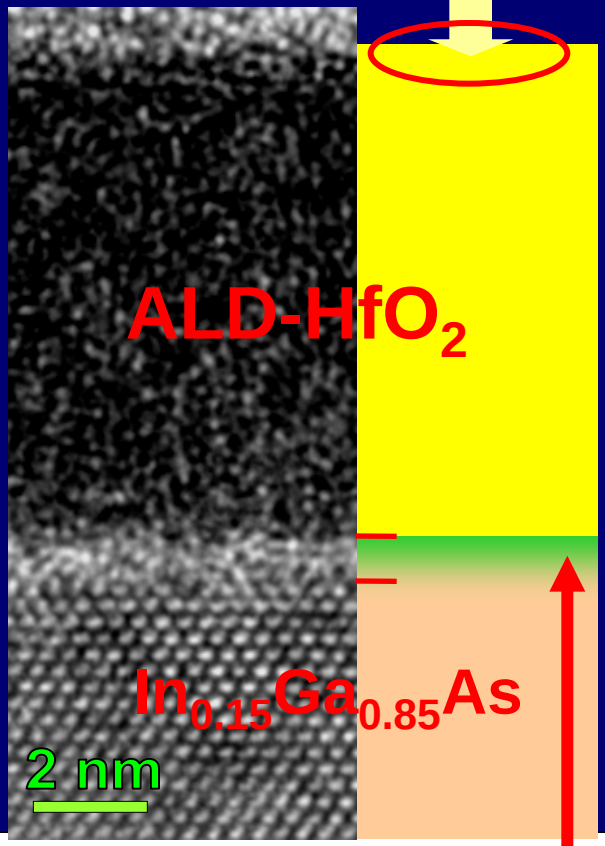
Fermi level unpinning at ALD-oxide/InGaAs

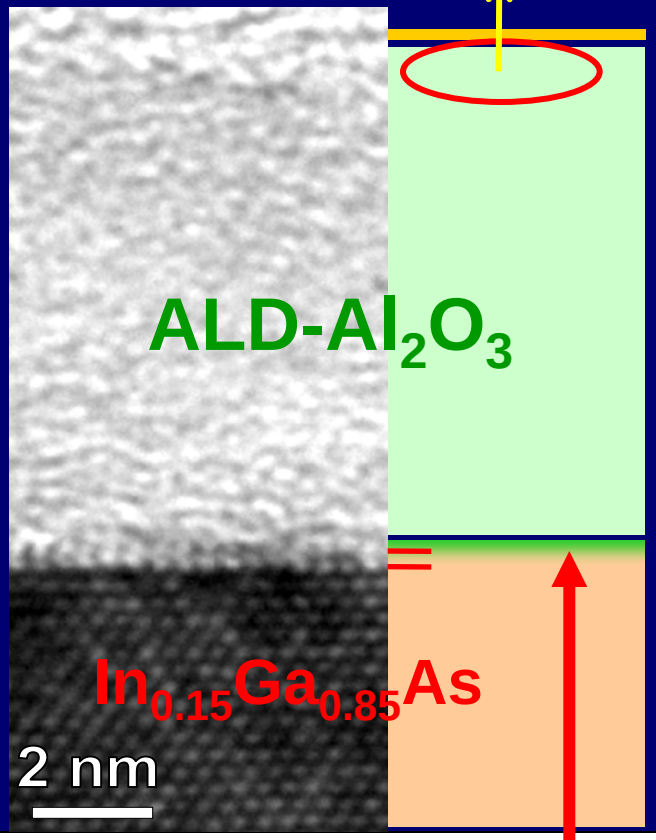
M.L.Huang, et al, APL 87, 252104 (2005); citations:115

Different chemical reaction for TEMAH/H_2O and TMA/H_2O on air-exposed InGaAs surface

Fraction of a mono-layer As_2O_5





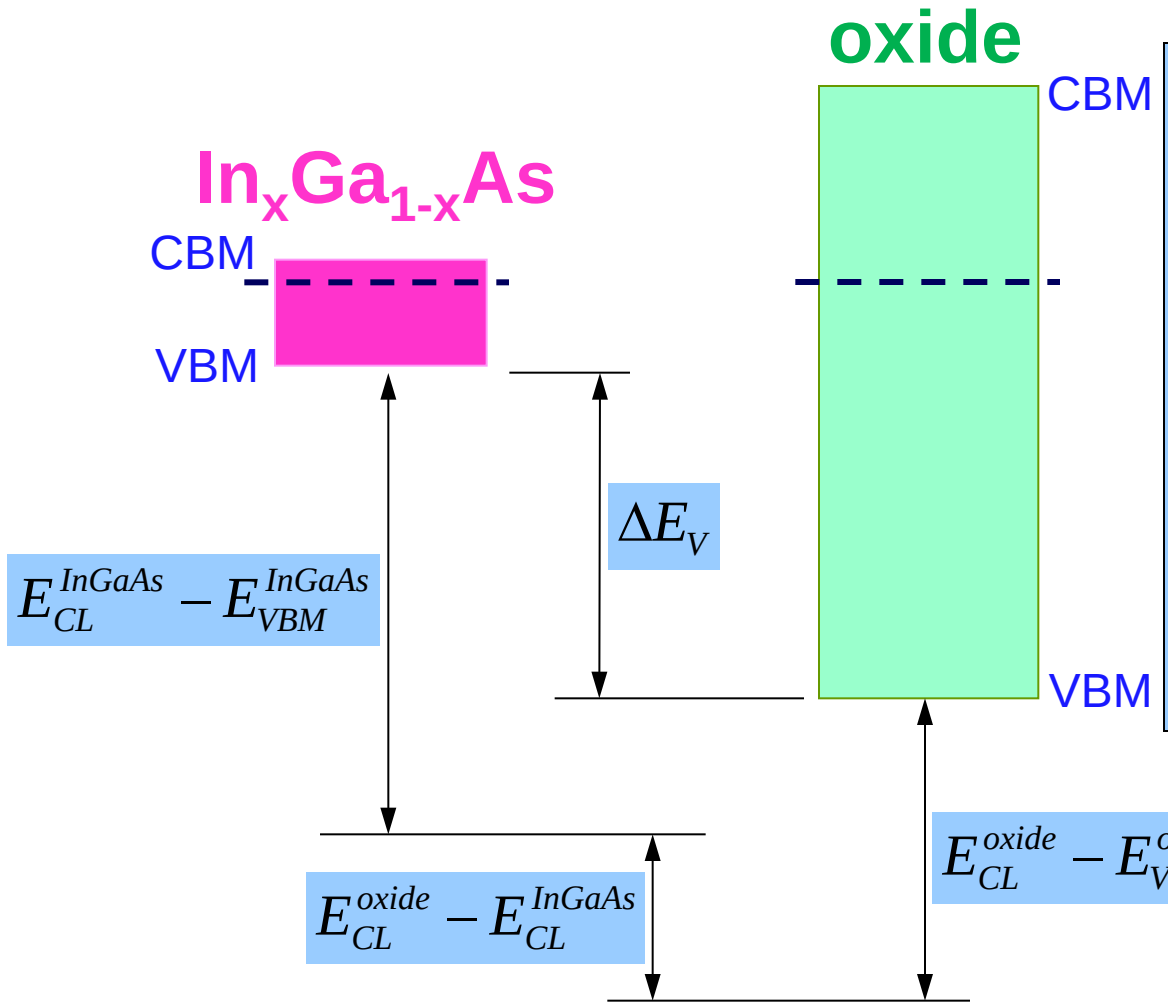


Interfacial layer: Ga_2O_3; In_2O_3; $In(OH)_3$

arsenic oxide was removed

Fermi Level unpinning

Valence band offsets: determined by XPS



E_{CL}^{InGaAs} : core level of InGaAs

E_{VBM}^{InGaAs} : valence level max of InGaAs

E_{CL}^{oxide} : core level of oxide

E_{VBM}^{oxide} : valence level maximum of oxide

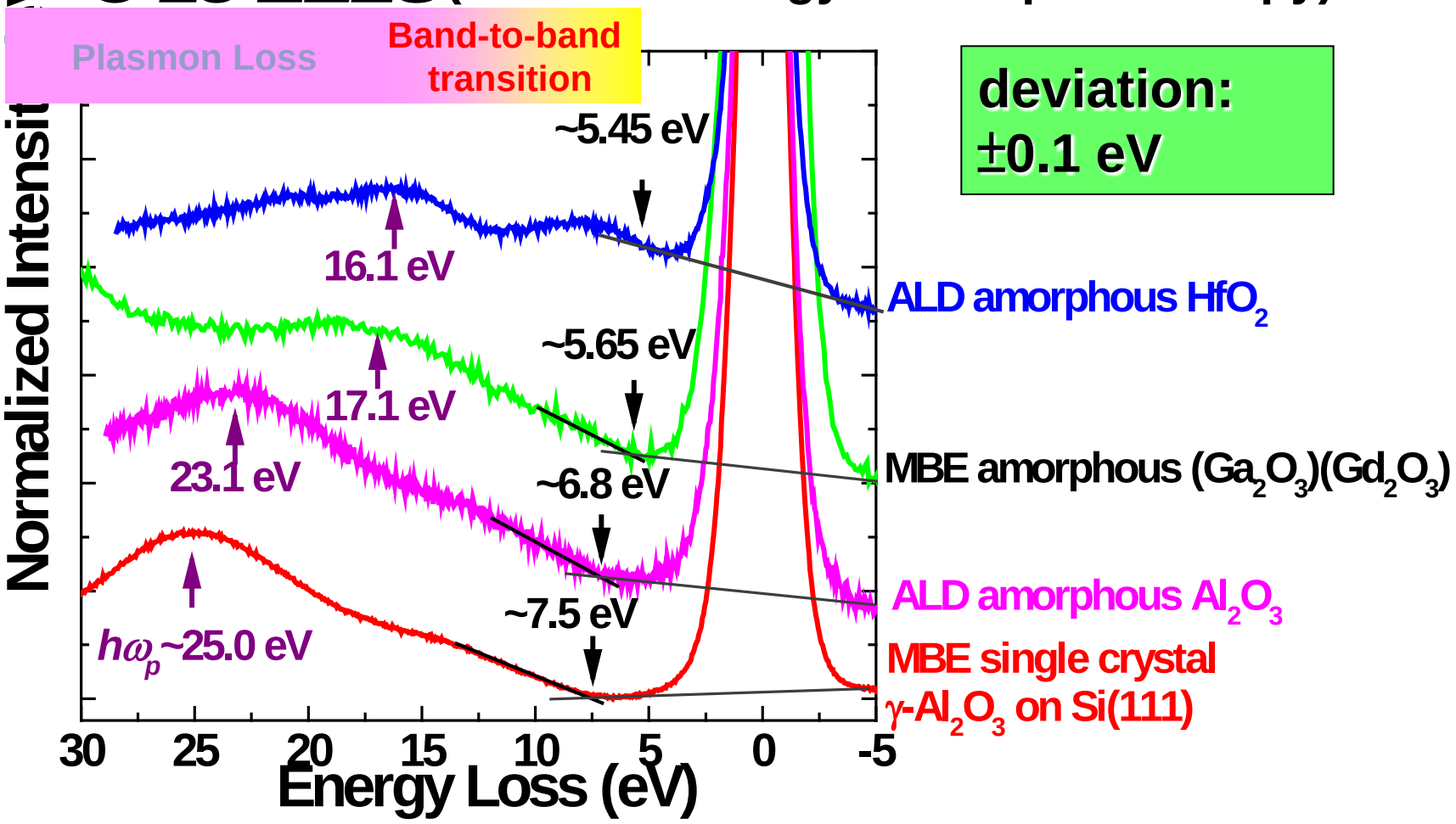
ΔE_v : Valence band offset

$$\Delta E_v = (E_{CL}^{InGaAs} - E_{VBM}^{InGaAs}) + (E_{CL}^{oxide} - E_{CL}^{InGaAs}) - (E_{CL}^{oxide} - E_{VBM}^{oxide})$$

E. A. Kraut et al., PRL 44, 1620 (1980); A. Franciosi et al., Surf. Sci. Rep. 25, 1 (1996)
M. L. Huang et al., APL 89, 012903 (2006)

Bandgap of oxide : determined by photoemission-EELS

O *1s EELS* (Electron Energy Loss Spectroscopy)

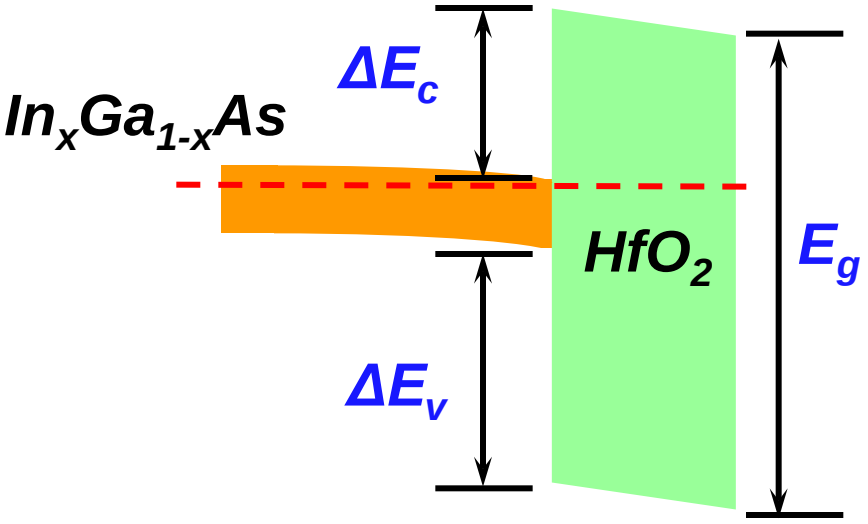


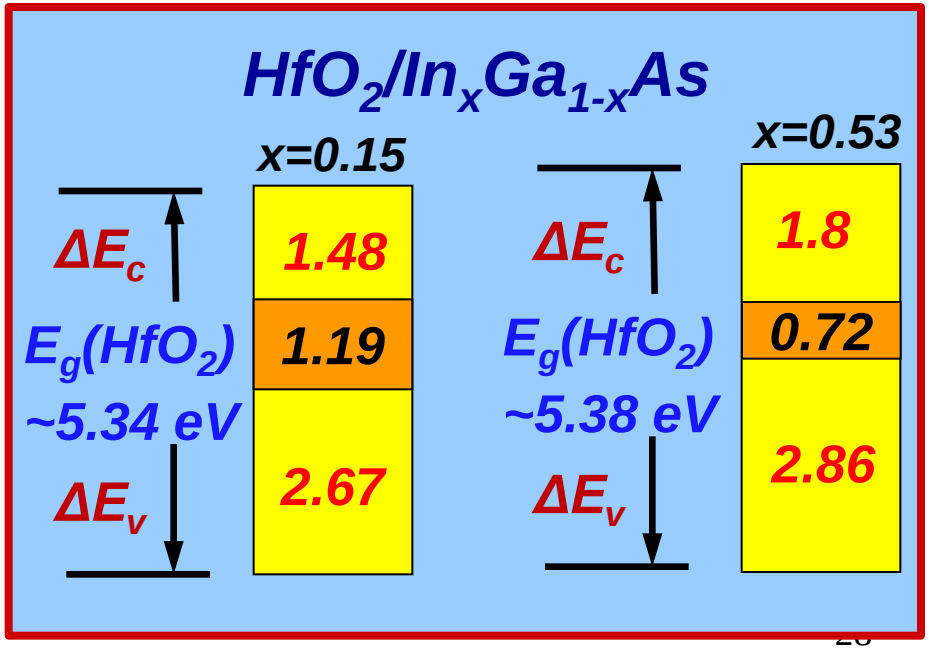
The minimum energy of band-to-band transition => Bandgap (E_g)

Energy-Band Parameters at HfO_2/InGaAs

$$\Delta E_v = (E_{CL}^{InGaAs} - E_{VBM}^{InGaAs}) + (E_{CL}^{oxide} - E_{CL}^{InGaAs}) - (E_{CL}^{oxide} - E_{VBM}^{oxide})$$

	$E_{As3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}$	$E_{Hf\,4f_{7/2}}^{oxide} - E_{As3d_{5/2}}^{InGaAs}$	$E_{Hf\,4f_{7/2}}^{oxide} - E_{VBM}^{oxide}$	ΔE_V
HfO_2/GaAs	40.36 eV	-23.58 eV	14.19 eV	2.62 eV
HfO_2/$In_{0.15}Ga_{0.85}As$	40.42 eV	-23.56 eV	14.19 eV	2.67 eV
HfO_2/$In_{0.53}Ga_{0.47}As$	40.57 eV	-23.52 eV	14.19 eV	2.86 eV





[1] M. L. Huang et al., APL 89, (2006)

Conduction band offsets: F-N tunneling

$\ln(J_{FN}/E_{ox}^2) = S/E_{ox} + \ln(C)$

$S = -8\pi(2m^*)^{1/2}(\varphi)^{3/2}/3qh$

$C = q^3/8\pi h\varphi m^*$

Φ_m: metal work function

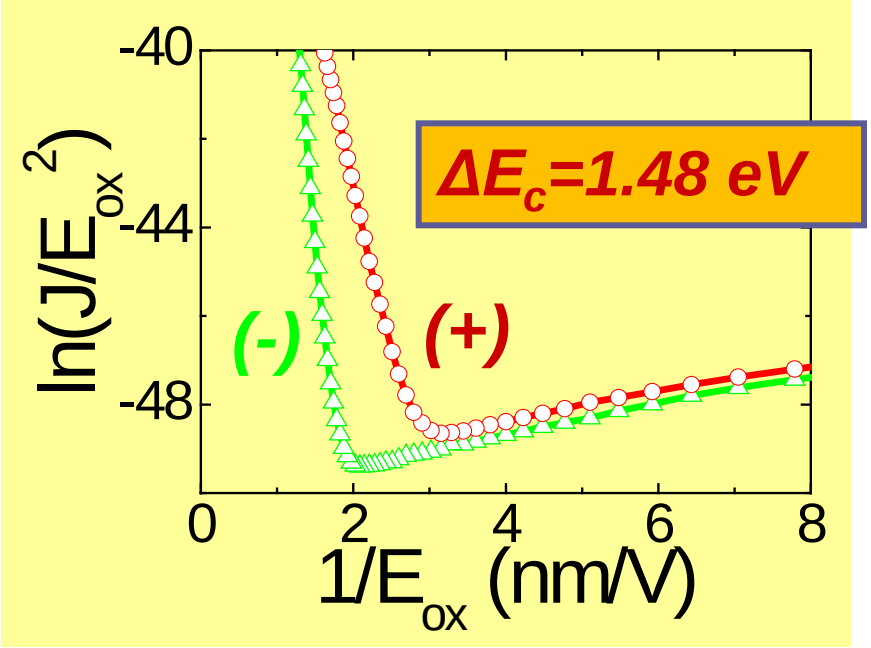
χ_s : electron affinity of InGaAs

$(\varphi^- - \varphi^+) = (\Phi_m - \chi_s)$ --- (1)

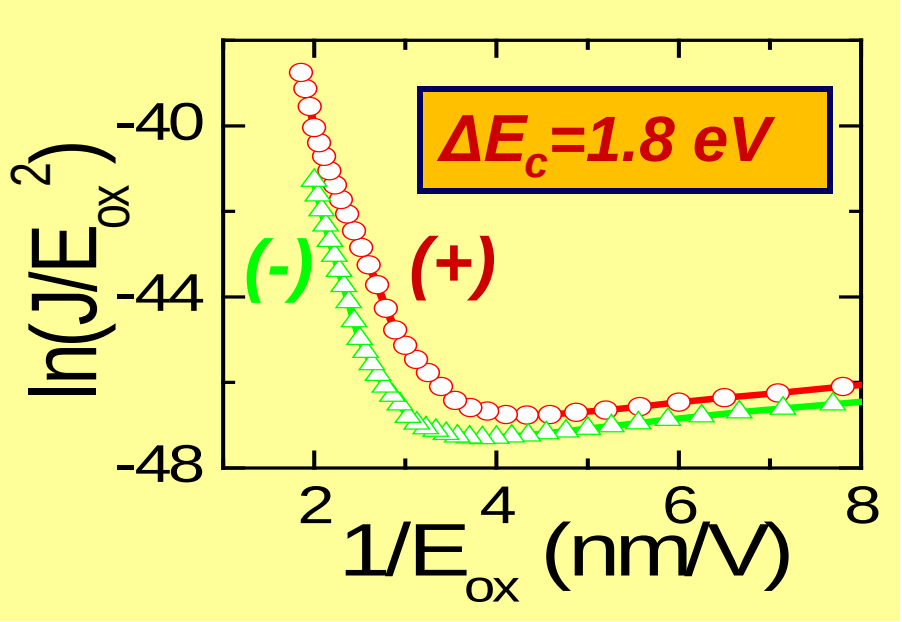
$S^+ = -8\pi(2m^*)^{1/2}(\varphi^+)^{3/2}/3qh$ --- (2)

$S^- = -8\pi(2m^*)^{1/2}(\varphi^-)^{3/2}/3qh$ --- (3)

$8.3nm\text{-}HfO_2 / In_{0.15}Ga_{0.85}As$



$7.8nm\text{-}HfO_2 / In_{0.53}Ga_{0.47}As$



deviation : ±0.08 eV

[1] T.S. Lay et al, Solid State Electron. 45, (2001)

[2] Y. C. Chang, et. al. Appl. Phys. Lett, 92, 072901 (2008).

Discussion: Energy band parameters

ALD-Al_2O_3/$In_xGa_{1-x}As$

	x=0	x=0.15	x=0.25	x=0.5
ΔE_c	1.71	1.83	1.89	2.09
$E_g(Al_2O_3)$ ~6.8 eV	1.42	1.19	1.05	0.75
ΔE_v	3.67	3.78	3.86	3.96

ALD-HfO_2/$In_xGa_{1-x}As$

	x=0	x=0.15	x=0.25	x=0.5
ΔE_c	1.41	1.59	1.66	1.84
$E_g(HfO_2)$ ~5.45 eV	1.42	1.19	1.05	0.75
ΔE_v	2.62	2.67	2.74	2.86

deviation : ±0.1 eV

ALD-Al_2O_3/$In_{0.15}Ga_{0.85}As$

$E_g(Al_2O_3)$ ~6.8 eV

ΔE_c	1.83±0.1eV	1.6 ± 0.1 eV
	1.19 eV	
ΔE_v	3.78 eV	

XPS method

FN tunneling

ALD-HfO_2/$In_{0.5}Ga_{0.5}As$

x=0.5

$E_g(HfO_2)$ ~5.45 eV

ΔE_c	1.84 ±0.1 eV	1.8 ± 0.1 eV
	0.75 eV	
ΔE_v	2.86 eV	

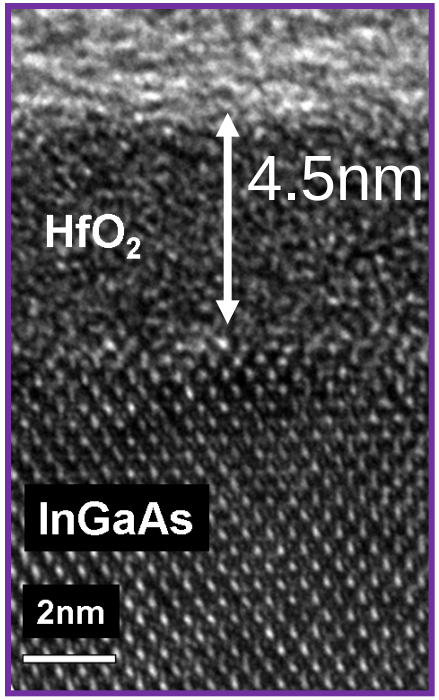
XPS method

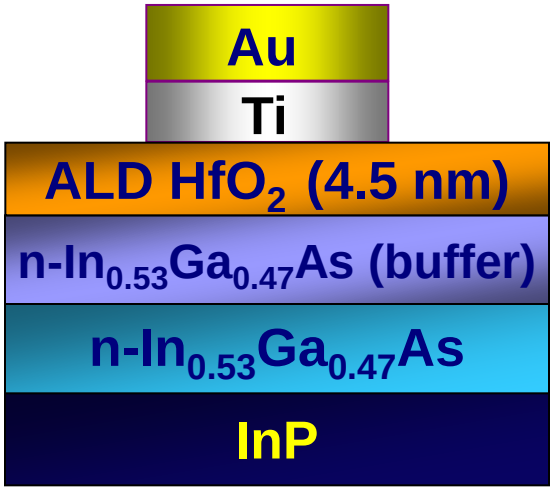
FN tunneling

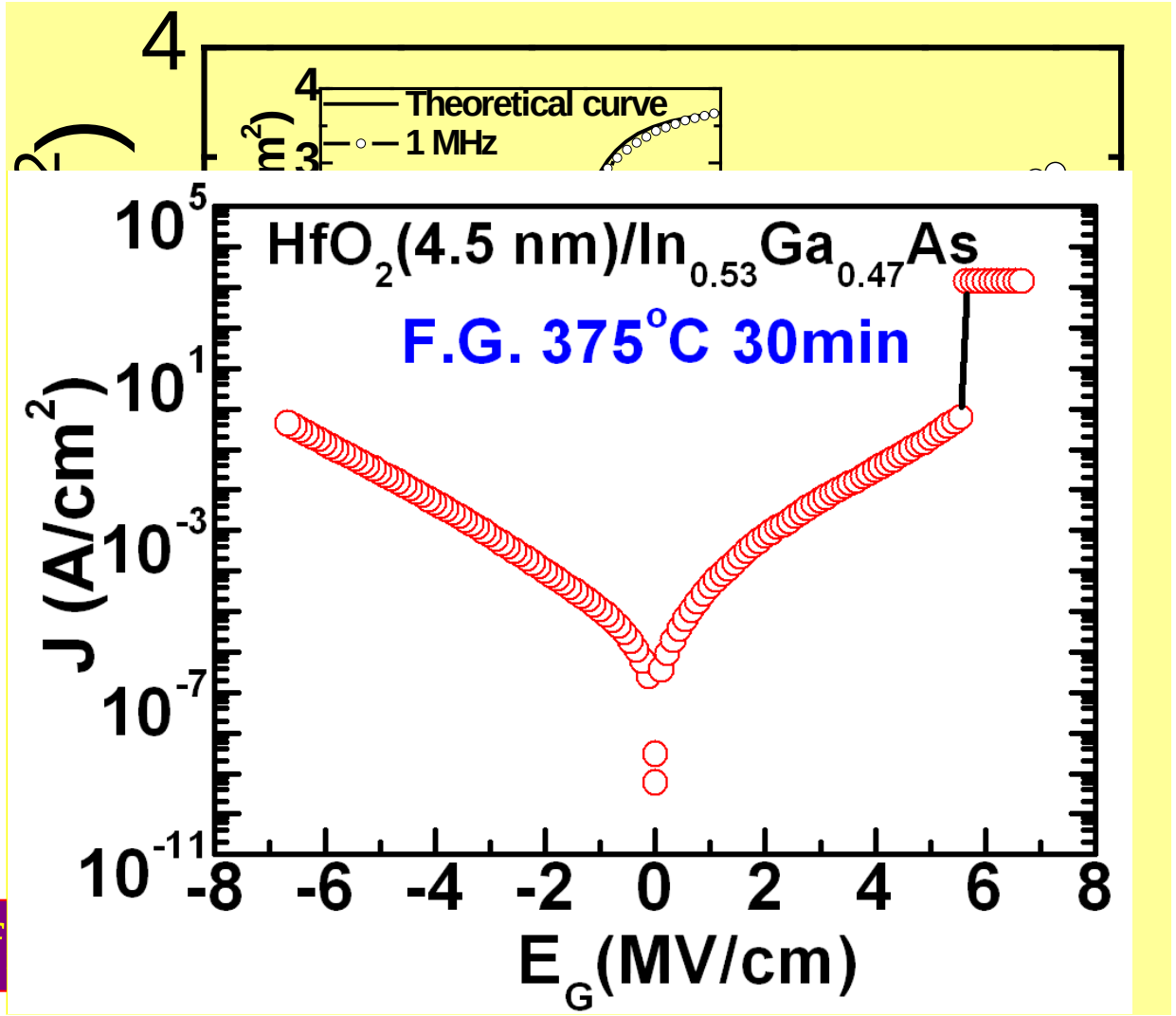
Y.C. Chang et al, APL 92 072901 (2008)
K. Y. Lee et al, APL 92, 252908 (2008)

ALD-HfO_2 on $In_{0.53}Ga_{0.47}As$ with short air exposure ~10 min

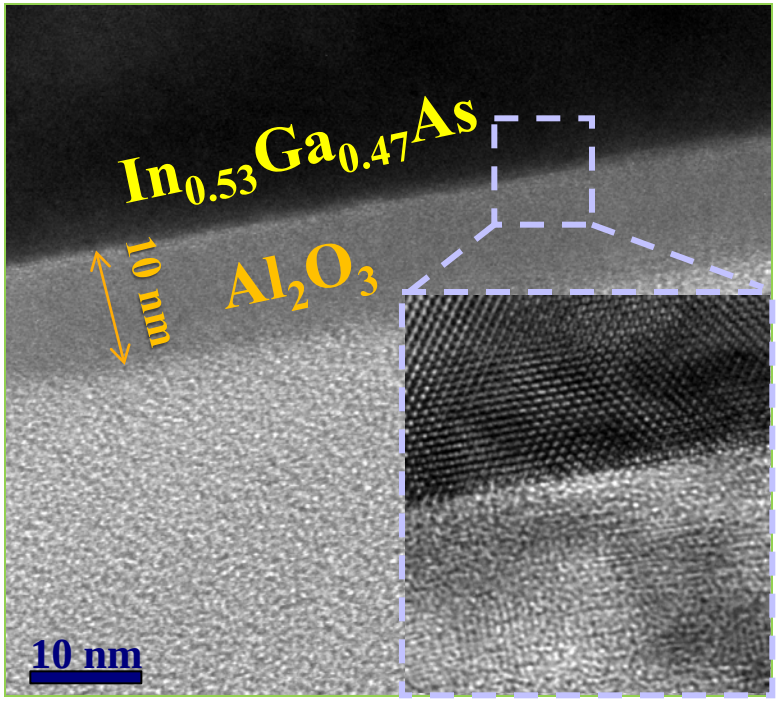
k ~17@100 kHz, CET=1nm

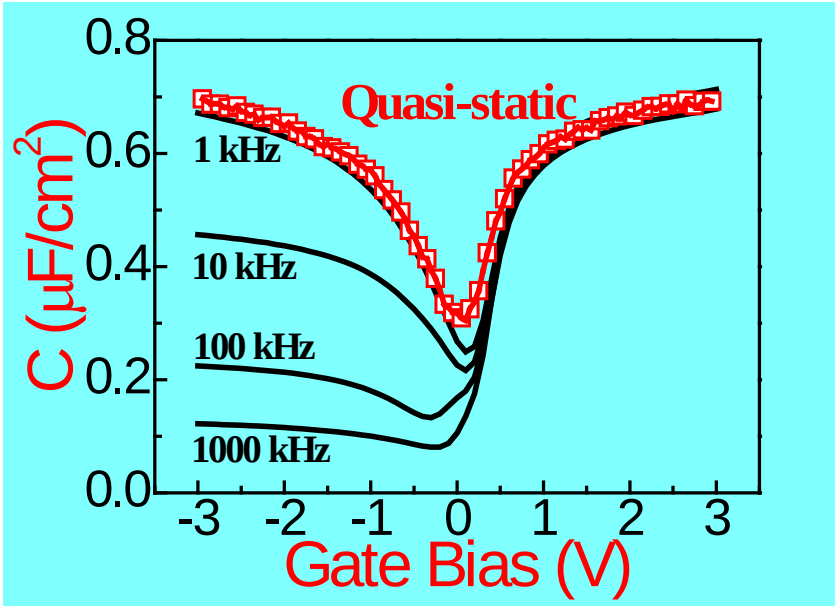




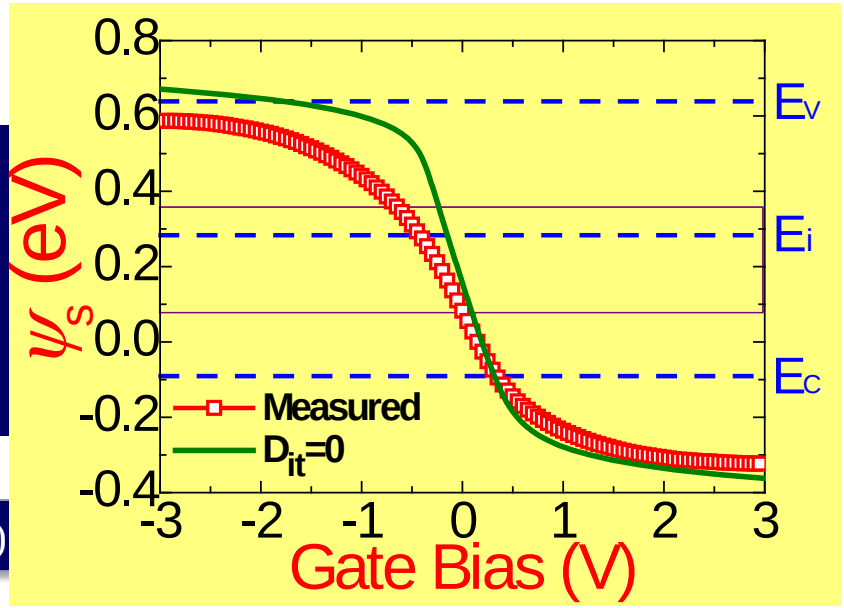


Achieving a low D_{it} in ALD-Al_2O_3 on $In_{0.53}Ga_{0.47}As$ with short air exposure





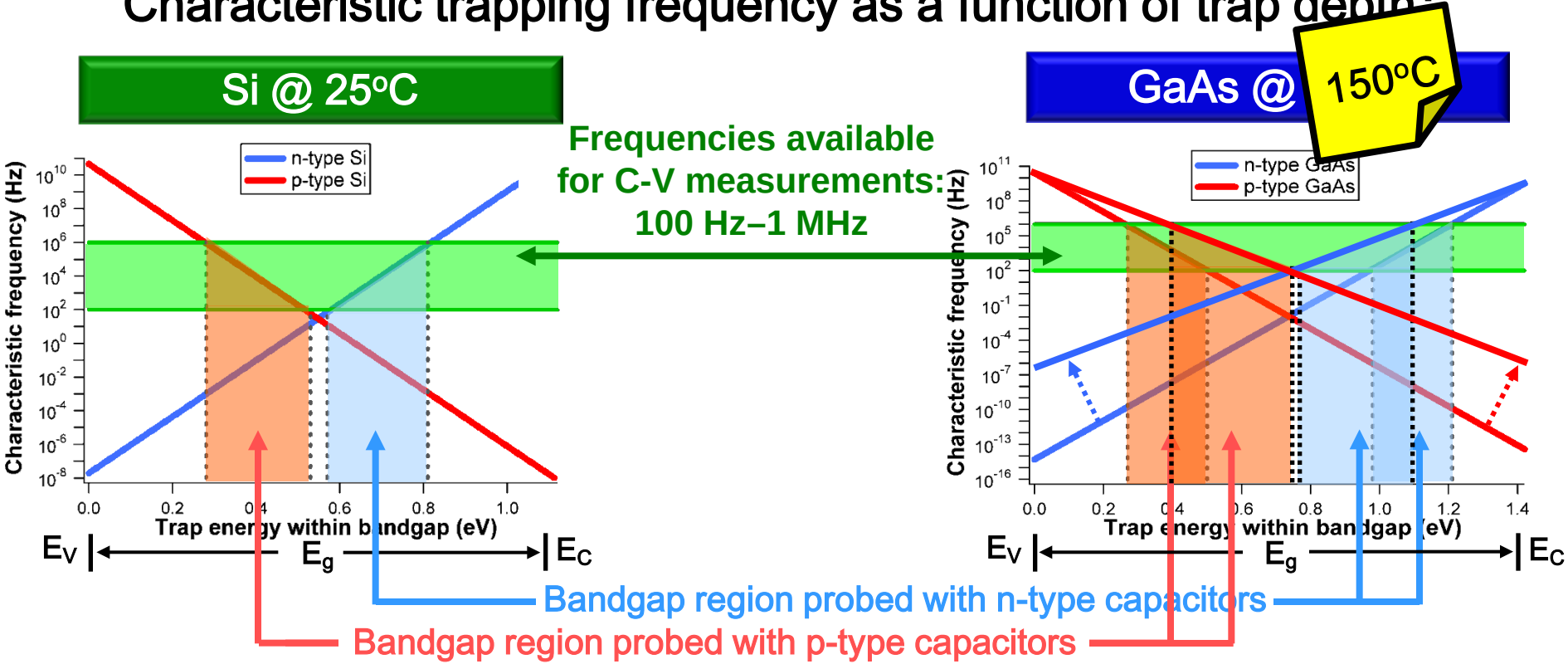
- very sharp Al_2O_3/InGaAs interface
- Fermi-level moves across the nearly entire bandgap
- high FLME of **63%** near midgap



H. C. Chiu et al., *Appl. Phys. Lett.*, 93, 202903 (2008)

D_{it} Extraction for Wide Bandgap Semiconductors

Characteristic trapping frequency as a function of trap depth:



For GaAs MOS devices:

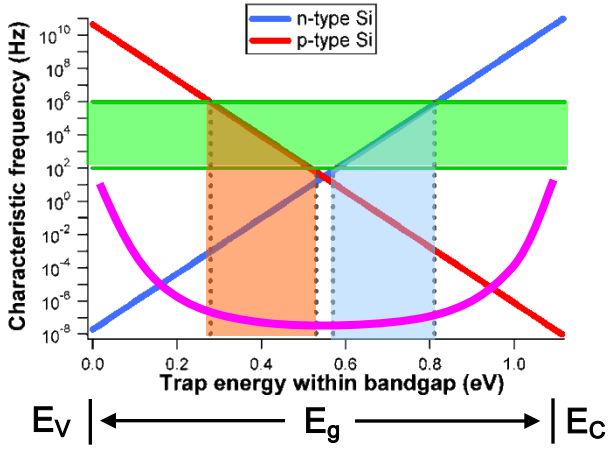
- Only very small portions of bandgap can be probed at 25°C.
- The midgap region is not accessible at all with these frequency range.

Measurements at 150°C giving a better coverage of the midgap region

Why D_{it} Extraction at Midgap is Important for GaAs?

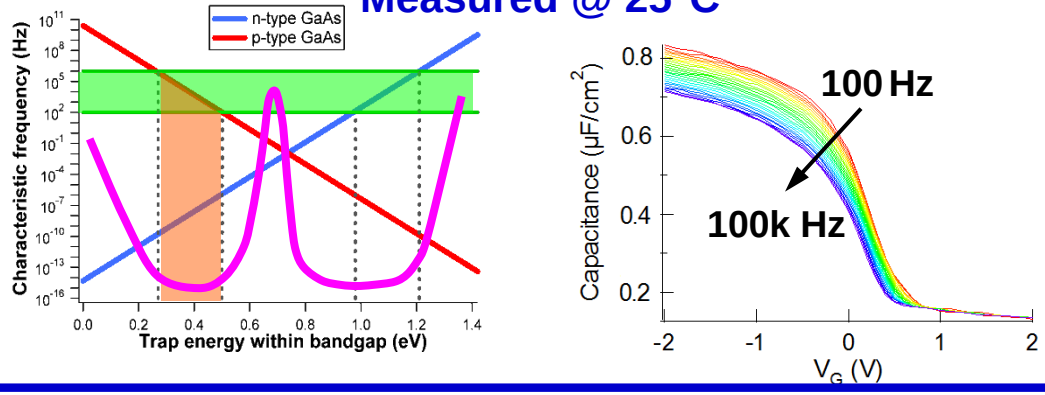
D_{it} distribution (—) as a function of the energy above E_v:

Si @ 25°C

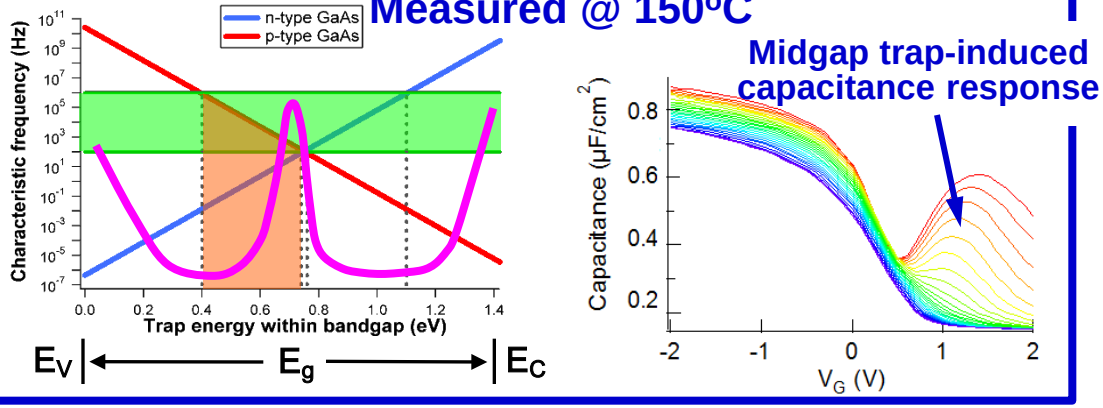


GaAs

Measured @ 25°C



Measured @ 150°C



- Unlike SiO_2/Si showing a flat D_{it} distribution at midgap, oxide/GaAs interfaces have high D_{it} at midgap → serious Fermi level pinning near midgap

W.E. Spicer *et al.*, JVST 91, 1422 (1979)

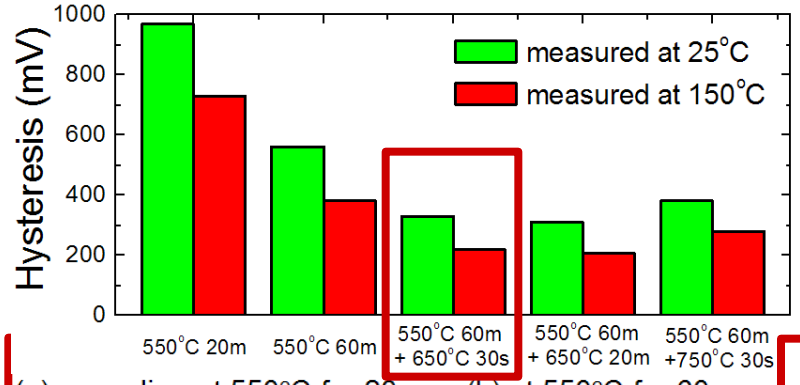
G. Brammertz *et al.*, APL 91, 133510 (2007)

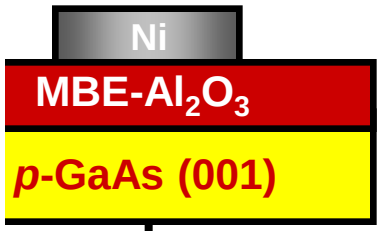
Y.C. Chang *et al.*, 68th DRC (2010)

K. Martens *et al.*, IEEE TED 55, 547 (2008)

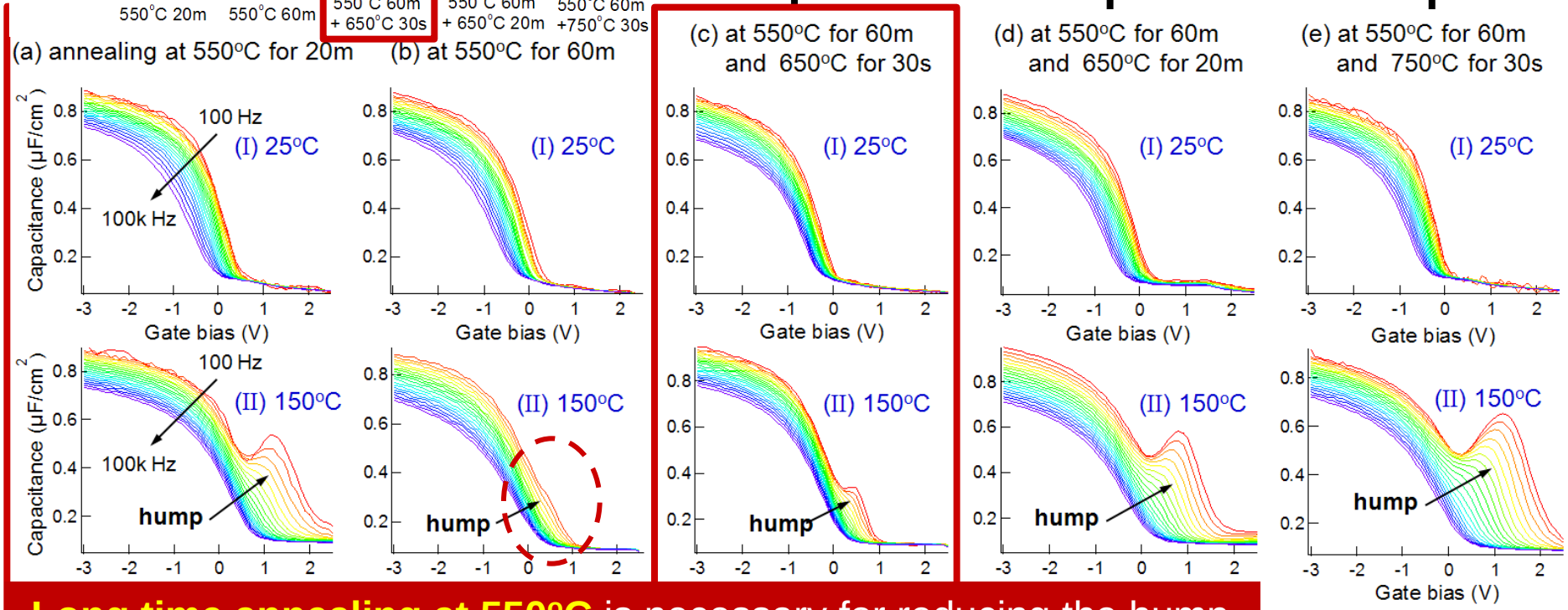
Y. C. Chang, J. Kwo*, and M. Hong*, et al, Appl. Phys. Lett. **97**, 112901 (2010).

Impact of **Post-Deposition-Annealing**





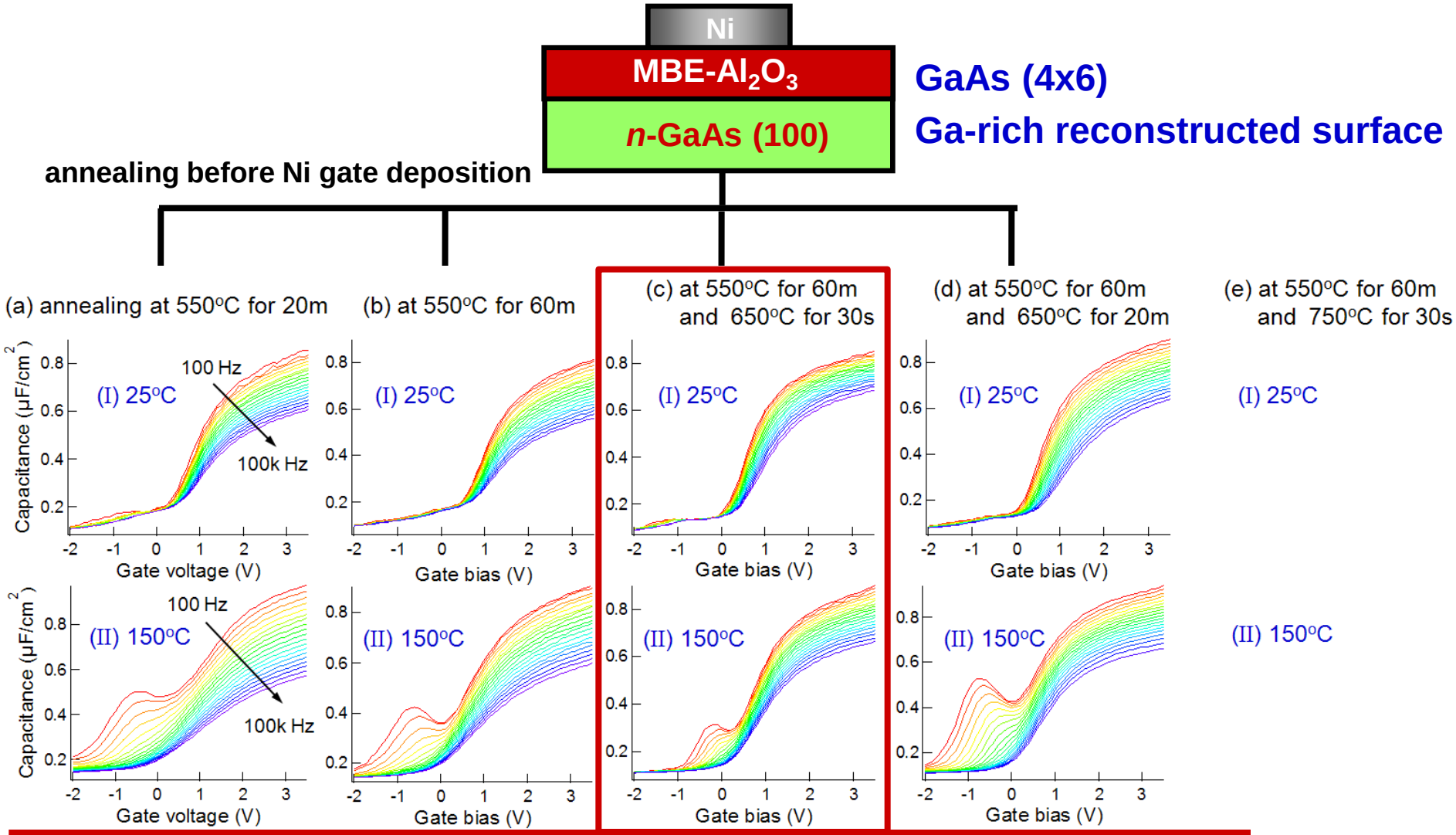
Ga-rich reconstructed surface



Long time annealing at 550°C is necessary for reducing the hump

Additional **RTP 650°C** is useful for optimizing the frequency dispersion and hysteresis

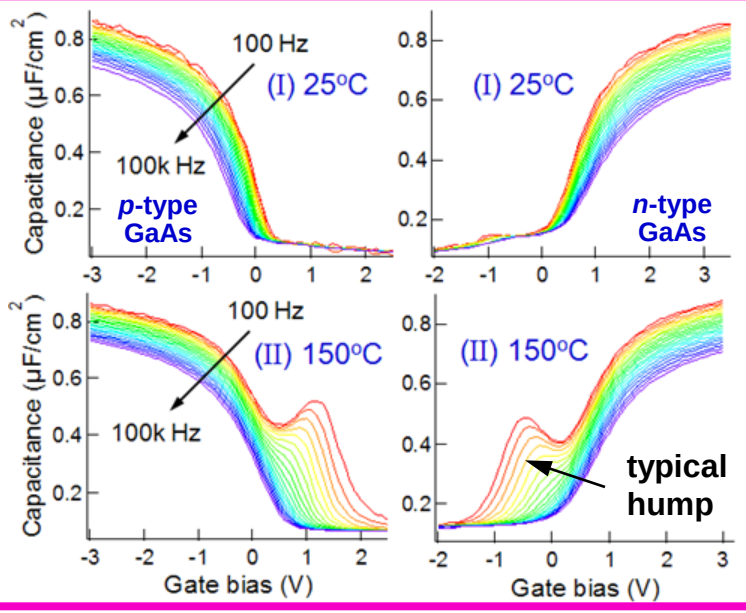
Impact of *Post-Deposition-Annealing*



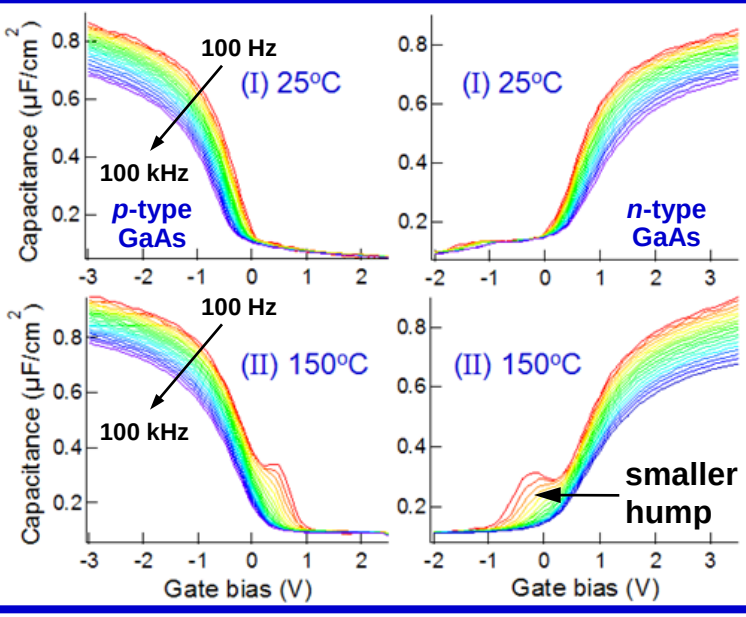
Same trend of annealing effect on *n*-type GaAs substrates

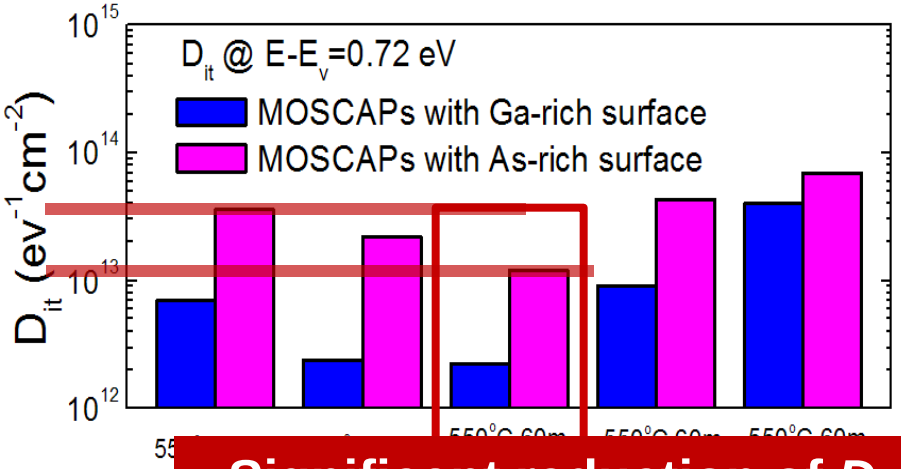
Impact of **Initial Surface Reconstruction**

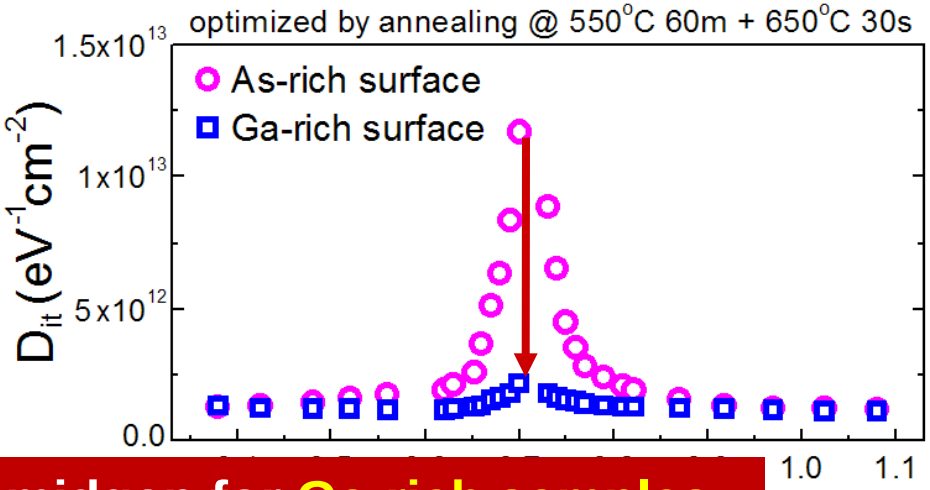
As-rich reconstruction: c(4x4)



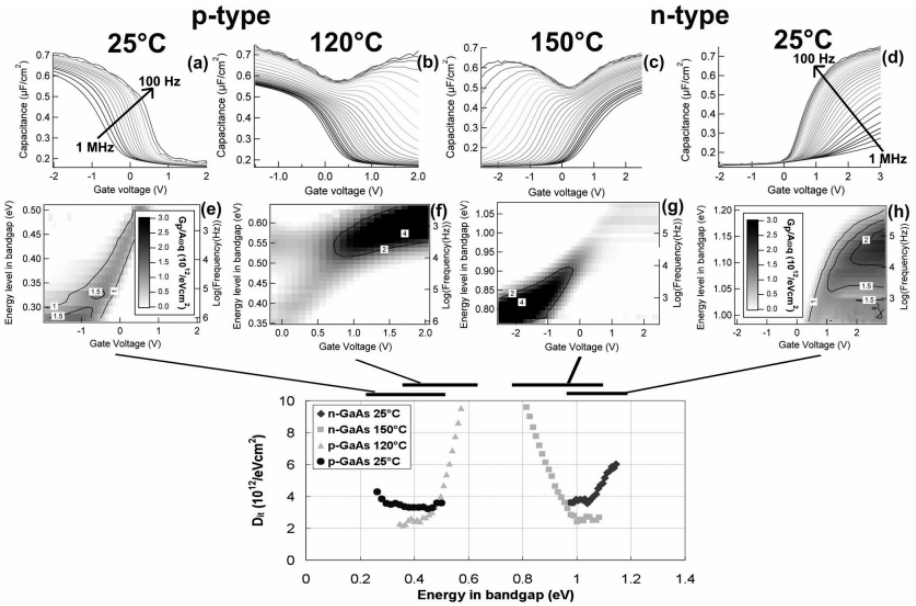
Ga-rich reconstruction: 4x6





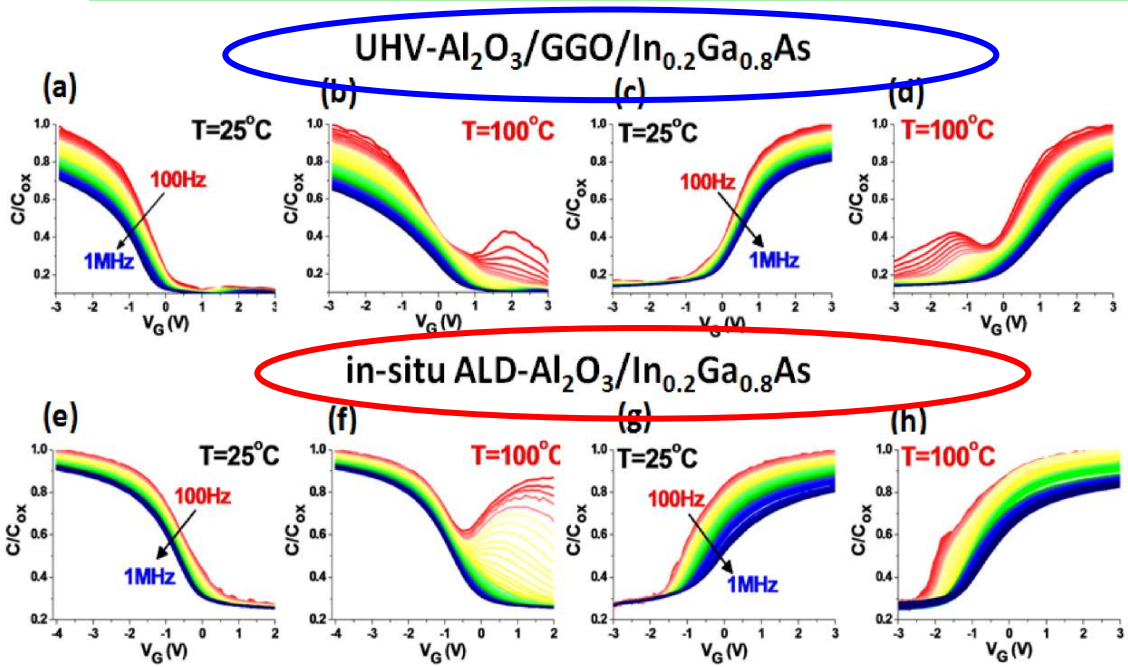


Significant reduction of D_{it} at midgap for Ga-rich samples

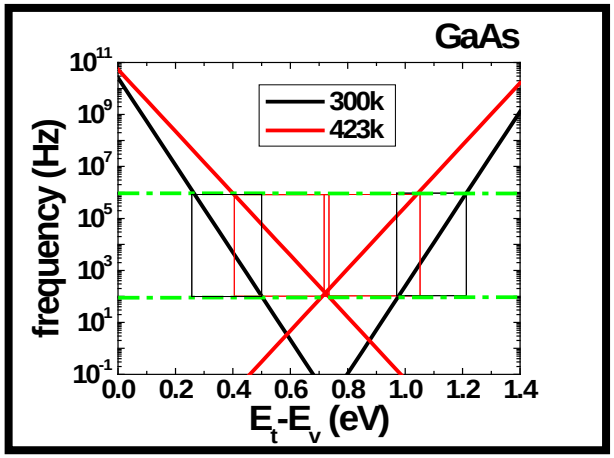


D_{it} spectrum for ALD-Al_2O_3/GaAs with HCl clean
(G. Brammertz *et al*, Appl. Phys. Lett. **93**, 183504 (2008))

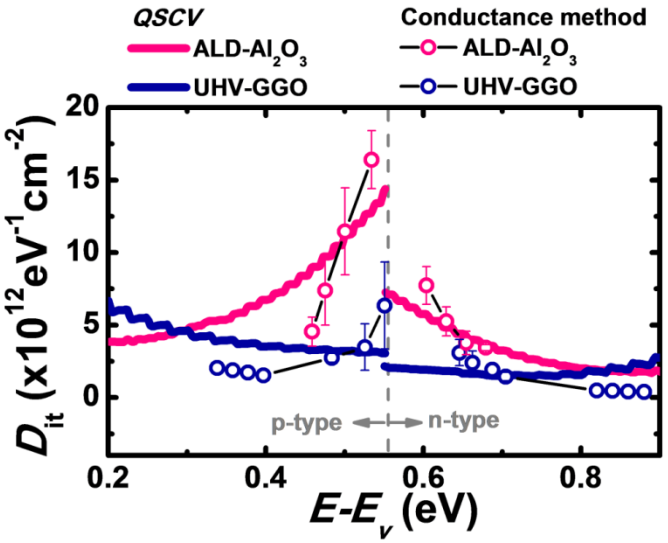
D_{it} distribution – *Conductance method*



$$\tau = \frac{1}{2\pi f} = \frac{\exp(\Delta E / kT)}{\sigma v_t N}$$



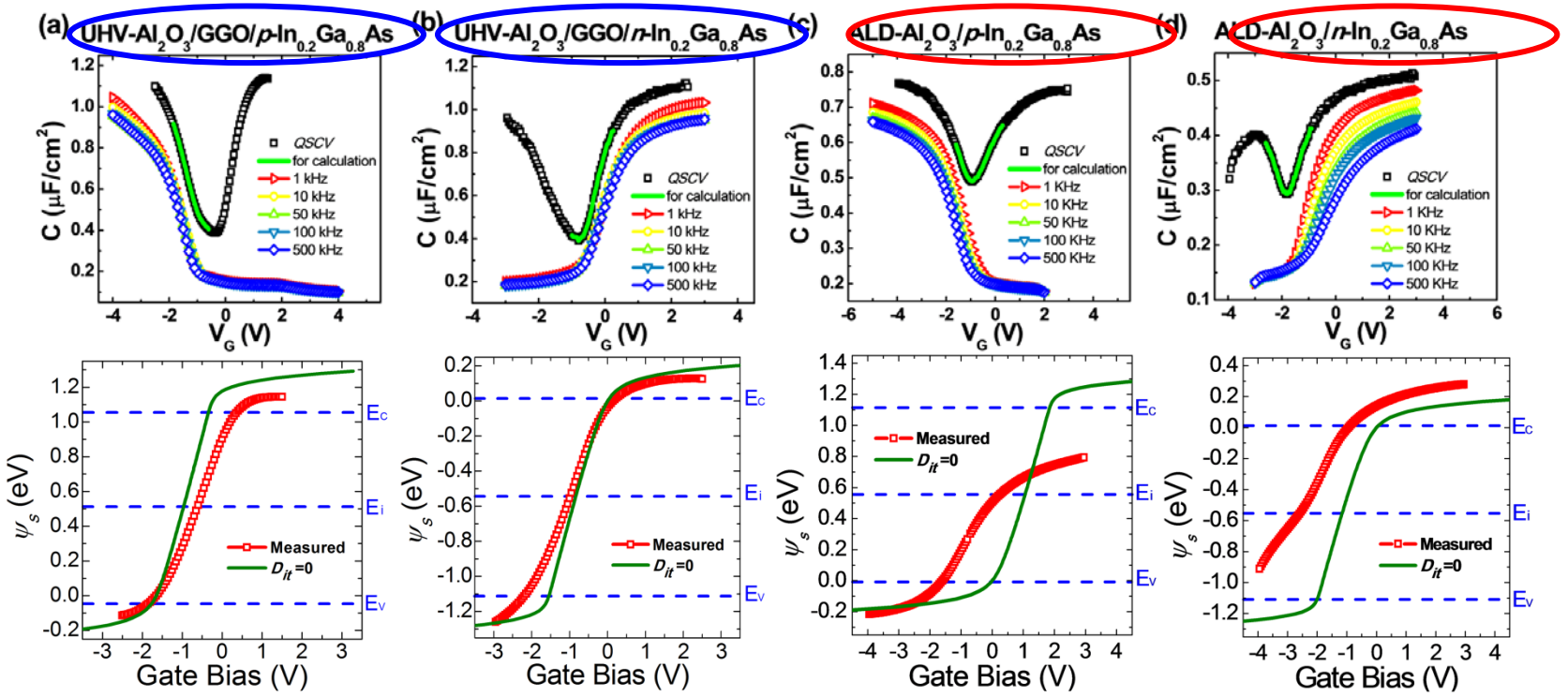
Mid-gap D_{it}'s from conductance measured at high temperatures (G. Brammertz et al, IMEC)

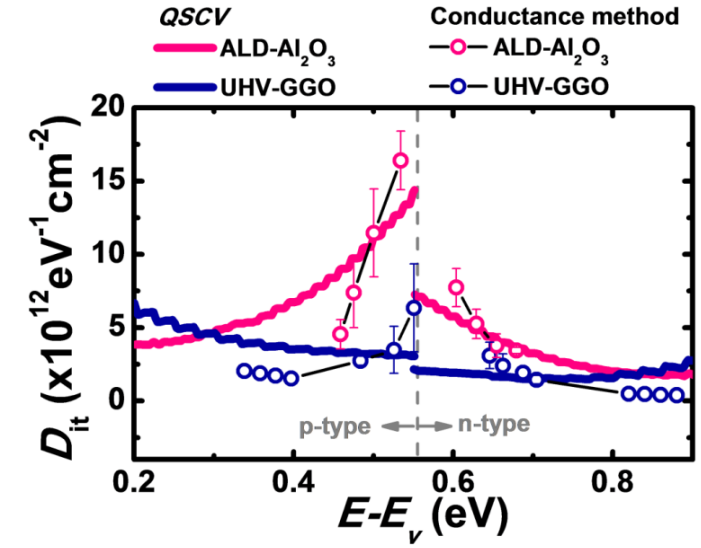


1. D_{it} spectra derived using both *QSCV* and temperature-dependent conductance method;
2. both UHV-Al_2O_3/Ga_2O_3(Gd_2O_3)/ and ALD-Al_2O_3/*n*- and *p*-$In_{0.2}Ga_{0.8}As$ MOSCAPs were investigated;
3. ALD-Al_2O_3/$In_{0.2}Ga_{0.8}As$ interface shows a high mid-gap D_{it} peak spectrum;
4. no discernible D_{it} peak for UHV-Ga_2O_3(Gd_2O_3)/$In_{0.2}Ga_{0.8}As$ interface

C.A. Lin et al., Appl. Phys. Lett., 98, 062108 (2011)

D_{it} distribution – *calculation from QS-CV method*





Berglund's integral

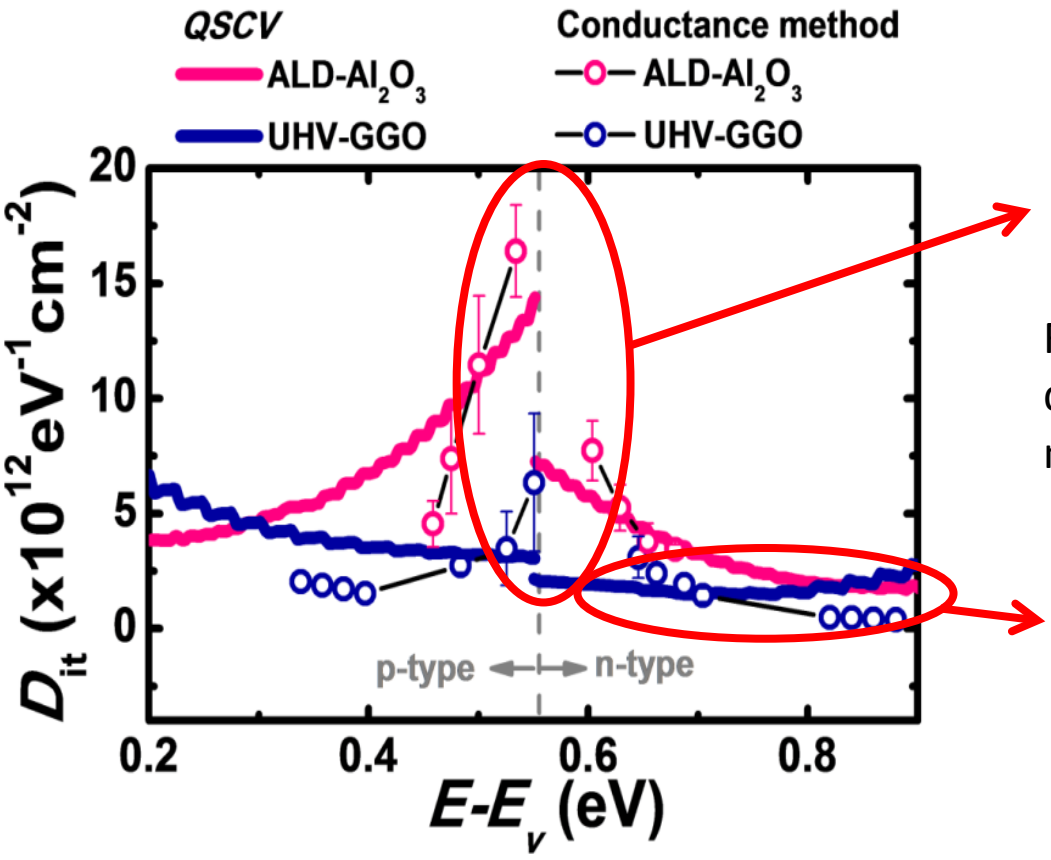
$$\psi_s = \int \left(1 - \frac{C(V_G)}{C_{ox}}\right) dV_G$$

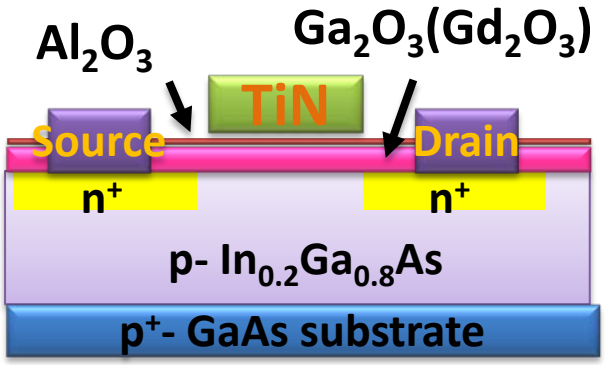
$$D_{it} = \frac{C_{ox}}{q^2}\left[\left(\frac{d\psi}{dV_G}\right)^{-1} - 1\right] - \frac{C_D}{q^2} = \frac{C_{ox}}{q^2}\frac{d\left(V_G(\psi) - V_G^0(\psi)\right)}{d\psi}$$

1. a gradual trending down of D_{it} from E_v to E_c;
2. a mean D_{it} ~10^{12} $eV^{-1}cm^{-2}$ near the mid-gap of $In_{0.2}Ga_{0.8}As$ with no discernible peak

C.A. Lin et al., Appl. Phys. Lett., 98, 062108 (2011)

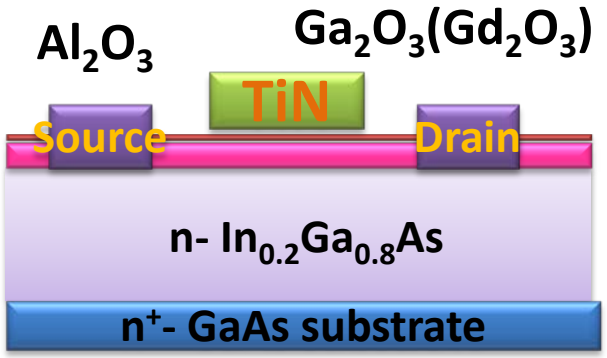
Impact of D_{it} on Device Performance





Inversion channel MOSFET

Fermi level near E_v should be driven across mid-gap to generate minority carriers



Depletion-mode MOSFET

Fermi level near E_c should be driven back to mid-gap to deplete channel

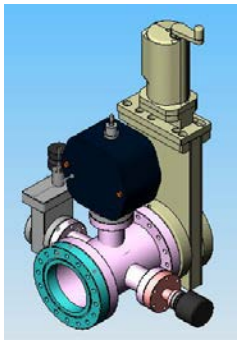
In situ growth and analysis of oxide/III-V interfaces

✓ *In-situ* ALD- & MBE-oxides on freshly MBE grown InGaAs surfaces

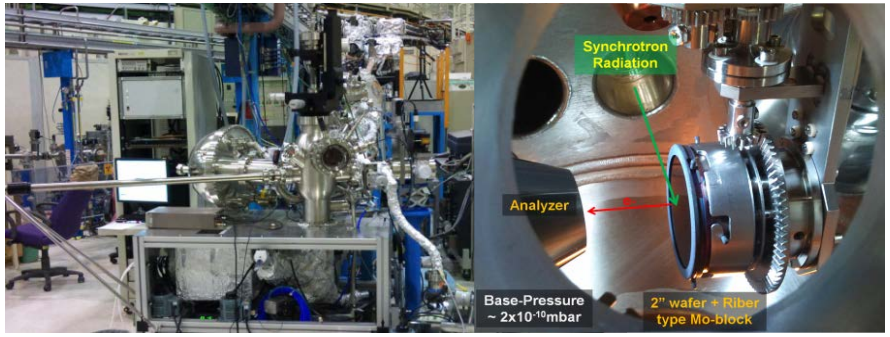
✓ Portable UHV chamber for 2”wafer (Pressure < $3x10^{-10}$ torr)

✓ *In-situ* high resolution synchrotron radiation photoemission analysis

In-situ MBE/ALD/XPS/STM

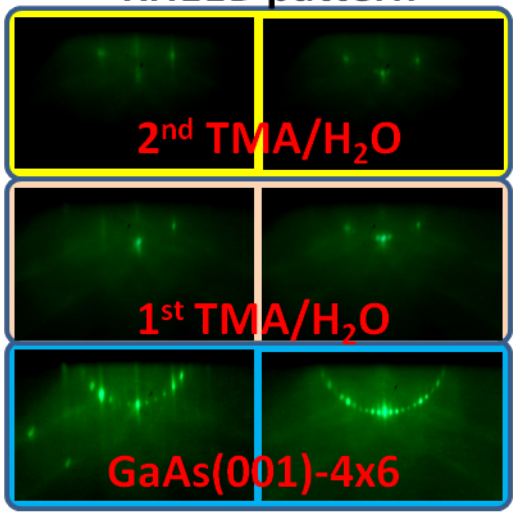


Portable UHV chamber

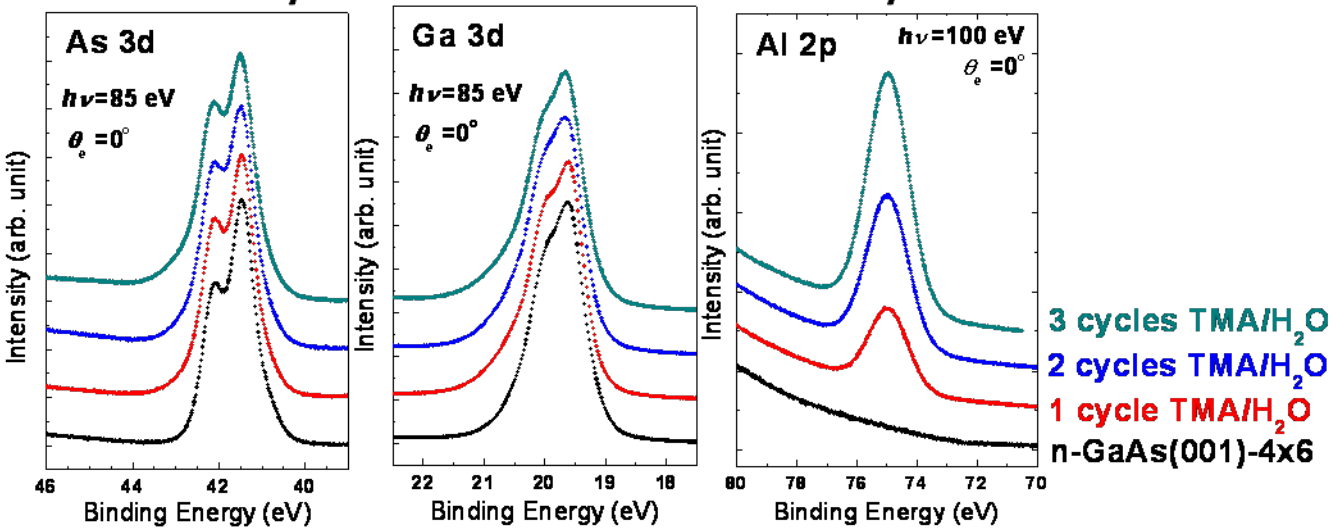


In-situ synchrotron radiation XPS analysis

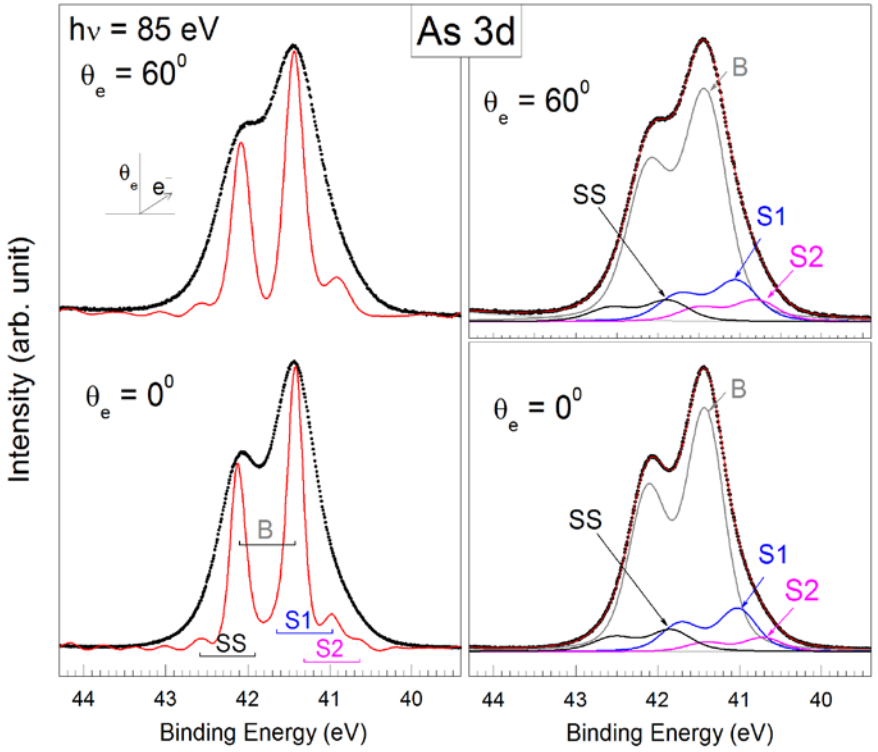
RHEED pattern



In situ synchrotron radiation-XPS analyses



In-situ ALD-Al_2O_3 on Ga-rich n-GaAs(001)-4x6 surface: A synchrotron-radiation photoemission study

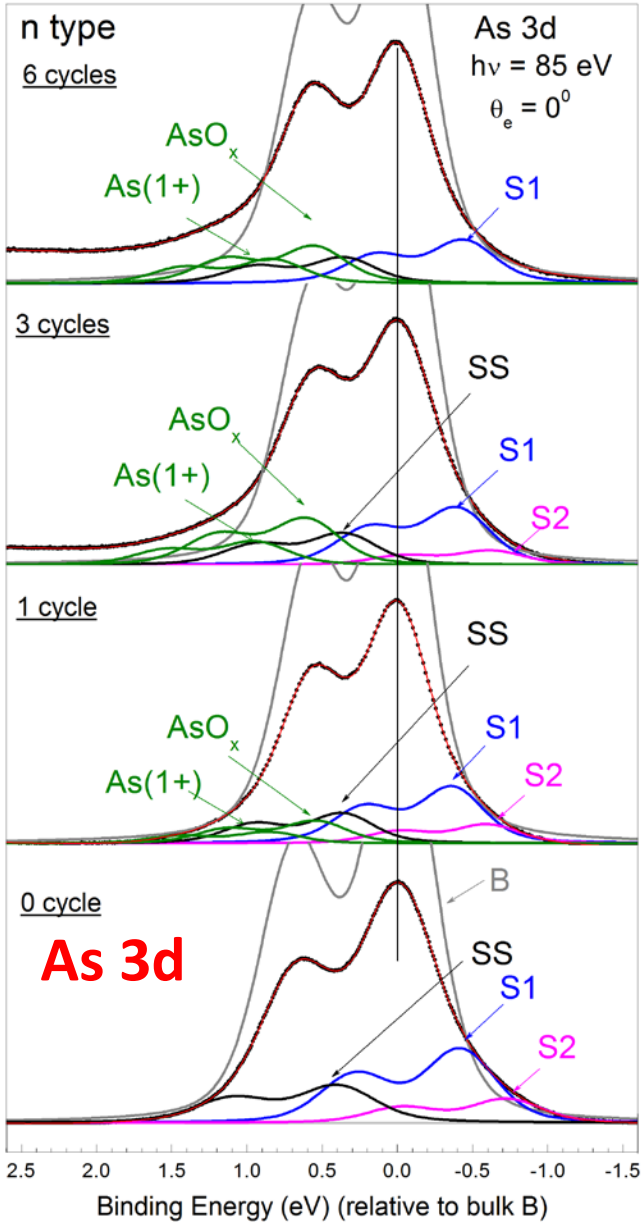


(a) As 3d core level spectra of the clean GaAs(001)-4x6 surface taken with hn = 85 eV in normal and 60^0 off-normal emission. The line represents a de-convoution of the curve. (b) An analytical fit to the spectra plotted in (a).

Symbols B, SS, S1, and S2 stand for the doublets of bulk, the subsurface, the surface As atoms at the faulted position, and the As in the surface As-Ga dimer.

In situ ALD-Al_2O_3/GaAs(001) interfaces: cycle by cycle analyses

Y. H. Chang et al, Microelectronic Engineering 88, 1101 (2011)



TMA/H_2O: 6 cycles

S1 : can not be passivated completely

S2: peak disappeared

As(1+), AsOx: exist at interface

TMA/H_2O: 3 cycles

S1, S2 peak ↓

As(1+), AsOx ↑

***No As-As at the ALD-Al_2O_3/GaAs interface**

TMA/H_2O: 1 cycles

S1, S2 peak ↓

As(1+): S1 As bond to O-Al (As-O-Al)

AsOx: S2 As bond to Al-O(As-Al-O)

Clean GaAs(001)-4x6

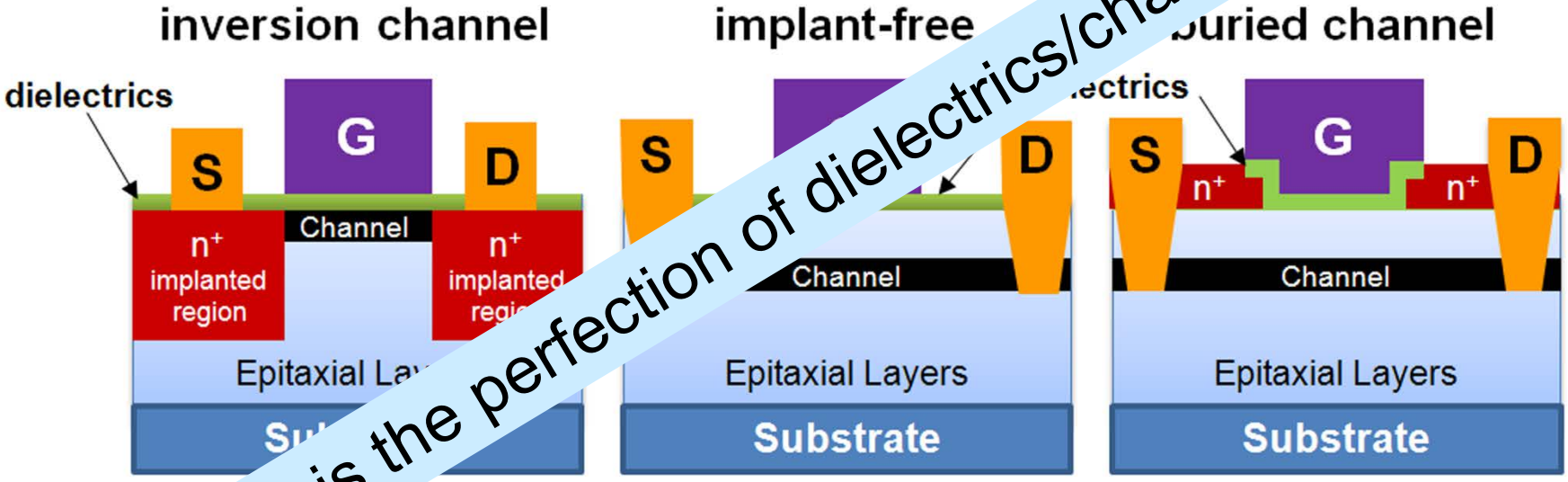
Surface-related doublet peak

S1: As in the faulted position (-380meV), excess charge

S2: As in As-Ga dimer (-652meV), excess charge

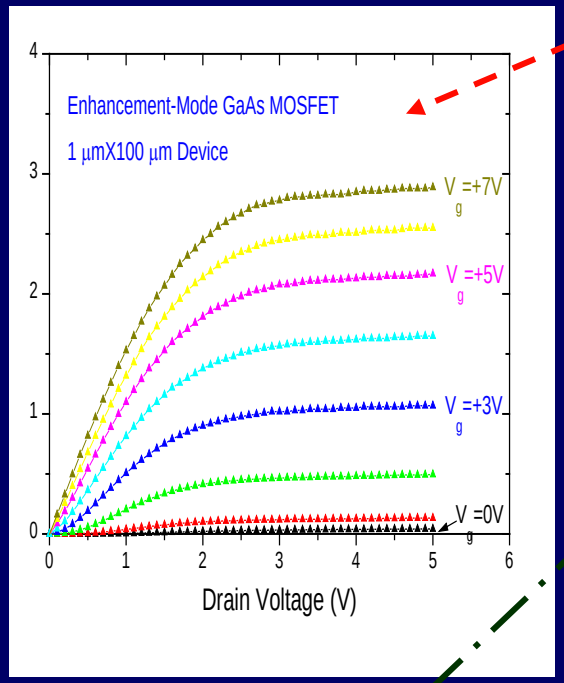
SS: As-As dimer in the subsurface layer (+338meV)

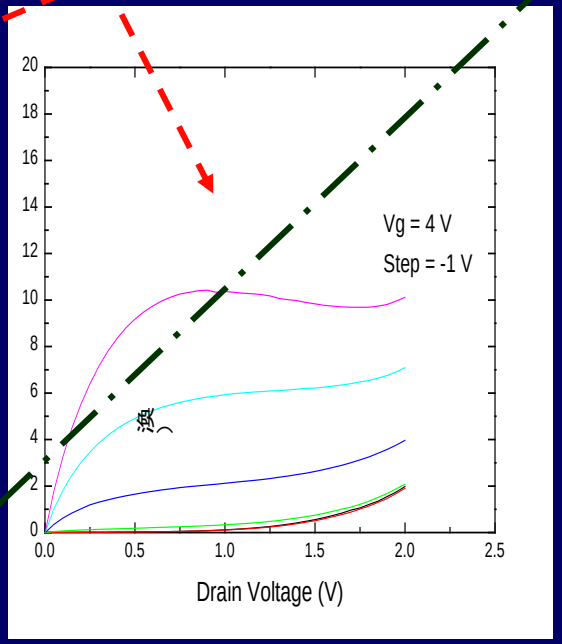
Enhancement-mode devices

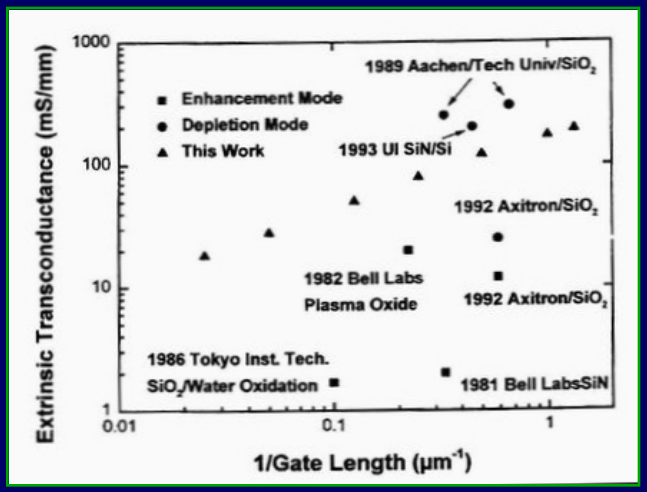


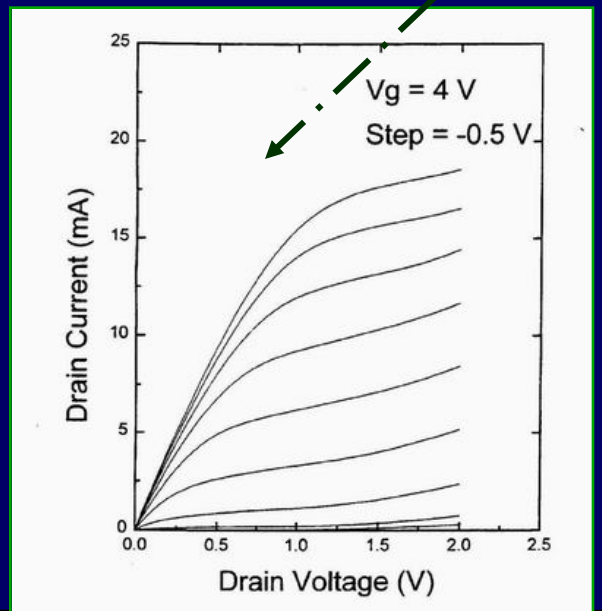
The key is the perfection of dielectrics/channel interface

Inversion channel n-GaAs and n-InGaAs/InP MOSFET



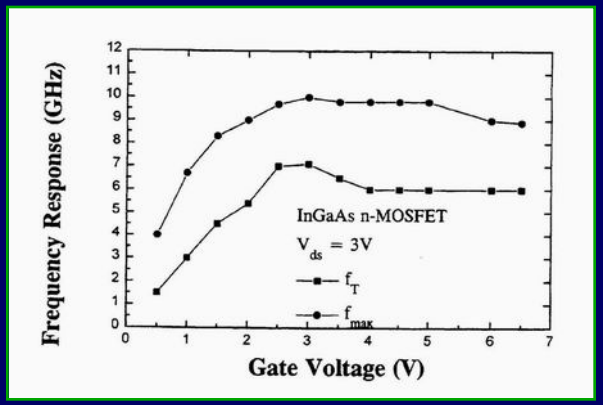


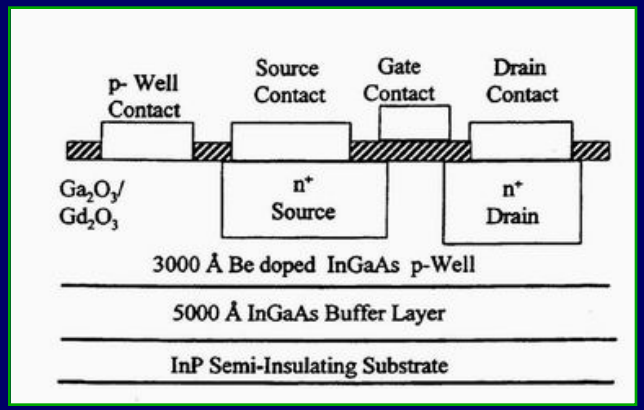




Drain current drive capability improved over 100 times

Due to the improved oxide quality and device fabrication



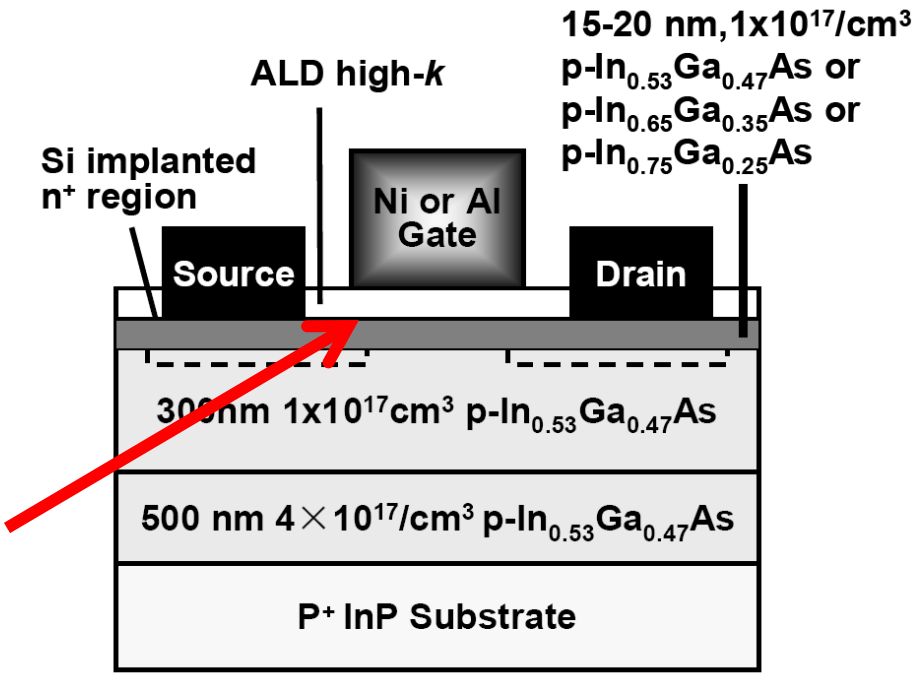


- 0.75 x 50 μm²
- g_m = 190 mS/mm
- f_T = 7 GHz
- f_{max} = 10 GHz
- μ = 470 cm²/Vs

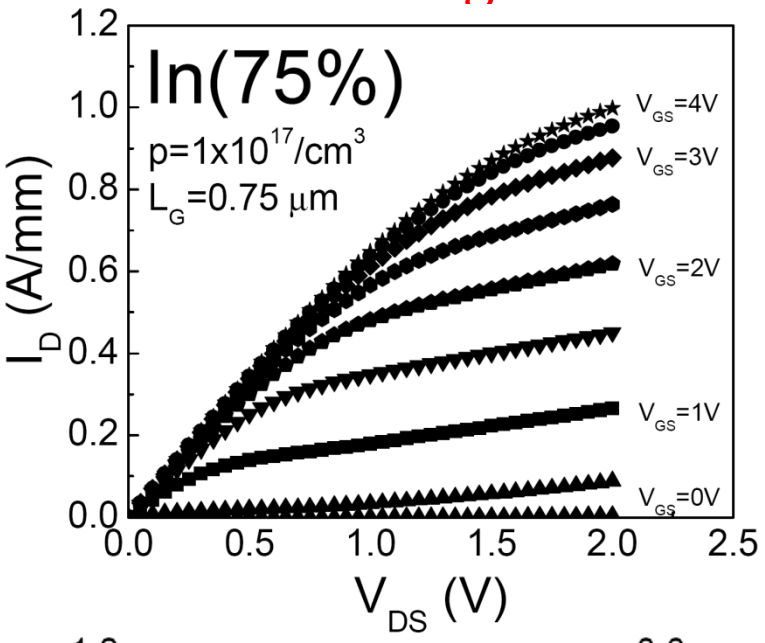
Ren et al, IEDM 1996, SSE 1997, EDL 1997

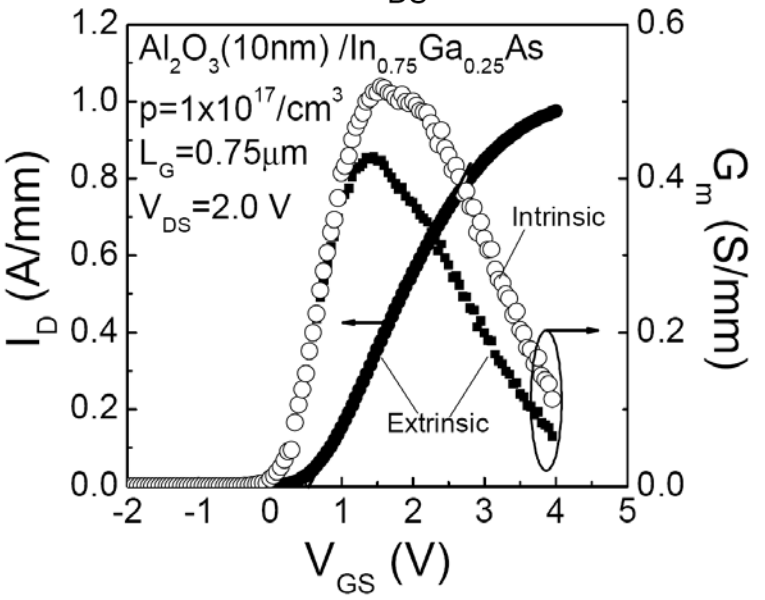
Wang et al, 1999

Surface channel InGaAs MOSFET with non-self-aligned Process



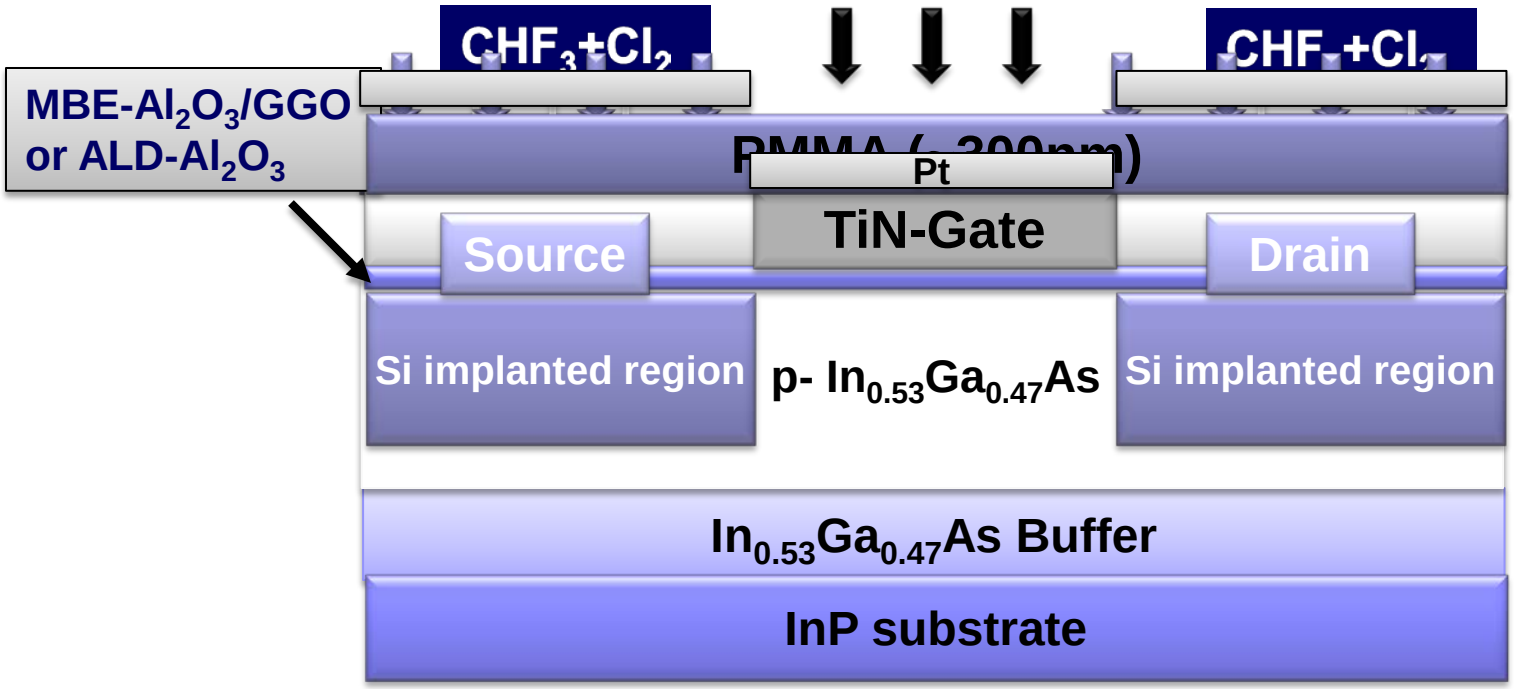
1) NH_4OH surface pretreatment
2) ALD Al_2O_3 30nm as an encapsulation layer
2) S/D patterning and Si implantation (30KeV/1E14 & 80KeV/1E14)
3) S/D activation using RTA (700-800°C 10s in N_2)
4) ALD re-growth: Al_2O_3
5) PDA: 400-600°C 30s in N_2
6) S/D contact patterning and Au/Ge/Ni ohmic metal evaporation and 400°C metallization
7) Gate patterning and Ni/Au or Al/Au evaporation





Y. Xuan et al., IEDM, p. 371, (2008)

Self-aligned inversion-channel InGaAs MOSFET

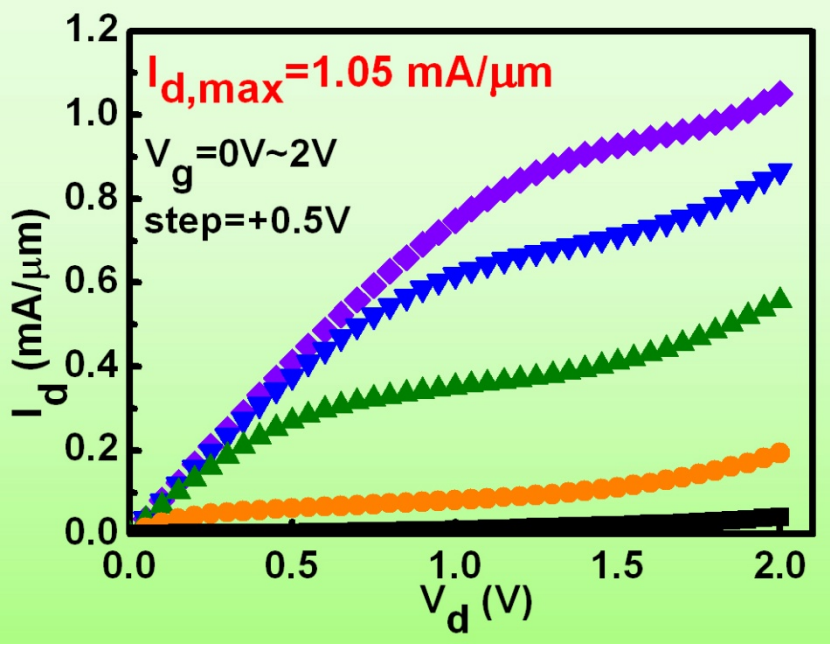


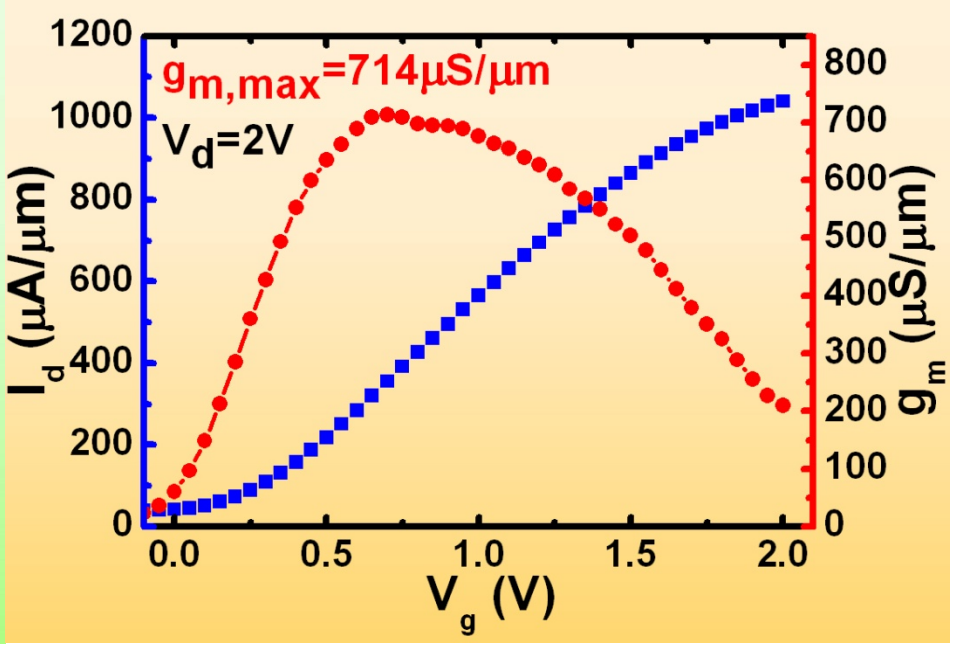
1. TiN sputtering
2. PMMA coating, E-beam writing, and hard mask deposition
3. Dry-etching
4. S/D patterning, implantation & activation
5. S/D contact region patterning, wet-etching of oxide, contact metal deposition, lift-off & ohmic alloying

Output & Sub-threshold Characteristics

T. D. Lin et al, APL 93 033516 (2008)

Self-aligned inversion-channel TiN/Al_2O_3/GGO/$In_{0.53}Ga_{0.47}As$/InP MOSFET

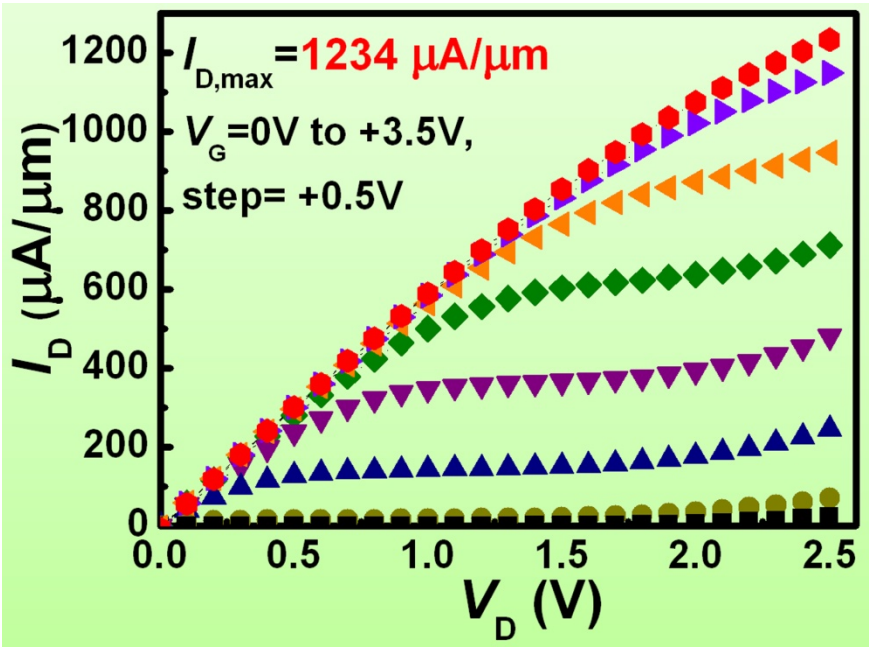


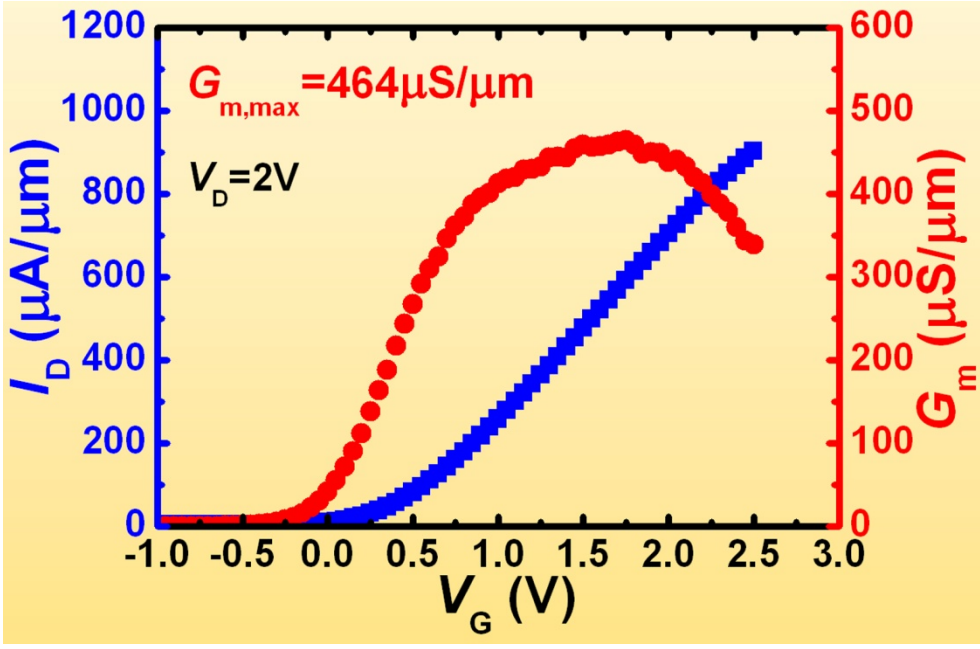


1. t_{TiN}= 160nm, $t_{Al_2O_3}$=2nm, t_{GGO}=5nm, W/L=10/1μm
2. $I_{d,max}$=1.05 mA/μm @V_g=2V, V_d=2V
3. $g_{m,max}$=714 μS/μm @V_g=0.7V, V_d=2V
4. V_{th}~0.2V, μ_{FE}=1300 $cm^2/V{\cdot}s$ (from transconductance analysis)

Si NMOSFET
90nm node
L_g~45nm
$I_{d,sat}$~1 mA/μm

UHV- Al_2O_3/GGO/$In_{0.75}Ga_{0.25}As$/InP MOSFET





- t_{TiN}= 200nm, $t_{Al_2O_3}$=3nm, t_{GGO}=6nm, W/L=10/1μm
- $I_{D,max}$=1.23 mA/μm @V_G=3.5V, V_D=2.5V
- $G_{m,max}$=464 μS/μm @V_G=1.75V, V_D=2V
- V_{th}~0.25V, μ_{FE}=1600 $cm^2/V{\cdot}s$ (from transconductance analysis)

T. D. Lin et al., Solid-State Electron. 54 (2010) 915.
39th ESSDERC, Athens, Greece

E-mode III-V MOSFETs

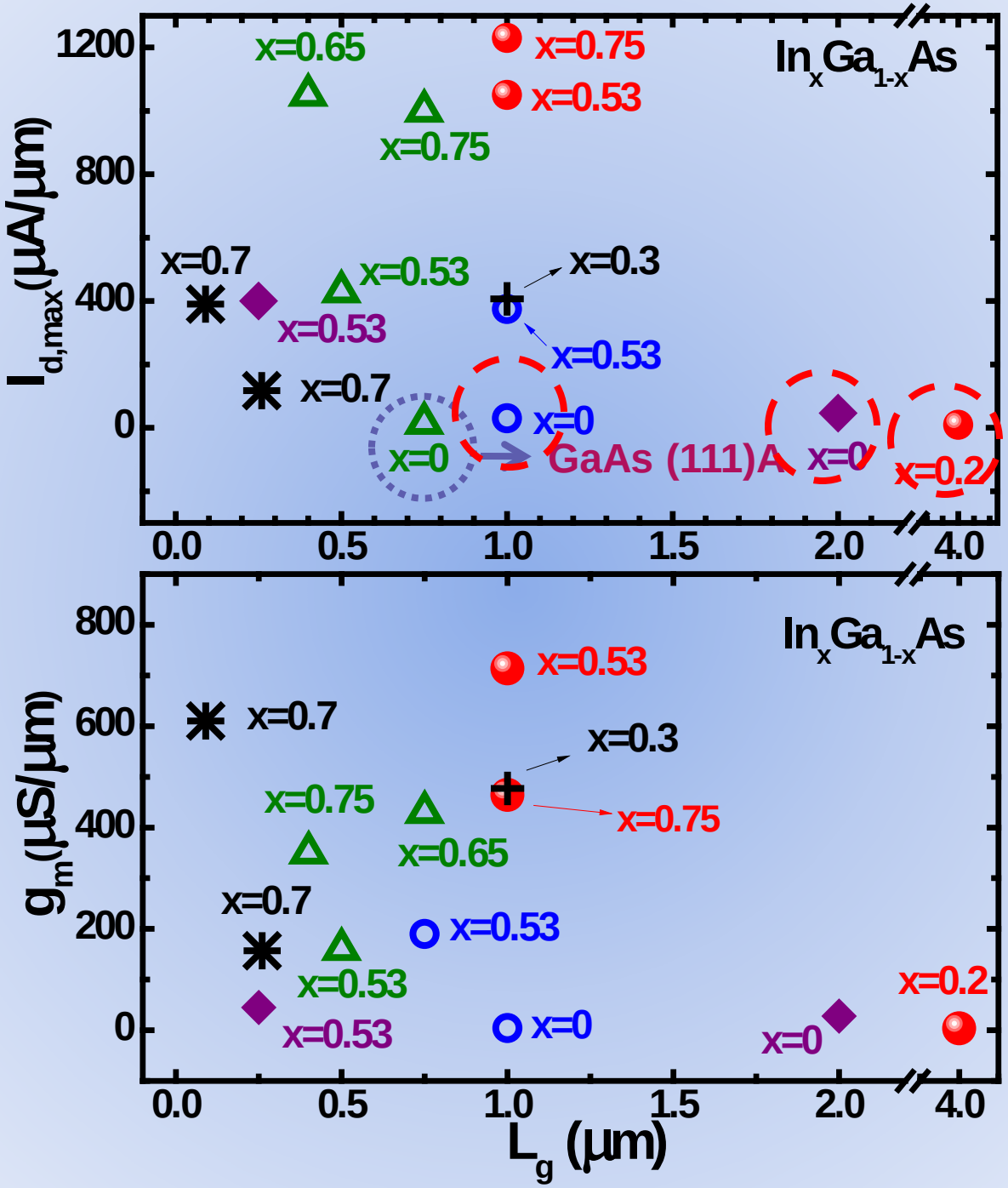
Benchmark

- Natl Tsing-Hua Univ.
- Univ. Singapore
- Bell Labs
- Purdue Univ.
- Freescale Univ. Glasgow
- IBM

MBE-Al_2O_3/GGO/$In_{0.75}Ga_{0.25}As$
L_g=1μm
I_D= 1.23 mA/μm,
G_m= 464 μS/μm
T. D. Lin et al., SSE, (2010)

MBE-Al_2O_3/GGO/$In_{0.53}Ga_{0.47}As$
L_g=1μm
I_D= 1.05 mA/μm
G_m= 714 μS/μm
T. D. Lin et al., APL 93, 033516 (2008)

MBE-Al_2O_3/GGO/$In_{0.2}Ga_{0.8}As$
L_g=4μm
I_D= 9.5 μA/μm
G_m= 3.9 μS/μm

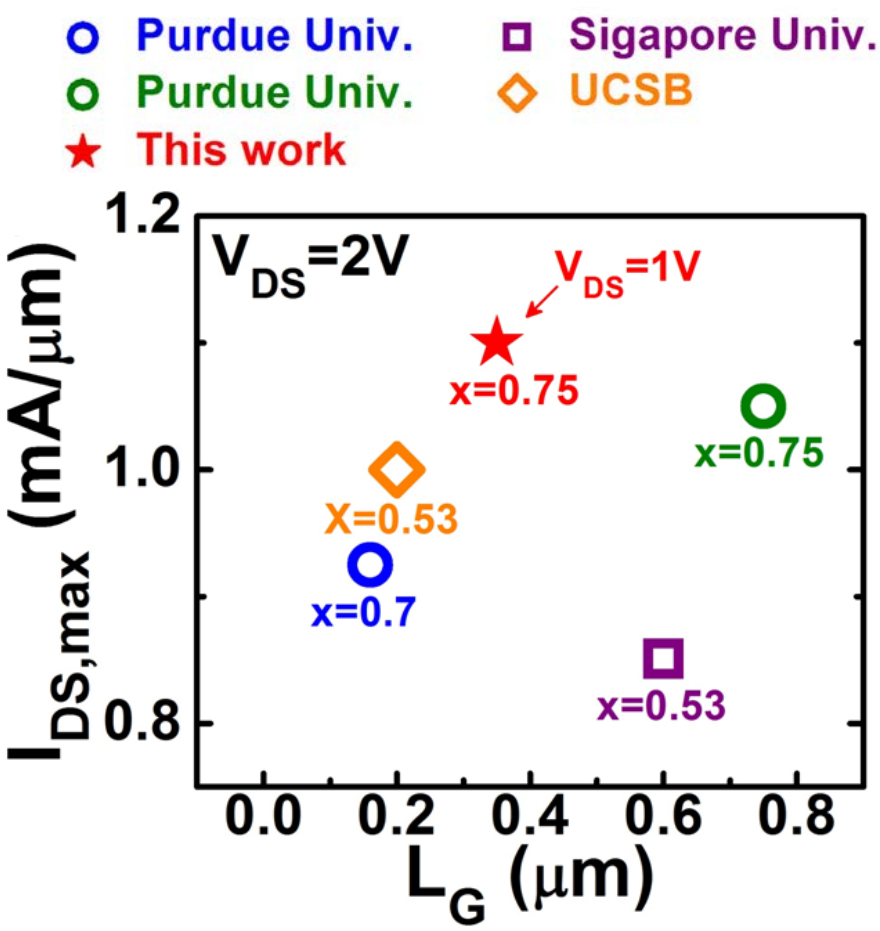


Conclusion

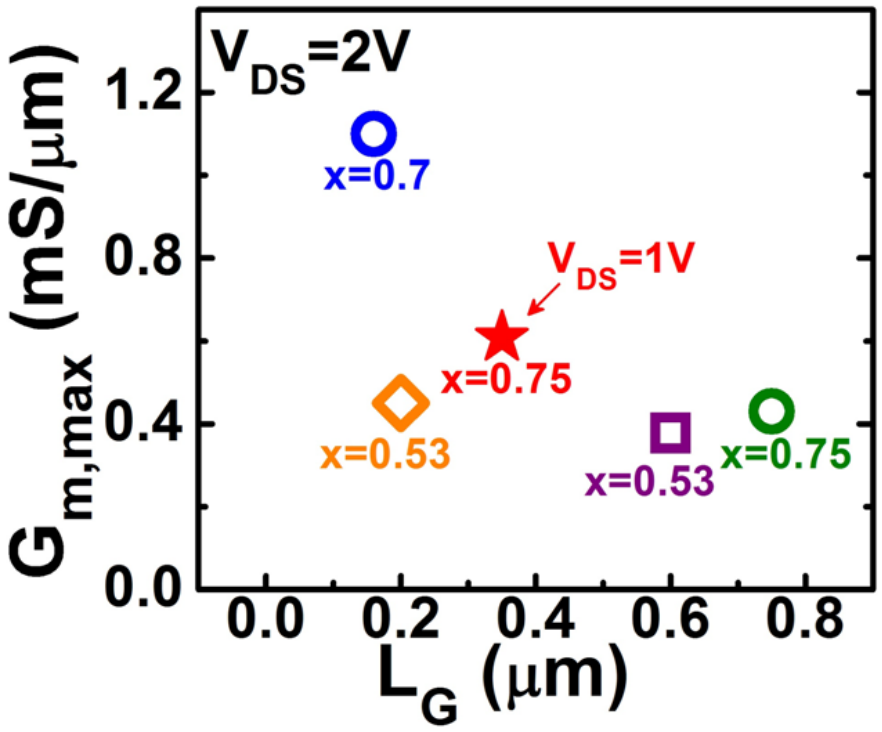
- Perfecting the best atomic-scale hetero-structures and their interfaces in high κ and high carrier mobility semiconductors
- Probing them with the most powerful analytical tools (XPS and x-ray diffraction using synchrotron radiation, *in-situ* XPS, and HR-TEM)
- Producing novel, high-performance electronic devices ready for **beyond Si CMOS**

Benchmark

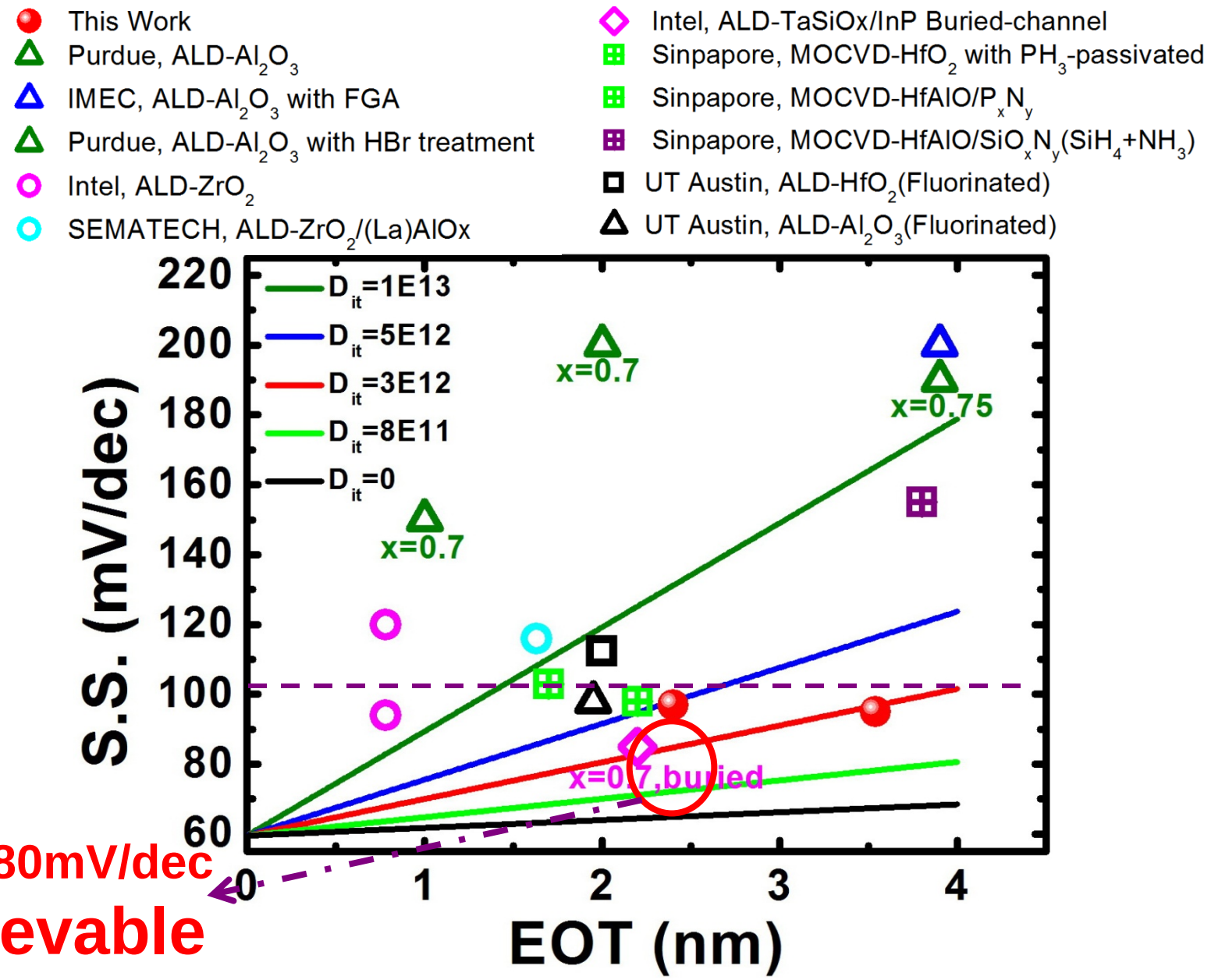
E-mode inversion-channel nMOSFETs with ALD or MOCVD oxide as gate dielectric



*Devices with gate-length < 1μm are included. The number near each data point indicates the In content (x) of the $In_xGa_{1-x}As$ channel.



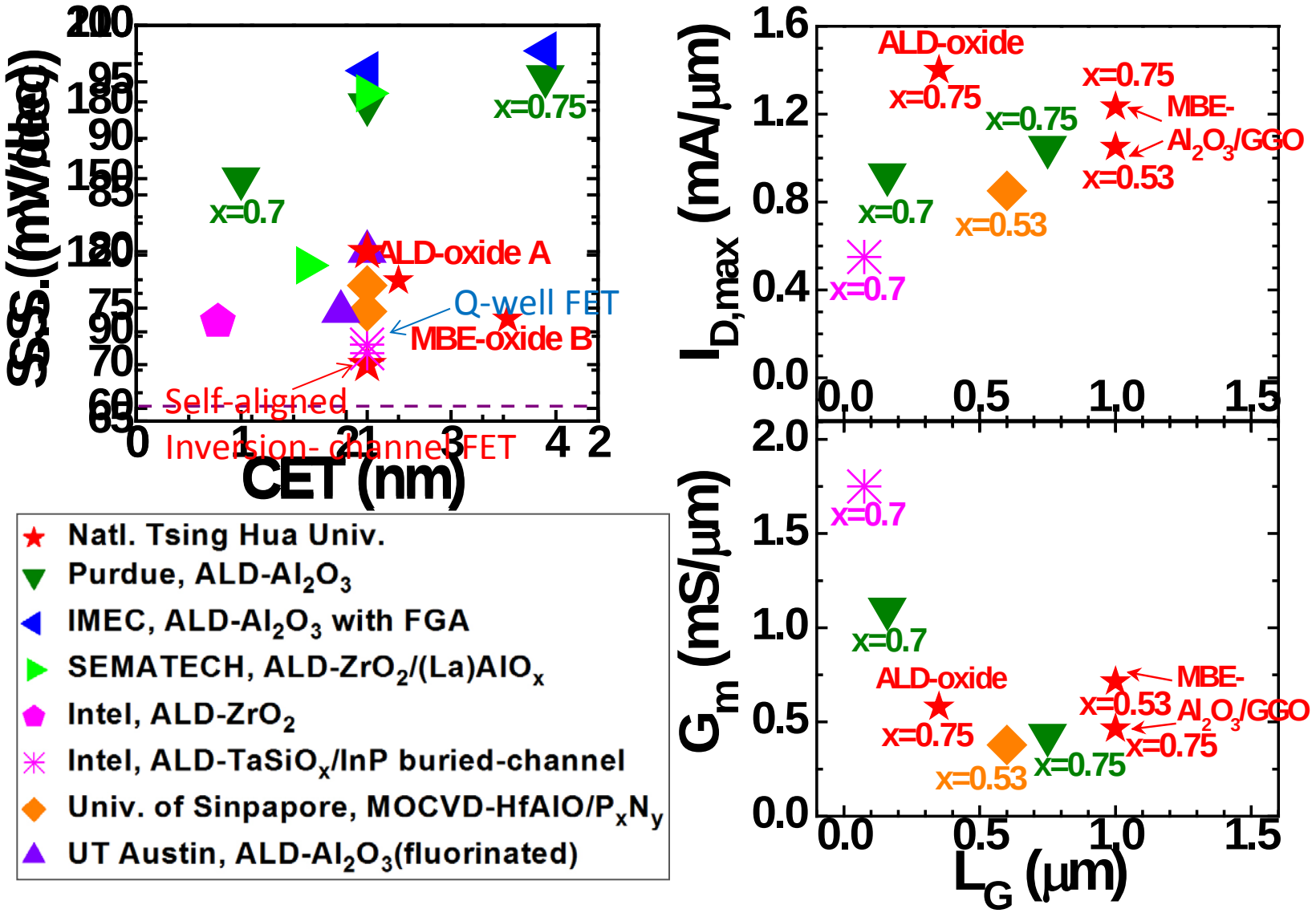
Benchmark



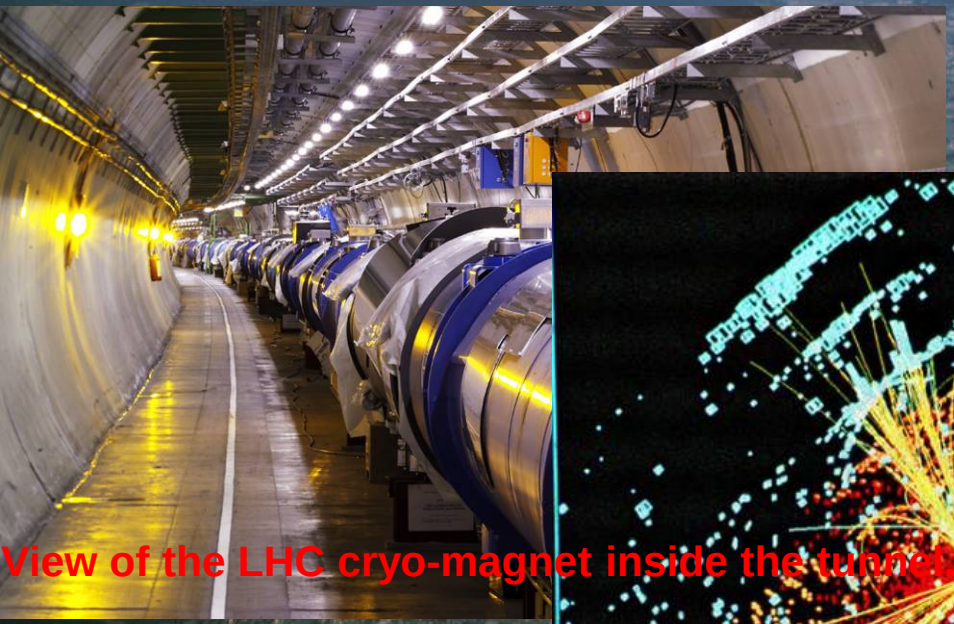
S.S.< 80mV/dec achievable

Benchmark

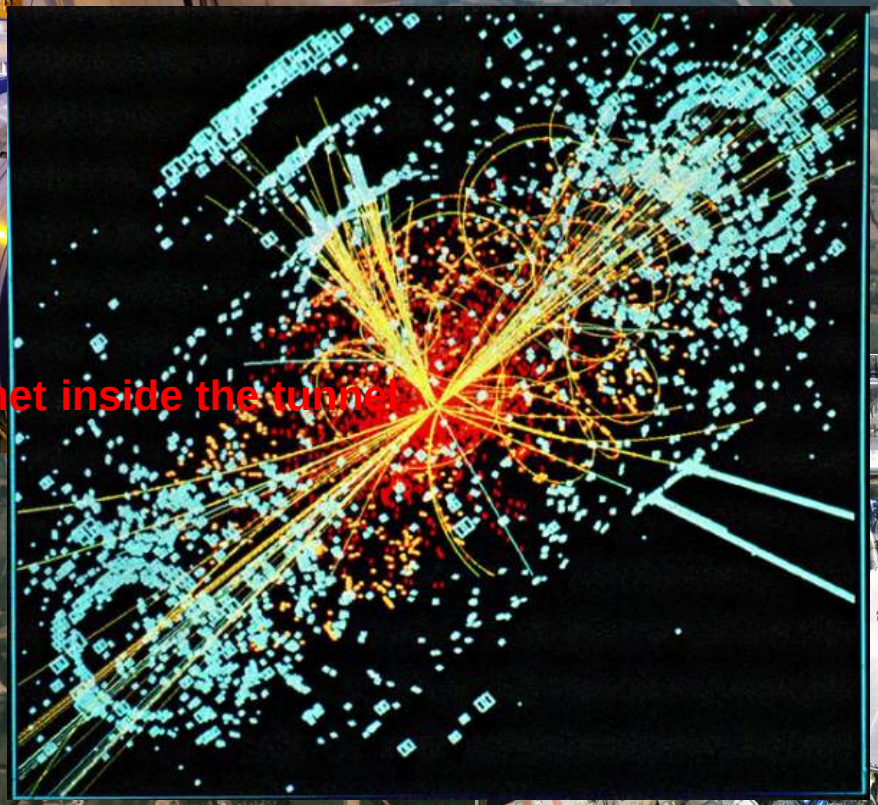
Enhancement-mode $In_xGa_{1-x}As$ MOSFETs

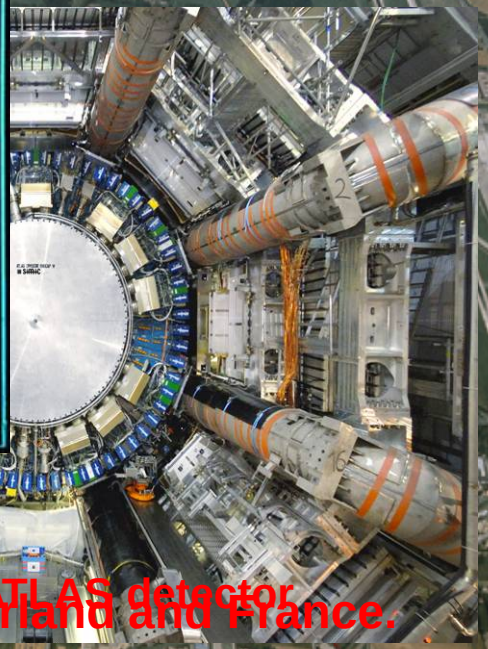


Large Hadron Collider (LHC) Experiment



View of the LHC cryo-magnet inside the tunnel





View of the ATLAS detector

Aerial view of CERN and the surrounding region of Switzerland and France.