

(II) Quantization

Confinement of the materials wave



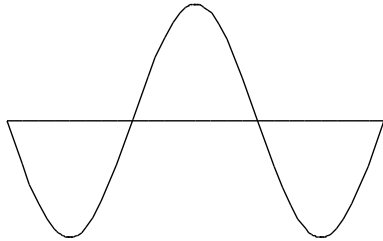
Standing Wave



Quantizations

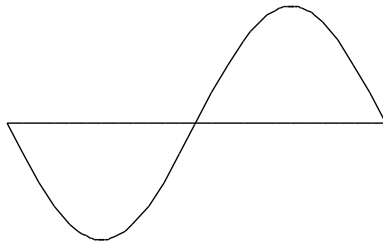
The Quantization of Energy

$n = 3$



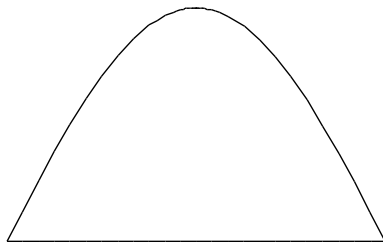
$$L = \frac{n}{2} \lambda$$

$n = 2$



$$p = \frac{h}{\lambda} = \frac{nh}{2L}$$

$n = 1$



$$\delta E \propto 1/L^2$$

$$E_n = \frac{p^2}{2m} = \frac{n^2 h^2}{8mL^2}$$

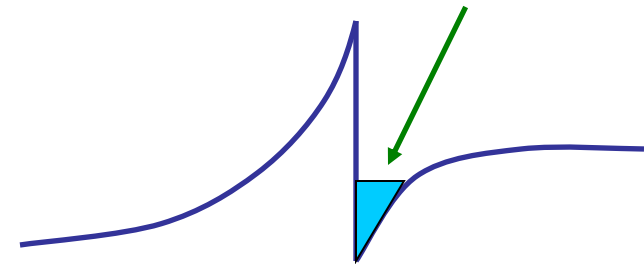
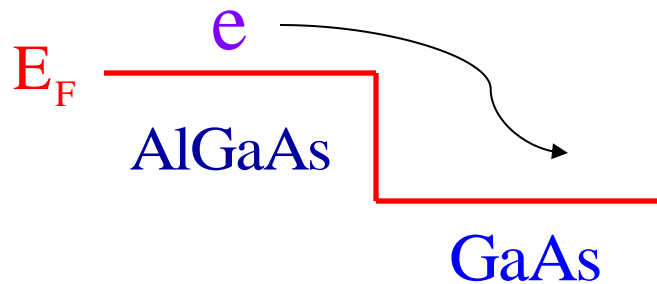
Quantum well: 1D confinement

MOSFET:

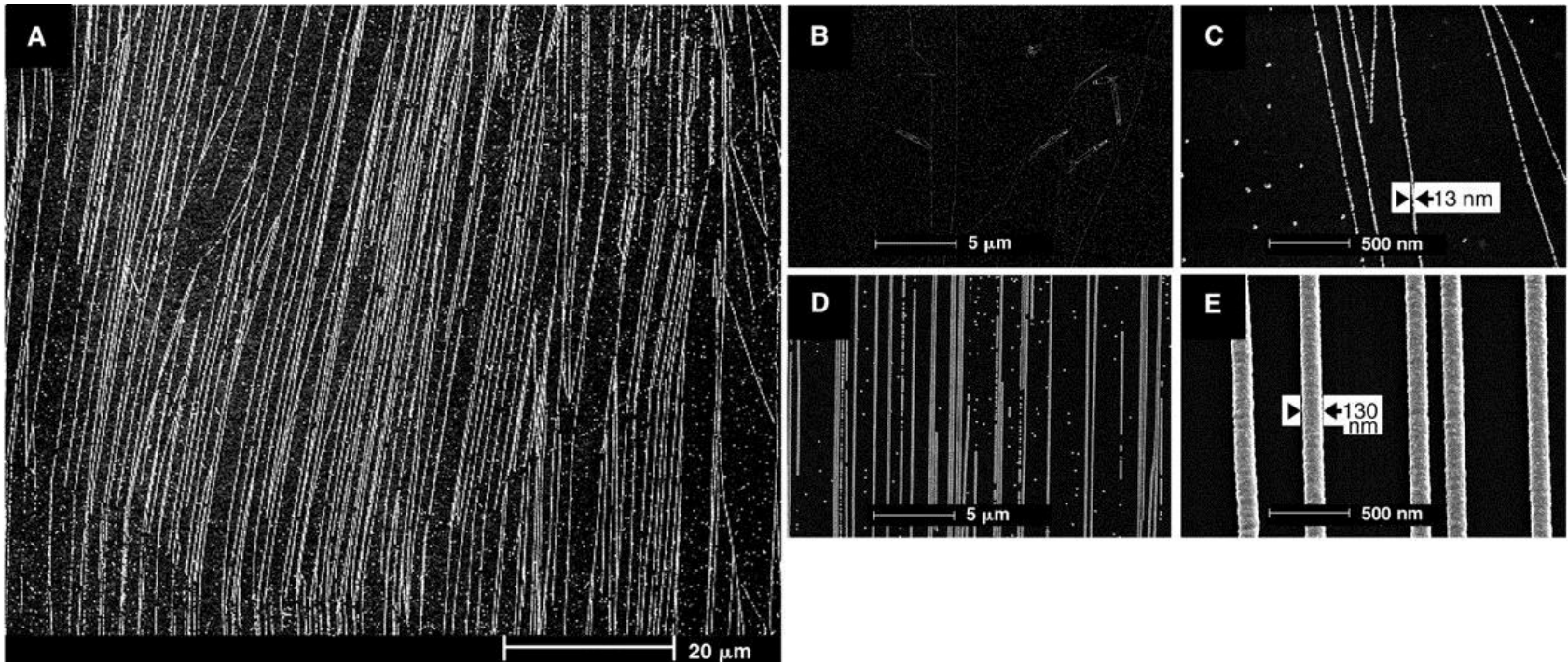


2D electron Gas

二維電子氣

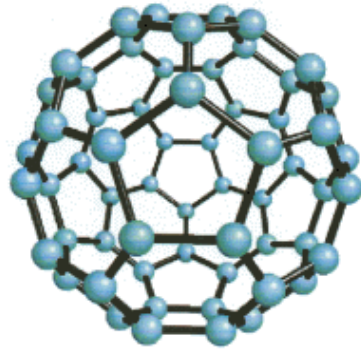


Quantum wire: 2 D-Confinement

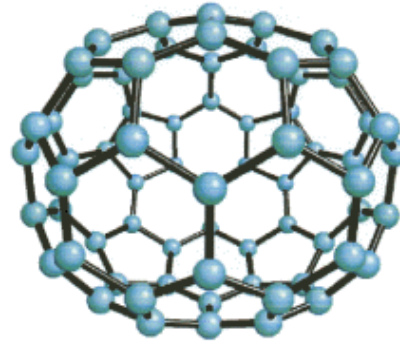


SEM images of MoO_x nanowires on graphite surfaces
Science **290**, 2120-2123, (2000)

Quantum dot: 3 D - Confinement

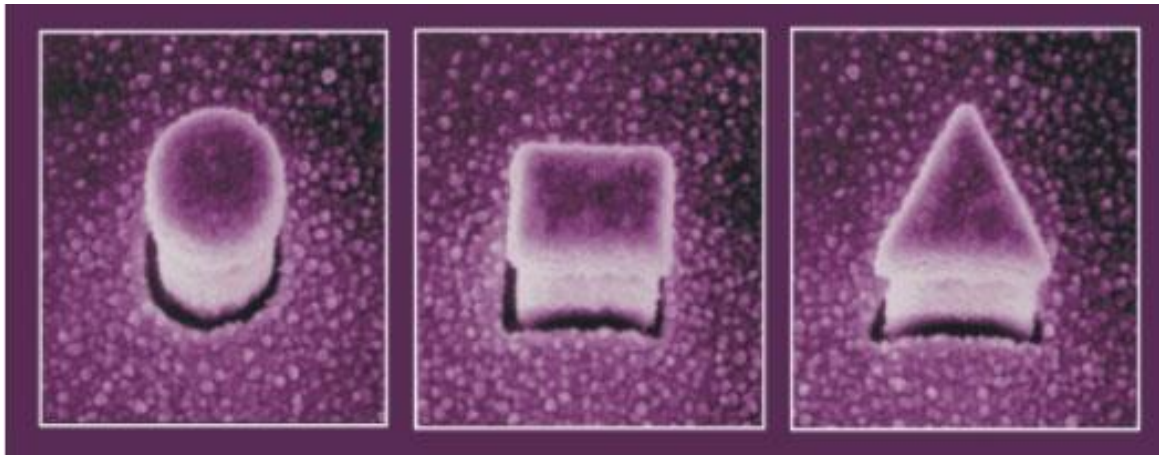
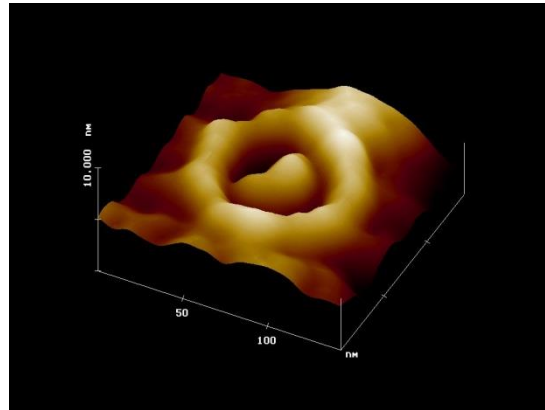


C_{60}



C_{70}

Quantum Dots of various shape



Absorption in scattering
From red to yellow



A diagram showing seven horizontal blue lines representing energy levels. To the right of the lines, a double-headed blue vertical arrow is labeled with the Greek letter λ . To the right of the arrow is the equation $E = hc / \lambda \propto 1 / L^2$.

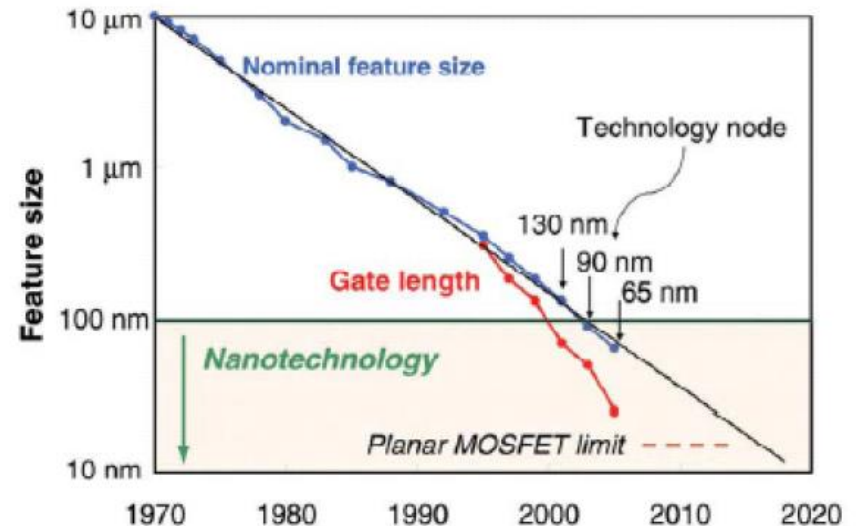
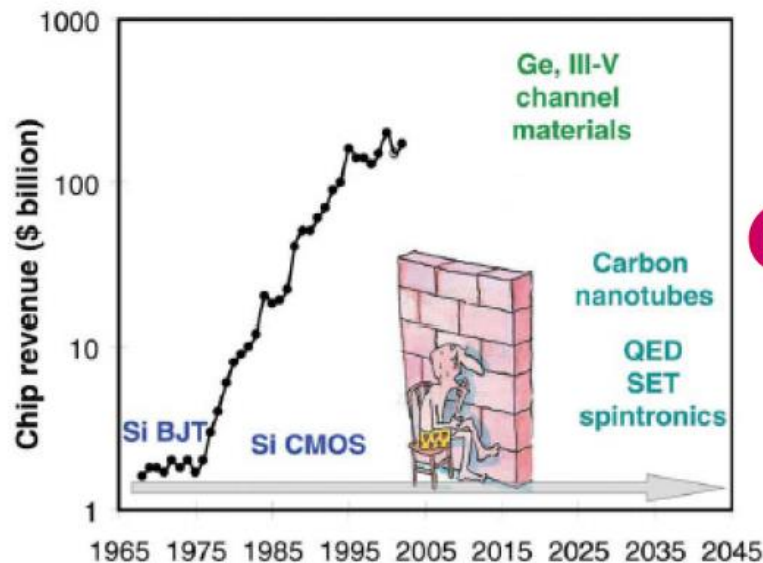
powdered Cadmium Selenide

larger
smaller



Background for search new platform

Scaling limit of Si MOSFET & superparamagnetism



Carbon era?

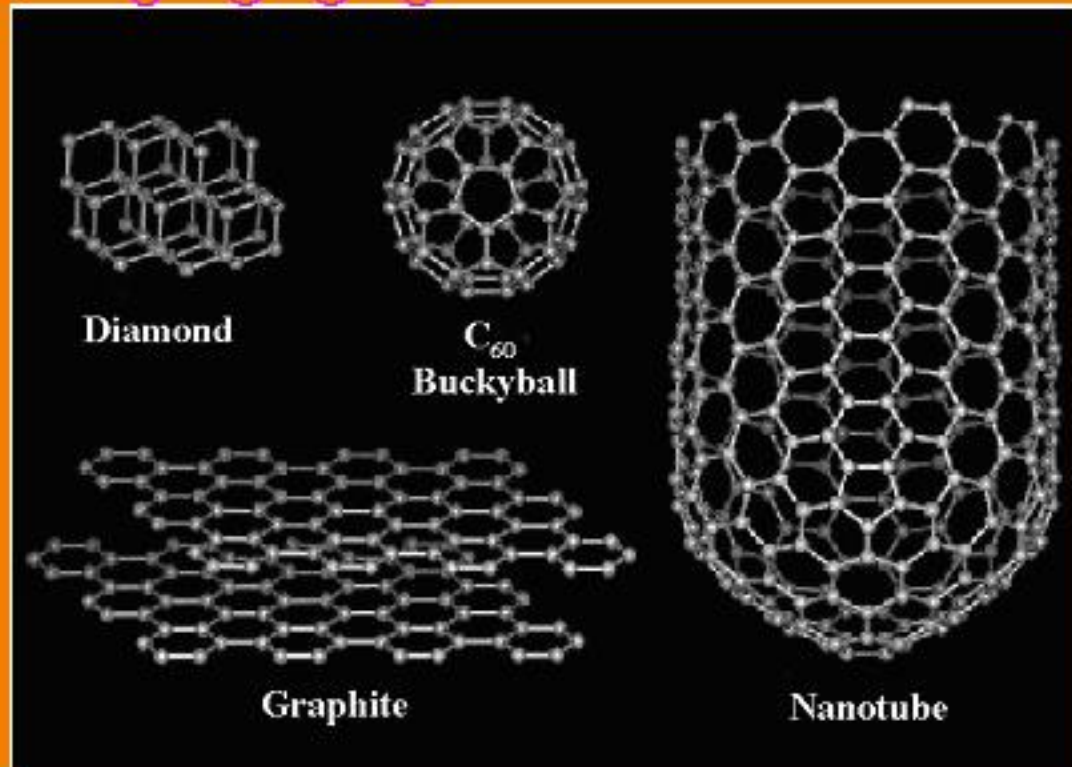
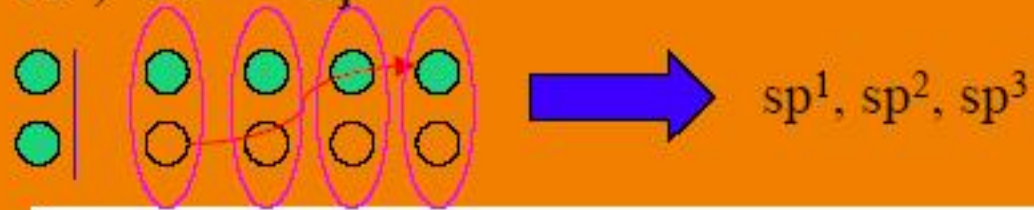
Thompson and Parthasarathy,
Materialstoday 9, 20, 2006

The Advent of Carbon Era ?

Carbon Nanotube

+ Structure of carbon nanotubes

Carbon: $1s^2, 2s^1, 2p^3$

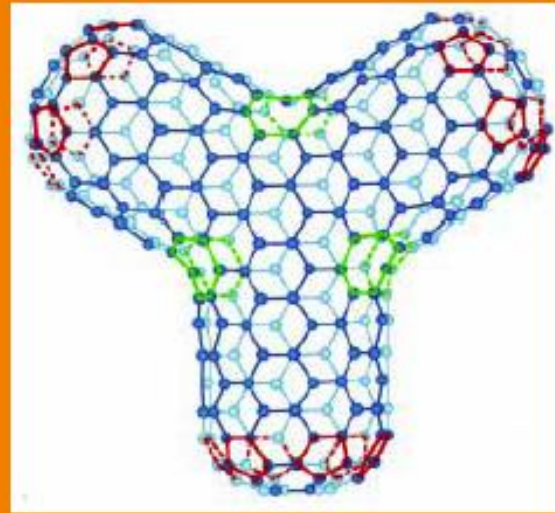


Carbon Nanotube



Sumio Iijima

Single-walled carbon nanotube, SWCNT



Multi-walled carbon nanotube, MWCNT



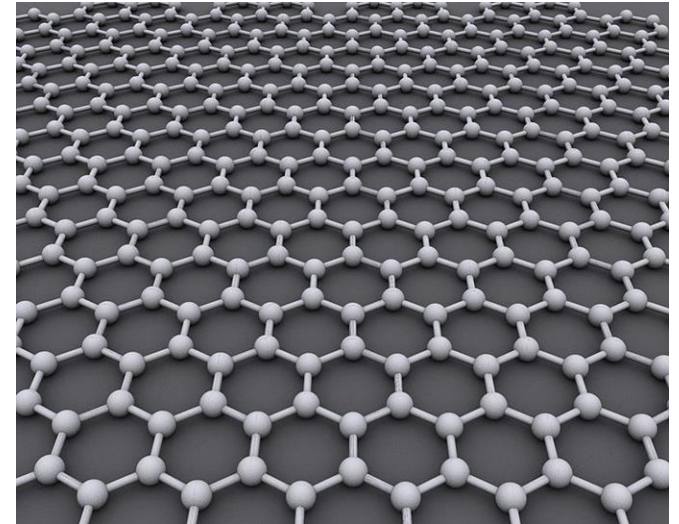
Carbon Nanotube based Transistors / Electronics

Unexpected realization of graphene sheet

(



mechanically exfoliated graphene sheets



AFM image of single-layer graphene on SiO_2
K.S. Novoselove et al., Science 306, 666 (2004)

(III) Tunneling and Nano-electronics


Classical Picture

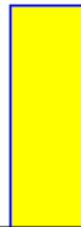
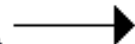
electron   electric field 



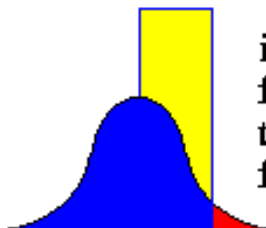
in classical physics, the electron is repelled by an electric field as long as energy of electron is below energy level of the field

Quantum Picture

electron wave 

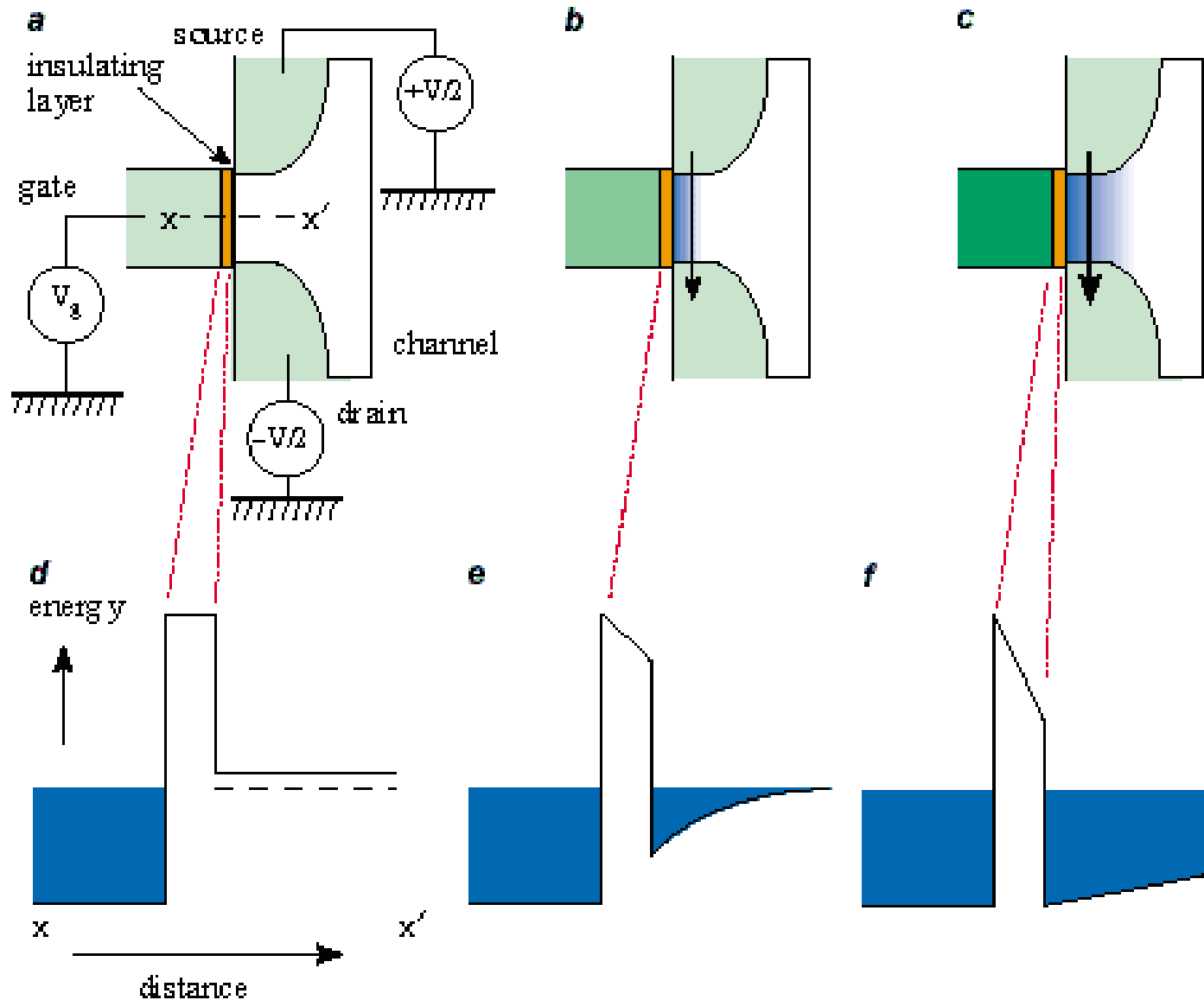


 ③nm



in quantum physics, the wave function of the electron encounters the electric field, but has some finite probability of tunneling through

Quantum Tunneling is the major effect for the failure of Transistor at nano scale





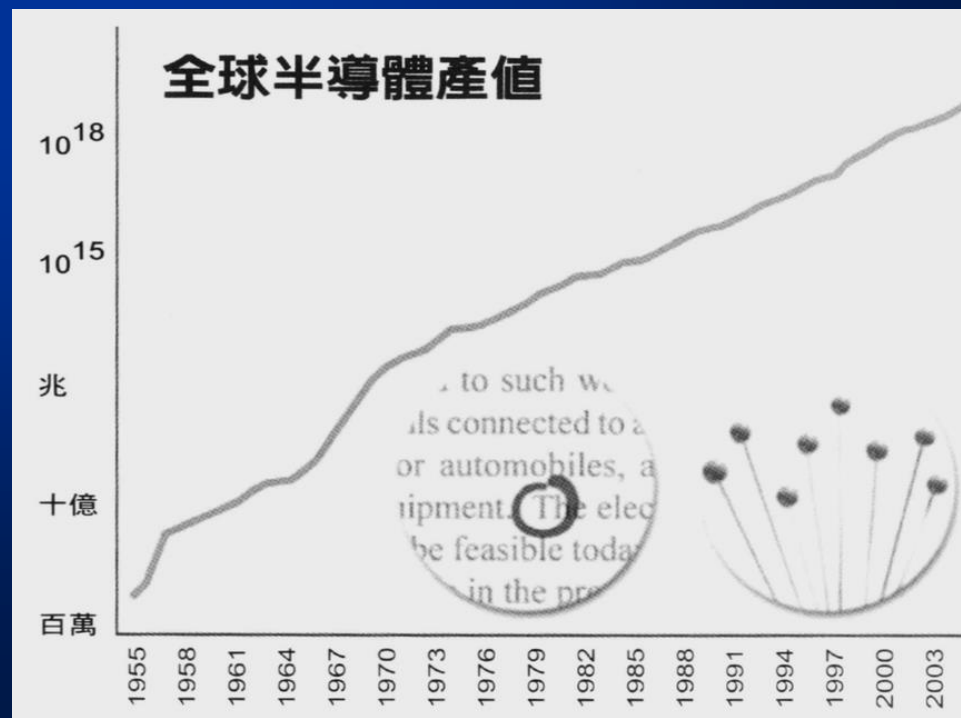
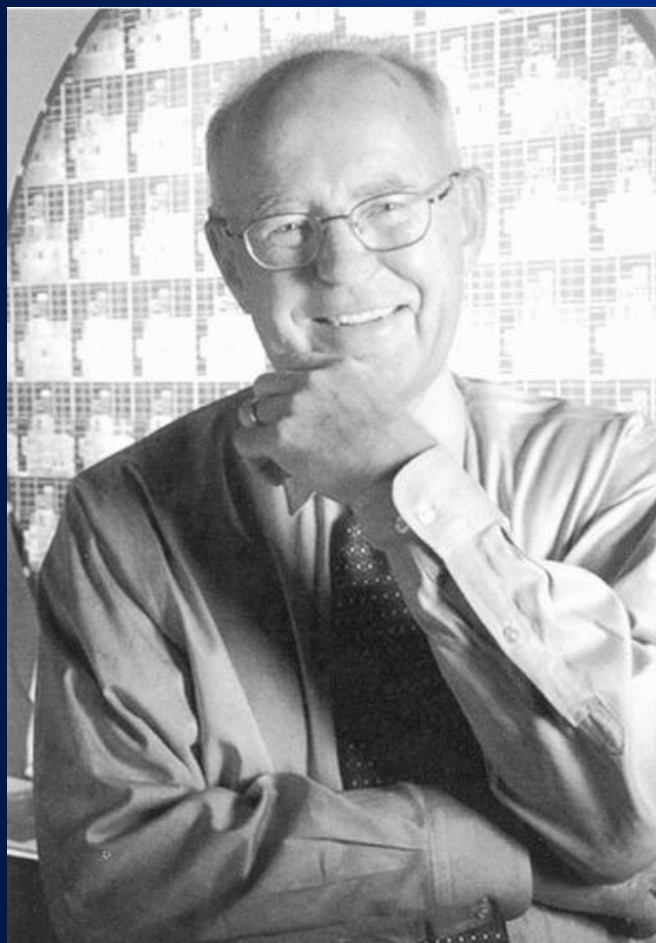
近來大力推動奈米科技的背景

來自微電子學可能遭遇瓶頸的考慮

Moore's Law : 摩爾定律

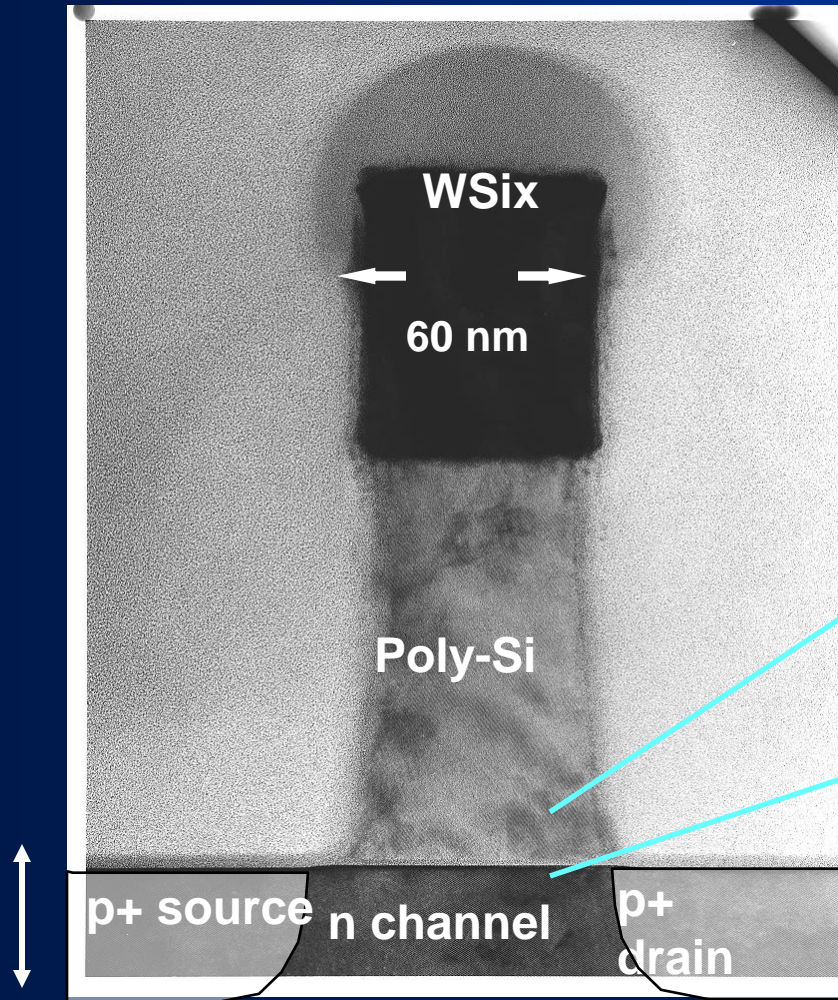
**A 30% decrease in the size of
printed dimensions every 1.5 years.**

矽晶上電子原件數每1年半會增加一倍

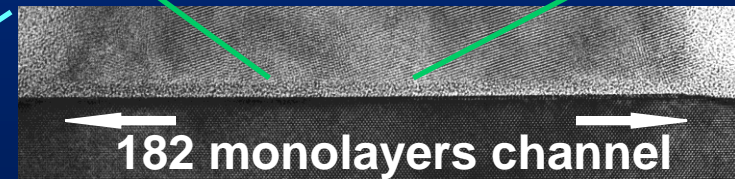
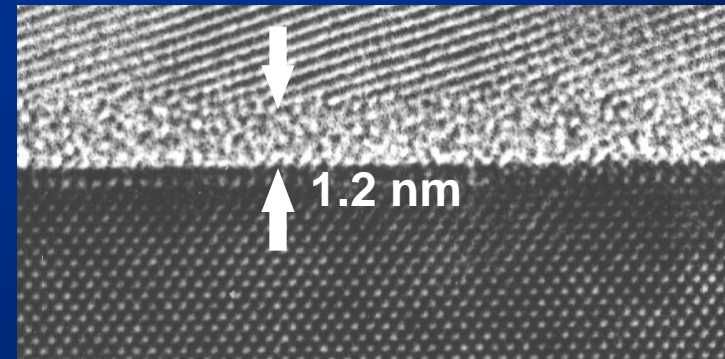




Scaling Limits to CMOS Technology



Gate Oxide ~ 5 Si Atoms thick !



Shrinking the junction depth \Rightarrow increasing the carrier concentration



CMOS scaling, When do we stop ?

Reliability: 25 ~~22~~ ~~18~~ ~~16~~ Å

processing and yield issue

Tunneling : 15 Å

Design Issue: chosen for 1 A/cm² leakage

$I_{\text{on}}/I_{\text{off}} \gg 1$ at 12 Å

Bonding:

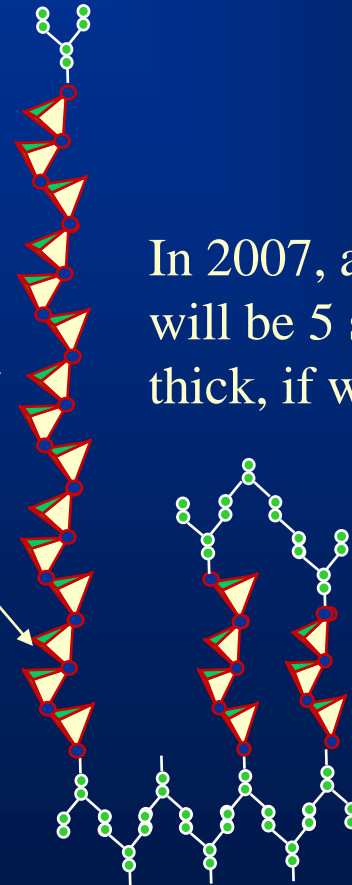
Fundamental Issues---

- how many atoms do we need to get bulk-like properties?
EELS -- Minimal 4 atomic layers !!
- Is the interface electronically abrupt?
- Can we control roughness?

In 1997, a gate oxide was 25 silicon atoms thick.

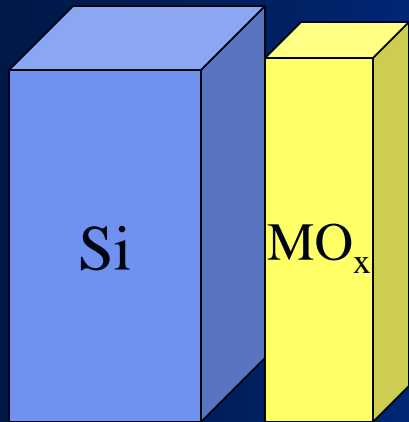
In 2007, a gate oxide will be 5 silicon atoms thick, if we still use SiO₂

and at least 2 of those 5 atoms will be at the interfaces.





Fundamental Materials Selection Guidelines



- Thermodynamic stability in contact with Si to 750°C and higher. **(Hubbard and Schlom)**
Alkaline earth oxide, IIIB, IVB oxide and rare earth oxide
- Dielectric constant, band gap, and conduction band offset
- Defect related leakage,
substantially less than SiO₂ at $t_{eq} < 1.5$ nm
- Low interfacial state density $D_{it} < 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$
- Low oxygen diffusivity
- Crystallization temperature $> 1000^\circ\text{C}$



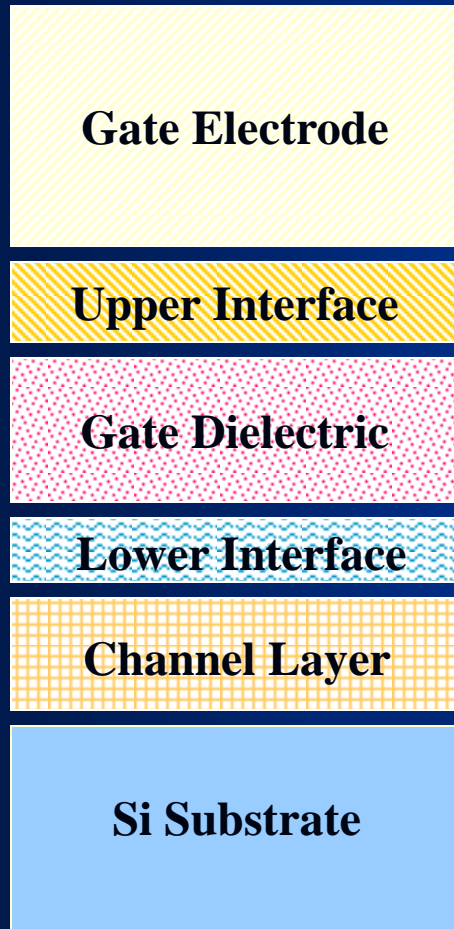
t_{eq} : **equivalent oxide thickness (EOT) to be under 1.0 nm**

$$t_{eq} = t_{ox} \kappa_{\text{SiO}_2} / \kappa_{ox}$$



Integration Issues for High κ Gate Stack

FET Gate Stack



Critical Integration Issues

- Morphology dependence of leakage
Amorphous vs crystalline films?
- Interfacial structures
- Thermal stability
- Gate electrode compatibility
- Reliability

Fundamental Limitations

- Fixed charge
- Dopant depletion in poly-Si gate
- Dopant diffusion
- Increasing field in the channel region



Basic Characteristics of Binary Oxide Dielectrics

Dielectrics	SiO ₂	Al ₂ O ₃	Y ₂ O ₃	HfO ₂	Ta ₂ O ₅	ZrO ₂	La ₂ O ₃	TiO ₂
Dielectric constant	3.9	9.0	18	20	25	27	30	80
Band gap (eV)	9.0	8.8	5.5	5.7	4.5	7.8	4.3	3.0
Band offset (eV)	3.2	2.5	2.3	1.5	1.0	1.4	2.3	1.2
Free energy of formation MO _x +Si ₂ → M+ SiO ₂ @727C, Kcal/mole of MO _x	-	63.4	116.8	47.6	-52.5	42.3	98.5	7.5
Stability of amorphous phase	High	High	High	Low	Low	Low	High	High
Silicide formation ?	-	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hydroxide formation ?	-	Some	Yes	Some	Some	Some	Yes	Some
Oxygen diffusivity @950C (cm ² /sec)	2x 10 ⁻¹⁴	5x 10 ⁻²⁵	?	?	?	10 ⁻¹²	?	10 ⁻¹³

Si CMOS Device Scaling – Beyond 22 nm node

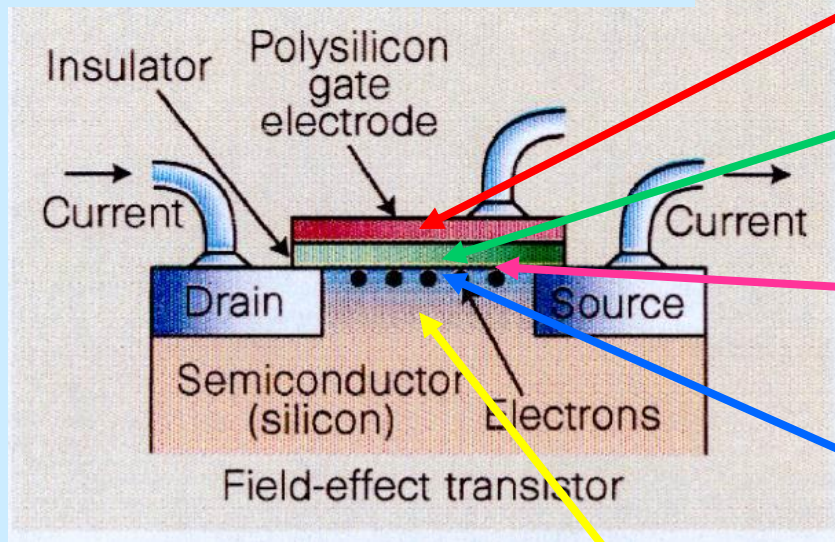
High κ , Metal gates, and High mobility channel

1947 First Transistor



The Transistor
50th Anniversary: 1947–1997

1960 First MOSFET



Metal Gate

High κ gate dielectric

Oxide/semiconductor interface

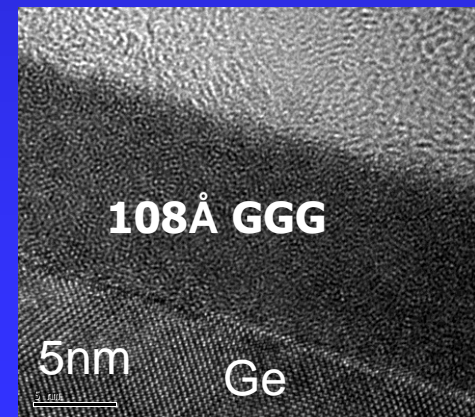
High mobility channel

Integration of Ge, III-V with Si

Moore's Law: The number of transistors per square inch doubles every 18 months

Shorter gate length L
Thinner gate dielectrics t_{ox}

Driving force :
High speed
Low power consumption
High package density



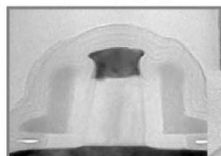


Intel Transistor Scaling and Research Roadmap

Transistor Scaling and Research Roadmap

90nm Node

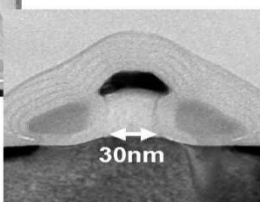
2003



50nm Length
(Production)

65nm Node

2005



30nm Length
(Development)

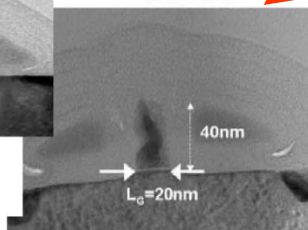
Uniaxial
Strain

SiGe S/D PMOS

1.2nm Ultra-thin SiO₂

45nm Node

2007

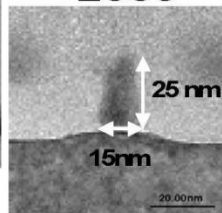


20nm Length
(Development)

High-K &
Metal-Gate
Options

32nm Node

2009

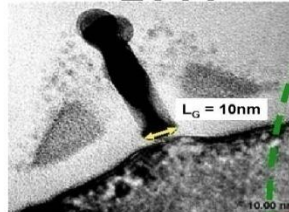


15nm Length
(Research)

Non-planar Tri-Gate
Architecture Option

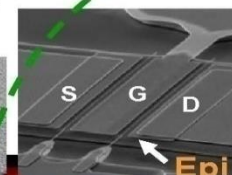
22nm Node

2011

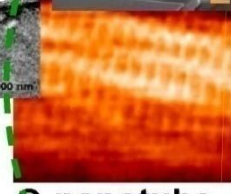


10nm Length
(Research)

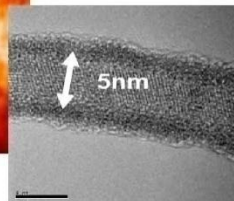
2015-2019
Research



III-V Device
Prototype
(Research)



C-nanotube
Prototype
(Research)



Nanowire
Prototype
(Research)

Robert Chau, Intel, ICSICT 2004

More non-silicon elements introduced

Science and Technology of Ultimate CMOS

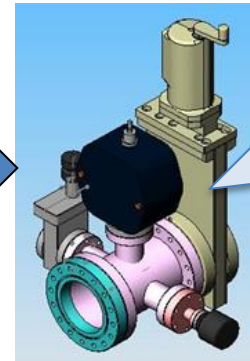
The Ultimate CMOS – End of road map

To achieve higher speed and lower power consumption

R&D of III-V InGaAs MOSFET state-of-art technology below 7 nm node,
by combining advanced analysis of spectroscopy/microscopy/quantum transport/theoretical modeling



- In-situ ALD of oxide integrated with MBE
- Tailor reconstructed surface to be Ga-rich
- Controlled chemical reaction route and species



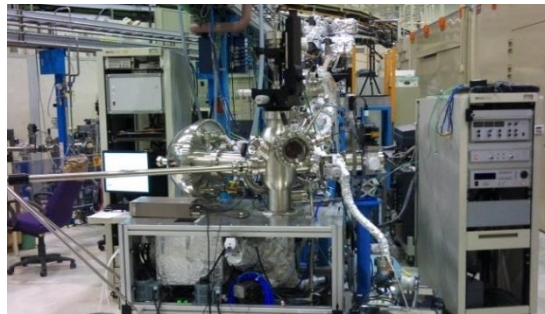
Portable UHV chamber for transfer 2" wafers in 3×10^{-10} torr for PES and STM analysis



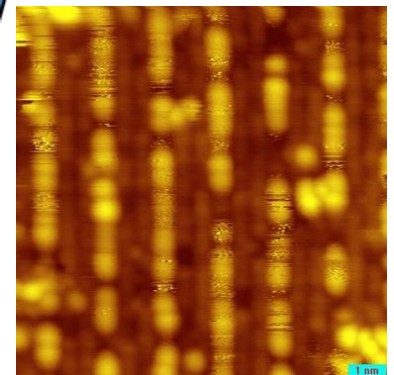
High resolution synchrotron radiation photoemission spectroscopy in NSRRC by Dr. T.W. Pi.



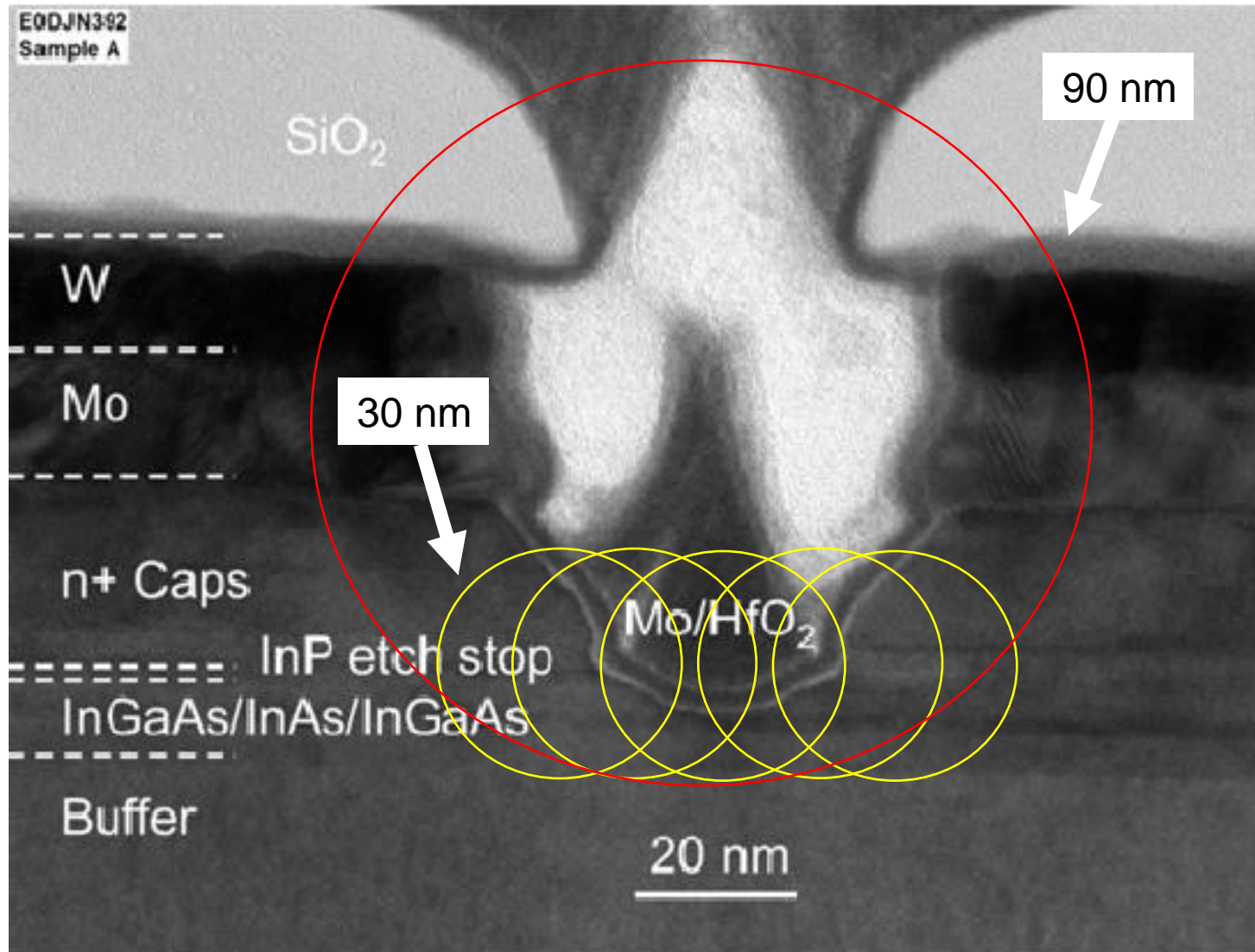
InGaAs surface reconstructed at 77K



RT and LT STM/STS study by Dr. W.W. Pi at CCMS/NTU



Bragg Ptychography on III-V MOSFETs with gate length < 30 nm

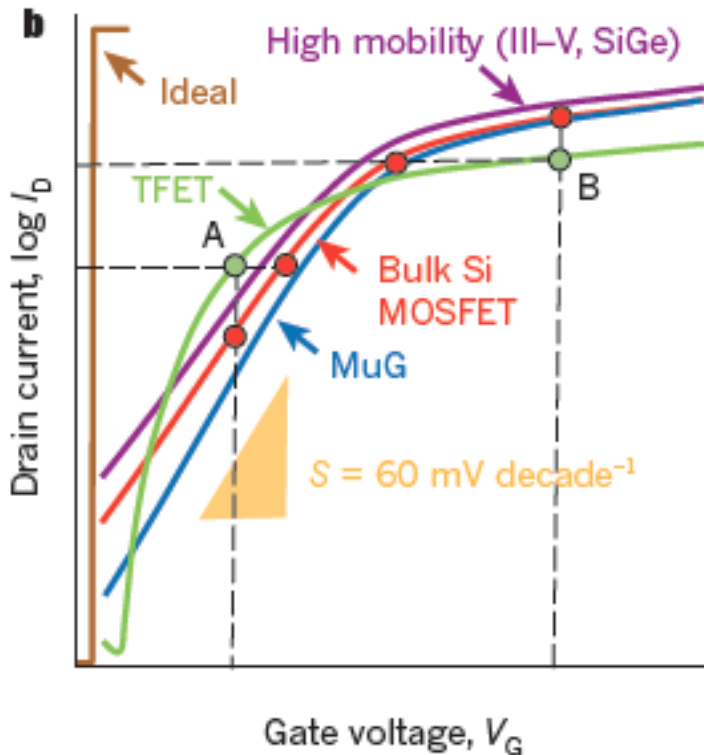


TFETs offer sharper turn-on devices compared to MOSFETs

lower V_{DD} to lower Switching Energy ($P_{\text{active}} \sim C \cdot V_{DD}^2$)

Better performance for ultra low-power applications

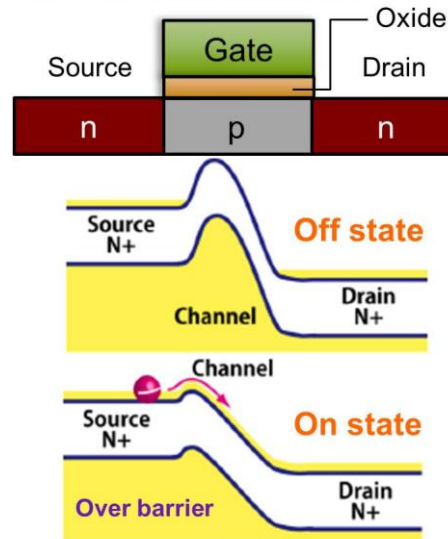
Atomic Model Prediction



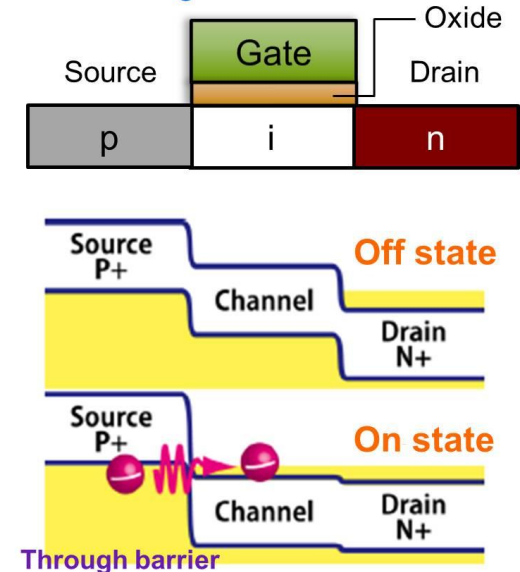
A. M. Ionescu et al.,

Nature **479**, 329 (2011).

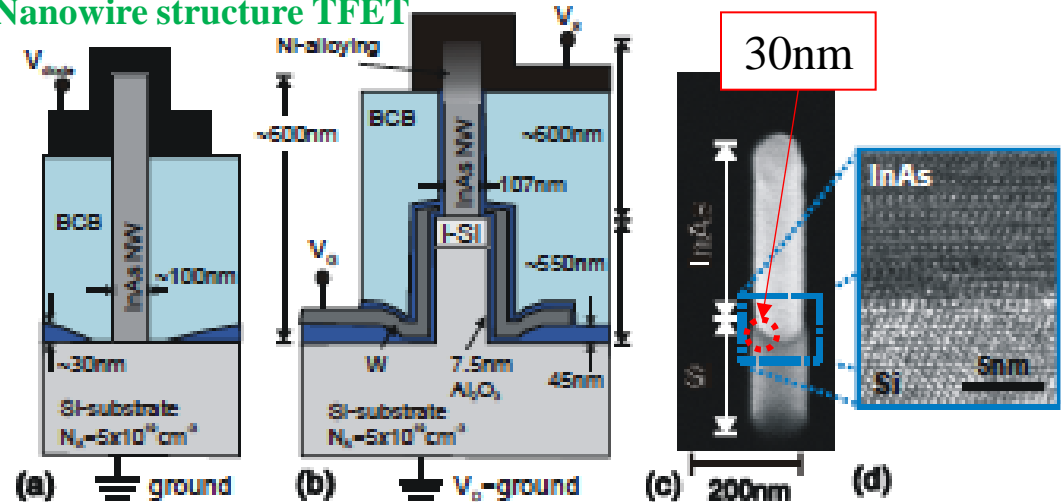
Conventional MOSFET



Tunneling FET



Nanowire structure TFET

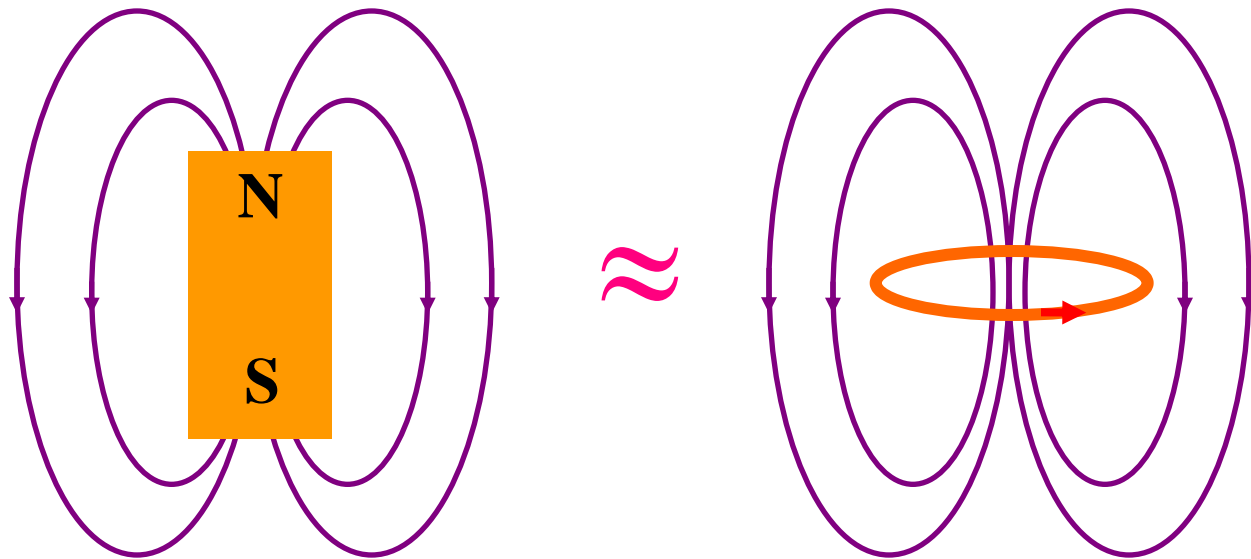


H. Riel et al., *IEDM* 391 (2012).

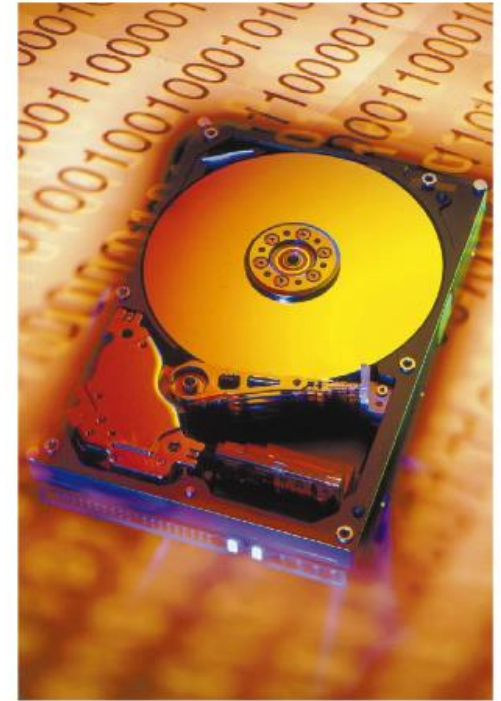
(IV) Quantum Spin

Spin and Nano technology

**Electron Spin is the smallest unit of magnetism,
Came from Quantum Mechanics**



**Often being used for
magnetic recording
~30 billion market**



Well read: spintronics has dramatically increased data storage densities in hard drives.

Spintronics \Leftrightarrow Electronics

Magnetic Tunnel Junctions(MTJ)

**New generation
of computer**

**Compu~~l~~ttion and storage
in one shot**

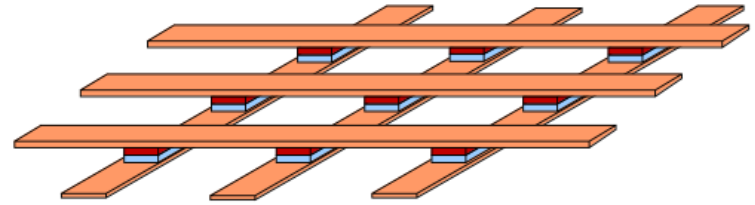
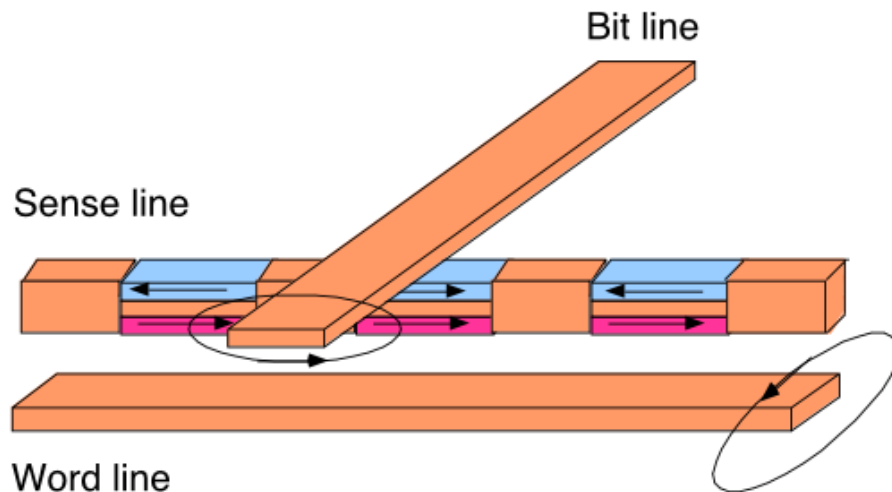


Fig. 7. A schematic representation of RAM that is constructed of magnetic tunnel junctions connected together in a point contact array. The conducting wires provide current to the junctions and permit voltage measurements to be made. They also enable the manipulation of the magnetization of the elements by carrying currents both above and below the magnetic junctions to create magnetic fields.

**When turn-on,
it is ready!**

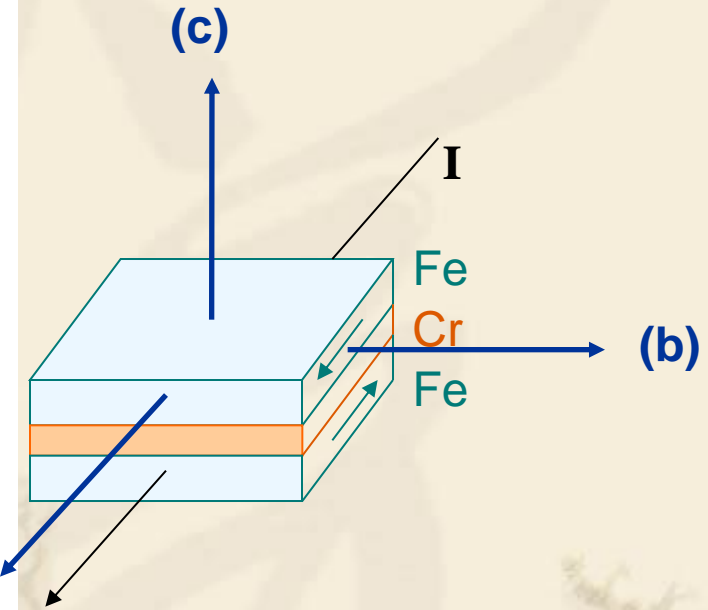
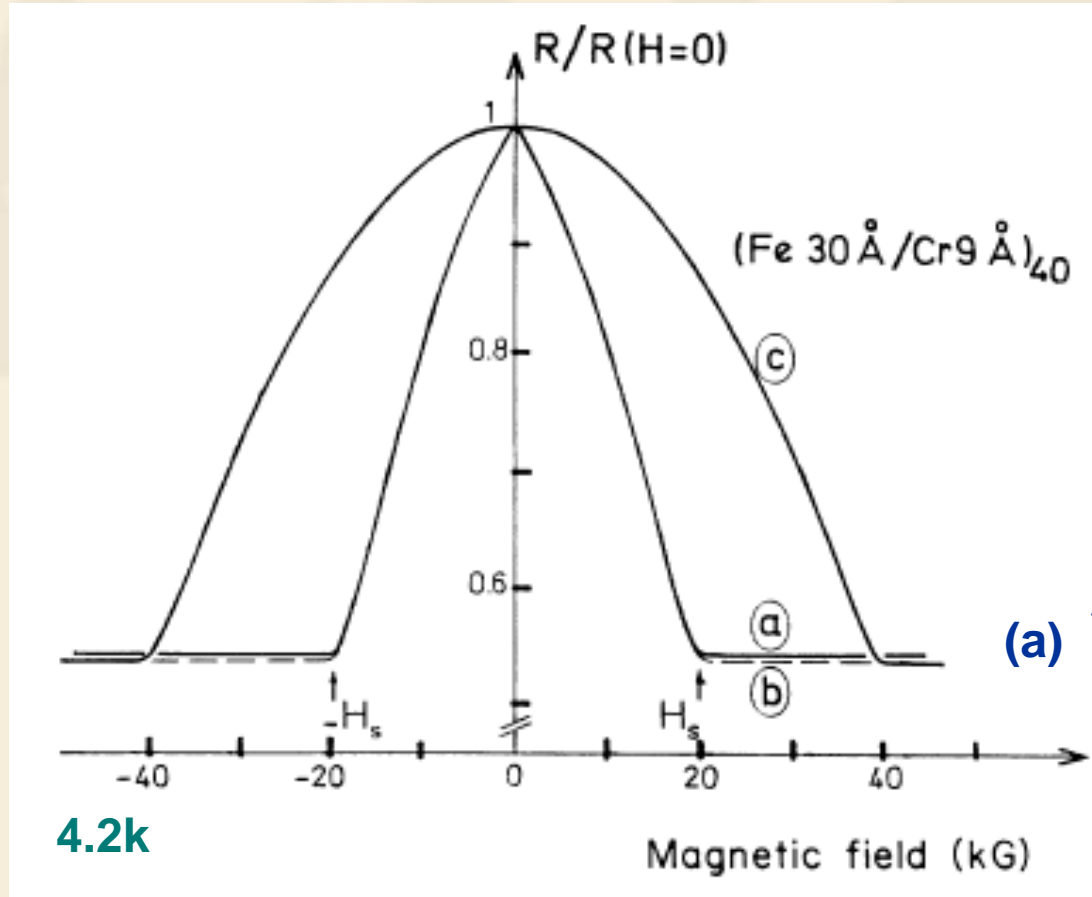
Giant Magnetoresistance(GMR)

❖ What is GMR?

- ✧ GMR is a very large change in electrical resistance that is observed in a ferromagnet/paramagnet multilayer structure.
- ✧ Resistance change occurs when the relative orientations of the magnetic moments in alternate ferromagnetic layers change as a function of applied field.
- ✧ The total resistance of this material is lowest when the magnetic orientations of the ferromagnetic layers are aligned, is highest when the orientations are anti-aligned.

Ferro.
Para.
Ferro.
Ferro.
Para.
Ferro.
Para.
Ferro.

First Evidence of GMR

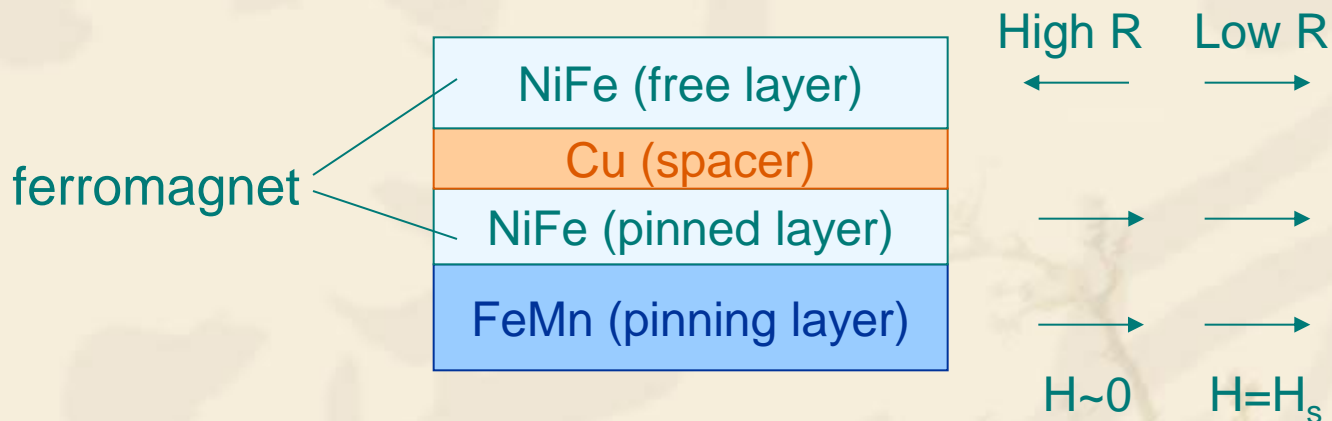


H_s corresponds to the field at which all layer magnetizations point along the field direction.

Spin-Valve GMR

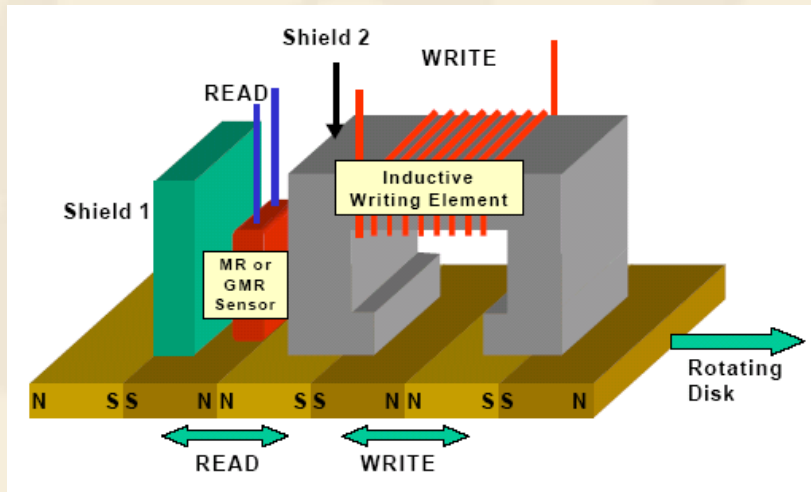
❖ What is Spin-Valve GMR ?

✧ The simple structure of Spin-valve GMR is



✧ The magnetisation of the top permalloy layer is free to rotate as the field is varied, Second permalloy layer is fixed due to its exchange interaction with the iron–manganese layer.

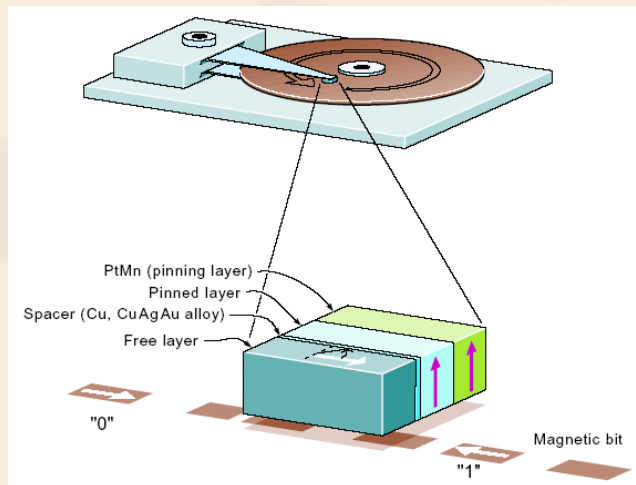
GMR Spin Valve Reading Head



✧ Magnetization is stored as a “0” in one direction and as a “1” in the other. This is the magnetic field sensed by the GMR head.

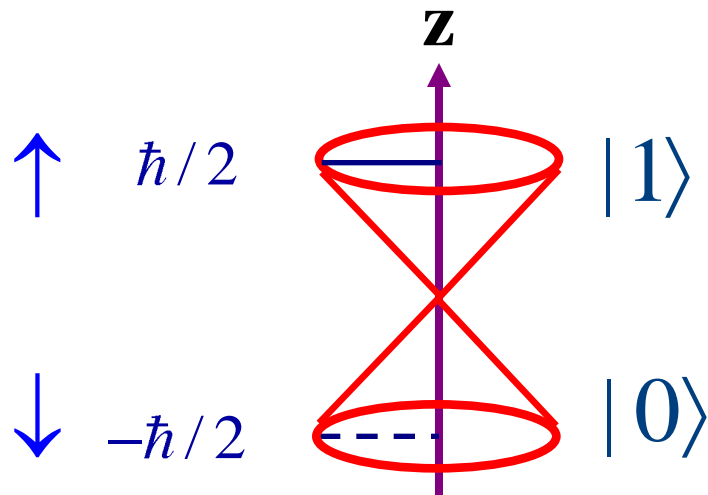
✧ When the head passes over these magnetic bits, the magnetization direction of the free layer in the head responds to the fields in each bit by rotating either up or down.

✧ The resulting change in the resistance is sensed by the voltage acrossing the GMR head (current passing through the GMR element is constant).



Quantum behavior of ferromagnets

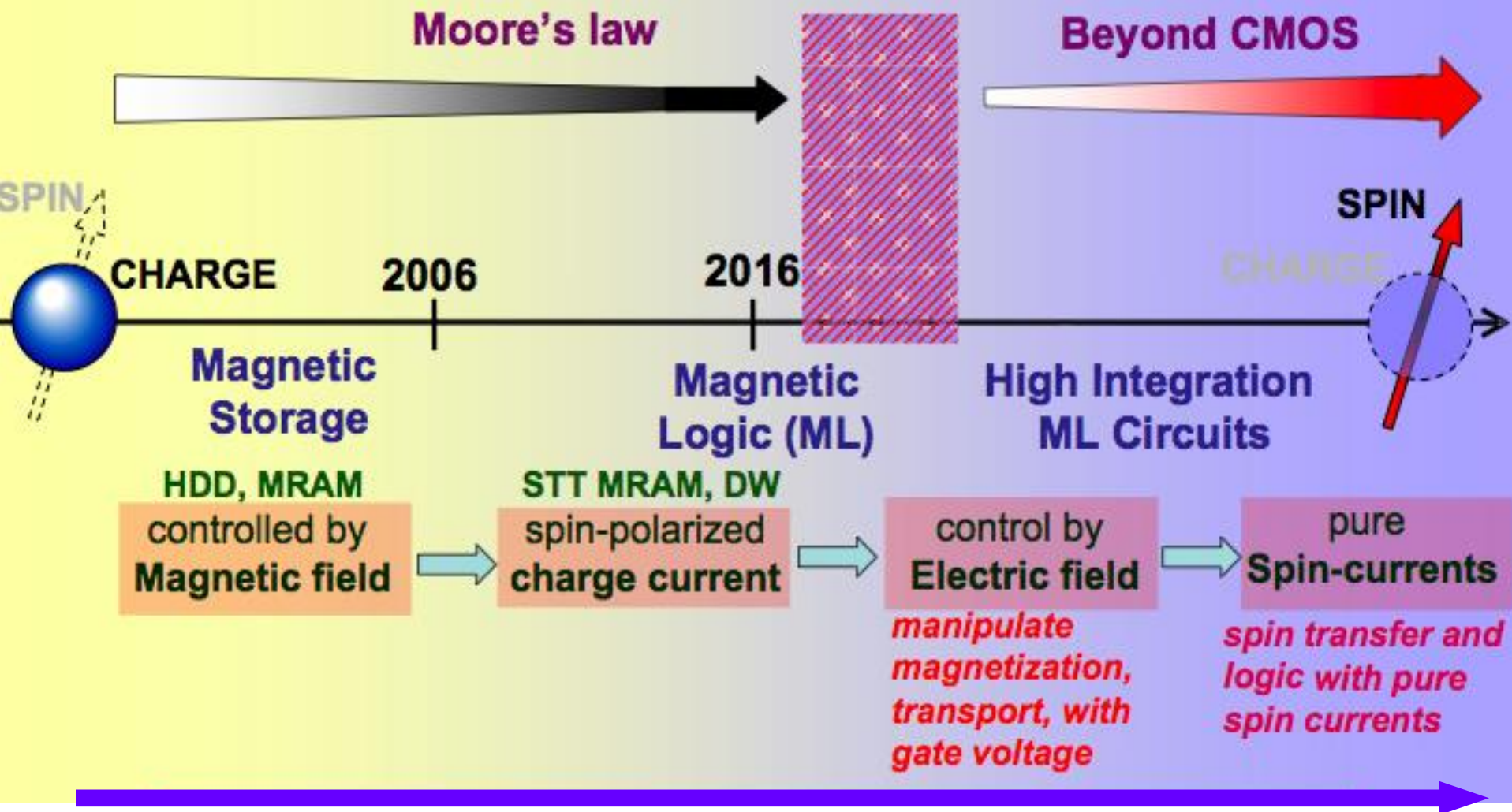
-Spin as a quantum qubit



$$\text{qubit} = \alpha |0\rangle + \beta |1\rangle$$

**Due to superposition
More information!**

Tentative roadmap



**Can we take the “charge” out of Spintronics ?
To generate pure spin current !**

Spintronics vs Electronics

- ✓ Reducing the heat generated in traditional electronics is a major driving force for developing spintronics.
- ✓ Spin-based transistors do not strictly rely on the raising or lowering of electrostatic barriers, hence it may overcome scaling limits in charge-based transistors.
- ✓ Spin transport in semiconductors may lead to dissipationless transfer of information by pure spin currents.
- ✓ Allow computer speed and power consumption to move beyond limitations of current technologies.

Reliable generation of pure spin currents !

- ✓ Spin Hall effect (2004)
- ✓ Spin Pumping (2006)
- ✓ Inverse Spin Hall effect (2006)
- ✓ Spin Seebeck effect (2008)
- ✓ Spin Caloritronics (2010)

Major Quantum Effect at the nano scale

- Interference
- Quantization
- Tunneling
- Quantum Spin