Beyond CMOS

(I) Ultimate CMOS: High k dielectrics on high carrier mobility semiconductors - accomplishments and challenges

(II) Spintronics: Pure spin current generation by spin pumping in FM/NM, FM/SC, and FM/TI

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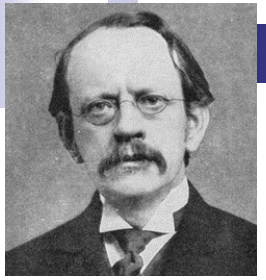
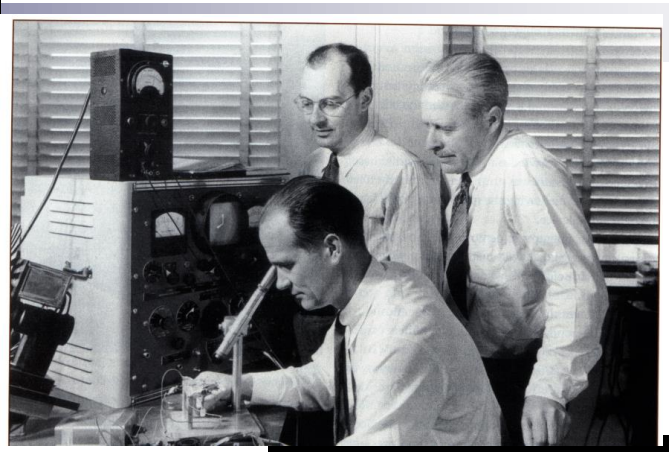


1897 J. J. Thomson discovery of electron - using properties of cathode rays, electron charges

The cathode ray tube (CRT) is a vacuum tube

What next?



1947 The Transistor

2007 High k + metal gate on Si for 45 nm node CMOS; 2010 32 nm, 2012 22 nm, and 2014 15 nm node. InGaAs, Ge, InGaSb, GaN 2016-2025?

- Mervin Kelly, the then Director of Research at Bell Labs, had predicted the problem and had already taken action to find a solution.
  - Although relays and vacuum tubes were apparently making all things possible in telephony, he had predicted for some years that the low speed of relays and the short life and high power consumption of tubes would eventually limit further progress in telephony and other electronic endeavors.
  - In the summer of 1945, Kelly had established a research group at Bell Labs to focus on the understanding of semiconductors. The group also had a long-term goal of creating a solid-state device that might eventually replace the tube and the relay.

What are the next "Big Innovation(s)"? ***Quantum Mechanics and Spin!!!***

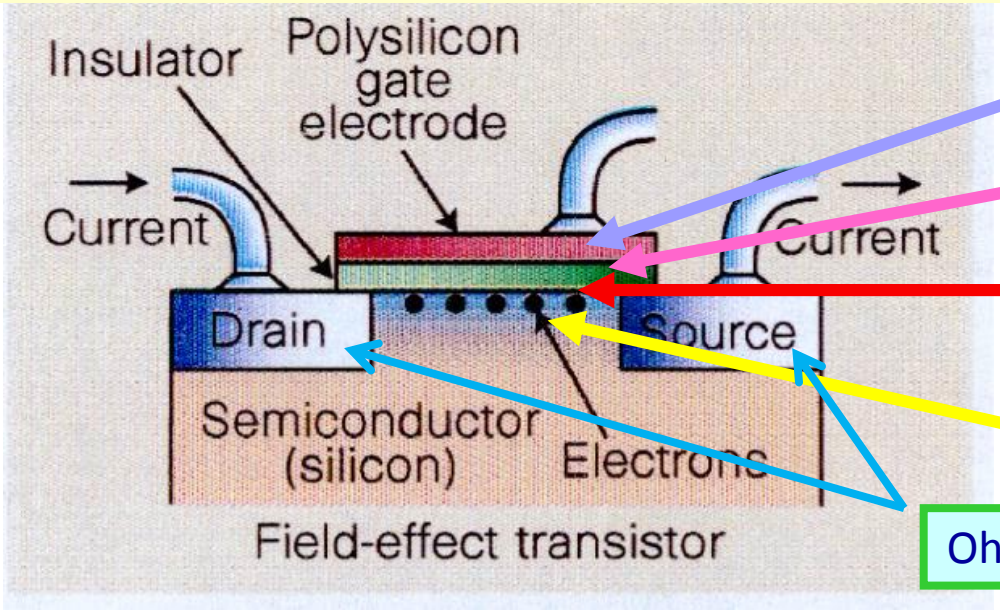
Beyond CMOS – new physics and novel devices

- CMOS integrated circuit technology for computation at an inflexion point
  - The technology has enabled the semiconductor industry to make vast progress over the past 40 years.
  - It is expected to see the challenges going beyond the ten/twenty-year horizon.
    - Particularly from an energy efficiency point of view.
- Extremely important for the semiconductor industry/academic institutions to discover a new technology which will carry us to the beyond CMOS area
  - Power-performance of computing continues to improve
- New devices
  - Spintronics
  - Non-Boolean logic associated memory
  - Quantum computing

Device Scaling – Beyond Si CMOS:

high κ, metal gates, and high carrier mobility channel

1960 Kahng and Atalla, Bell Labs First MOSFET



Metal gate

High κ gate dielectric

Oxide/semiconductor interface

High mobility channel

Ohmic Contacts

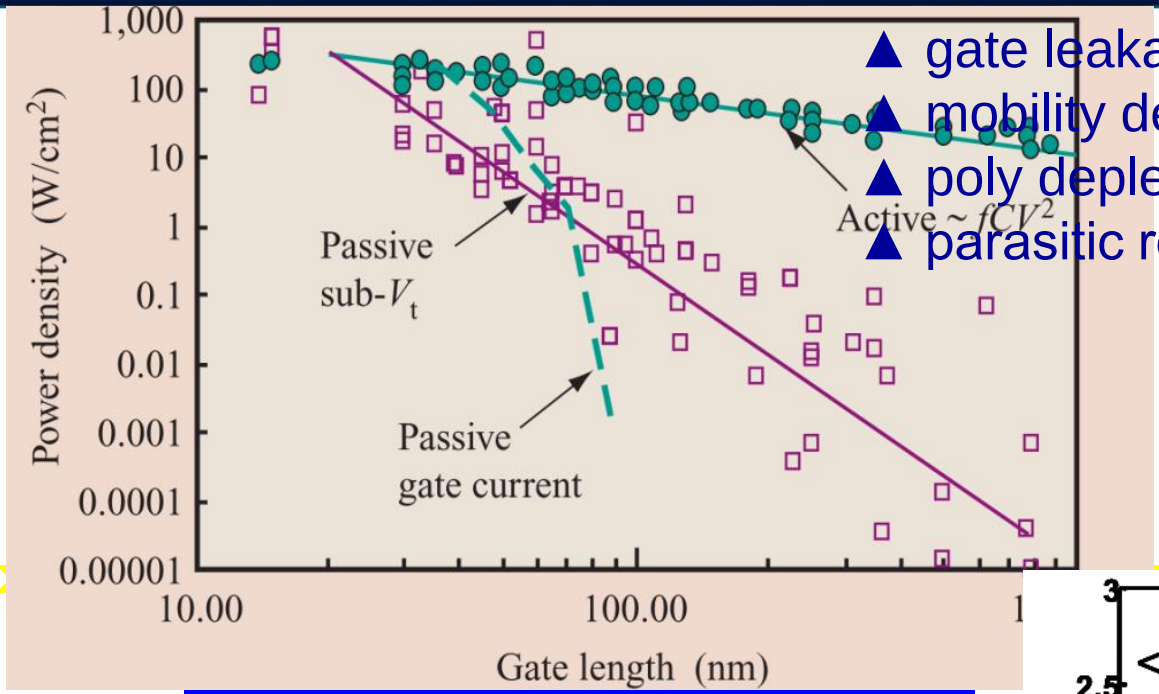
Integration of IIIV, Ge, GaN with Si

Moore's Law:
The number of transistors per square inch doubles every 18 months

Shorter gate length L
Thinner gate dielectrics t_{ox}

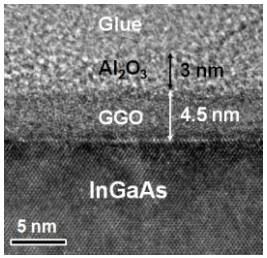
Driving force :
High speed
Low power consumption
High package density

Why high-κ/III-V's?



- gate leakage
- mobility degradation
- poly depletion
- parasitic resistance …

III-V

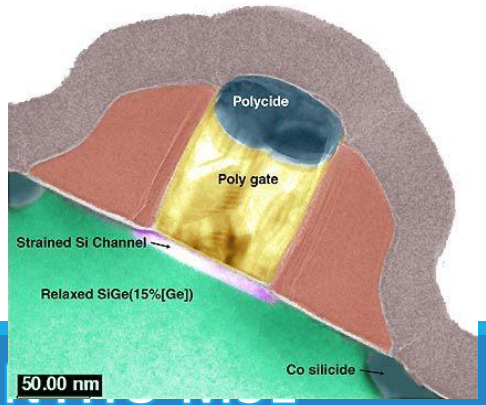


15nm 2014-2015

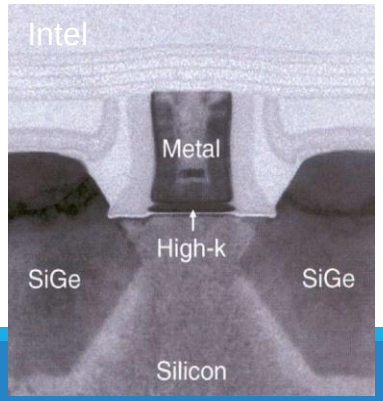
10--7nm 2014 … ?

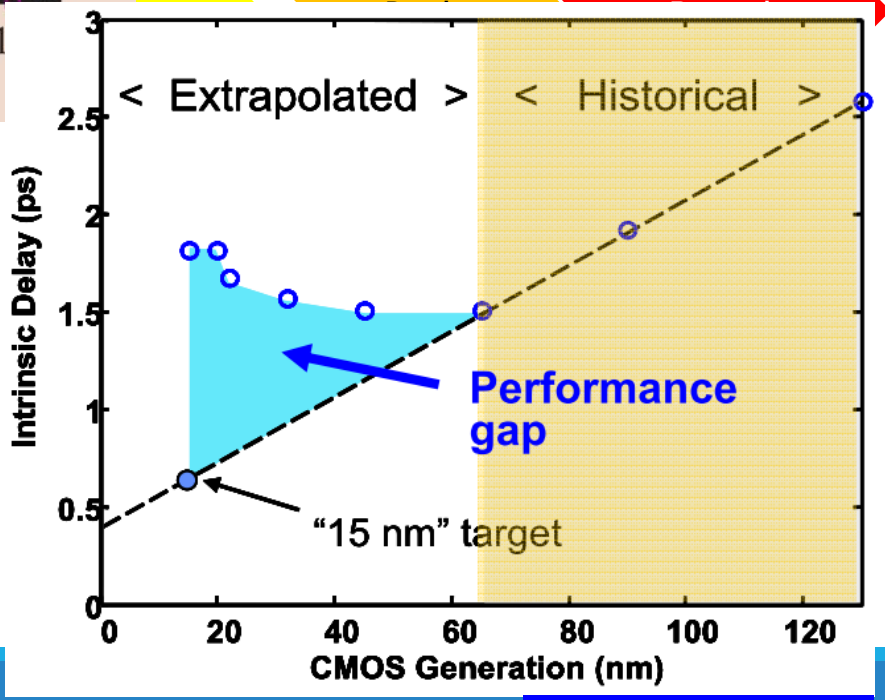
W. Haensch *et al.*, IBM J. Res. & Dev. **50,** 339 (2006)

Strained Si



High-κ metal Gate





D. Antoniadis, MIT

III-V Surface Passivation

Requirements

thermally and electronically stable at high temperatures of >800 ℃
low leakage currents
low interface trap density (D_{it})
high κ values $\Rightarrow$ low EOT < 1nm

Early Efforts (1960s - 1990s) reviewed by Hong et al, "Encyclopedia of Electrical and Electronics Eng.", v. 19, p. 87, Ed. Webster, John Wiley & Sons, 1999

- Anodic, thermal, and plasma oxidation of GaAs
- Wet or dry GaAs surface cleaning followed by deposition of various dielectric materials

Hong, Kwo et al,
- JVST (1996);
- Science (1999)
- APL (1999)

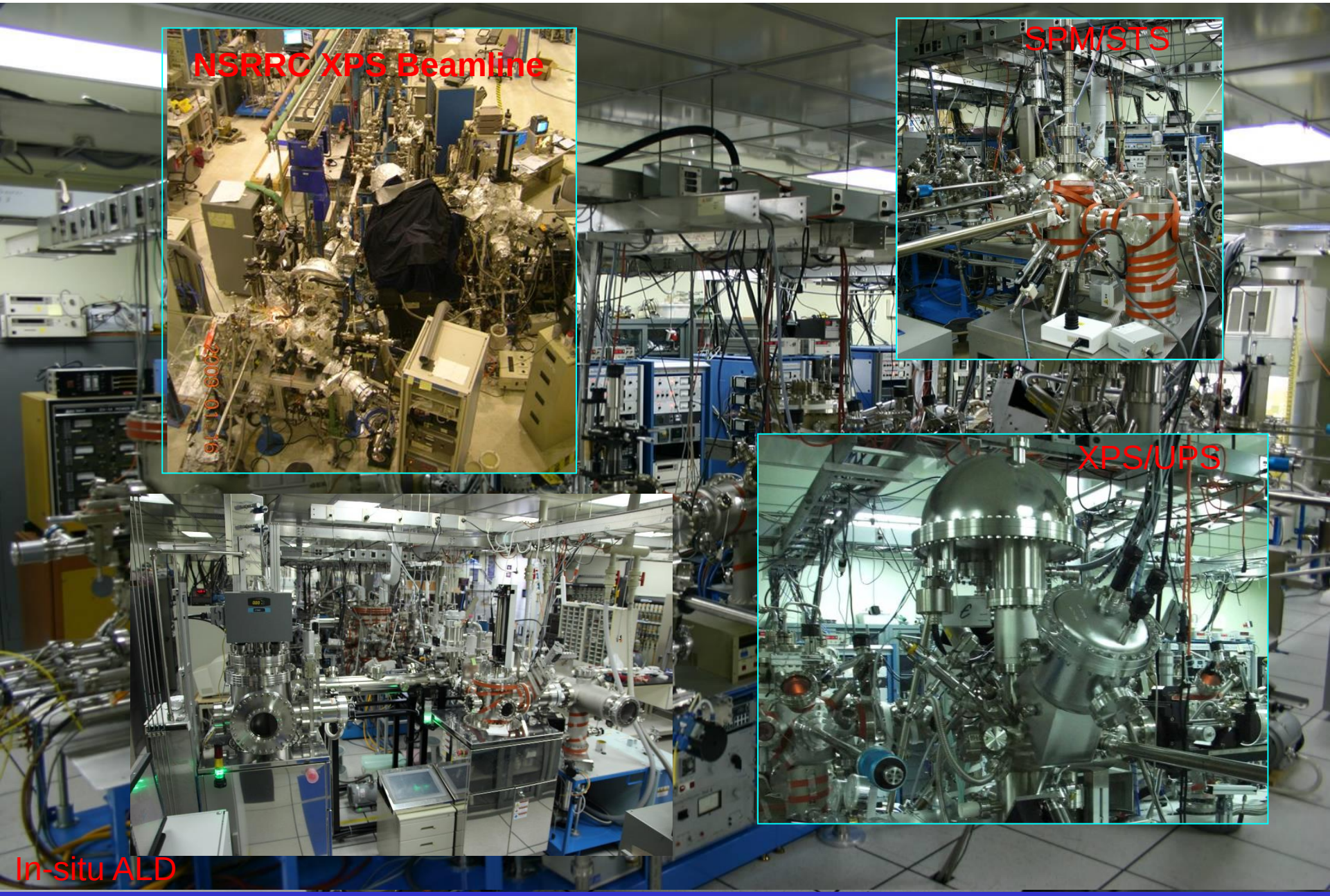
1st Breakthrough (1994)

- ***in-situ*** **UHV deposited $Ga_2O_3(Gd_2O_3)$ [GGO] and Gd_2O_3 (Bell Labs)**

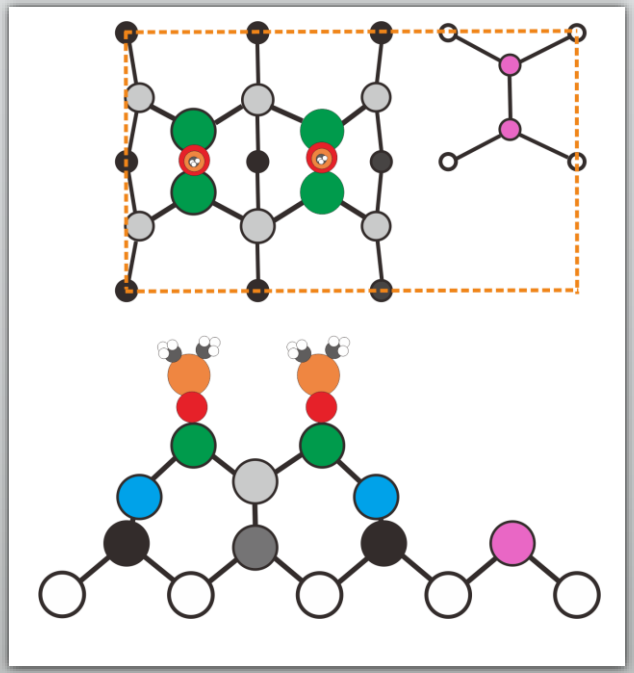
Recent Demonstrations

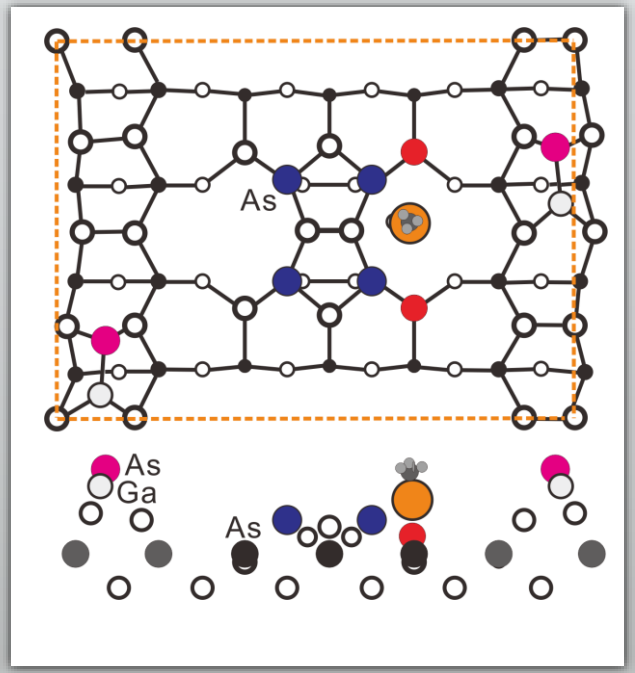
- ***in-situ*** **UHV deposited high-κ's (NTU/NTHU, Freescale/U. Glasgow, IMEC, UT-Dallas …)**
- ***ex-situ*** **ALD high-κ's (Agere, Purdue U., NTU/NTHU, Intel, IBM, IMEC, UCSB…) (2003)**
- **a-Si or Ge interfacial passivation layers (IPLs)+ high-κ's**

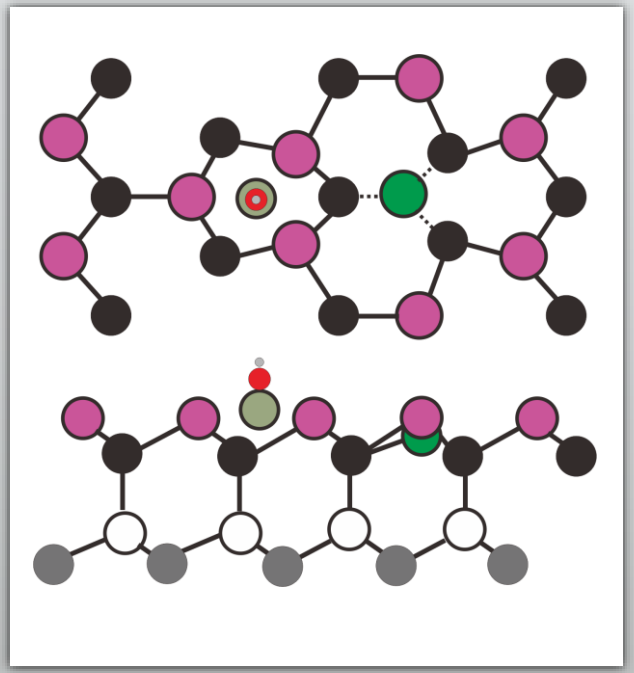
  (IBM, UT-Dallas, UT-Austin, NUS, U. Albany-SUNY/Intel/SEMATECH …)
- ***in-situ*** **ALD high-κ's (NTU/NTHU, UTD) (2009)**


NSRRC XPS Beamline
SPM/STS
XPS/UPS
In-situ ALD

ALD (TMA+H_2O) on GaAs







For GaAs(001)-2x4 and GaAs(001)-4x6:

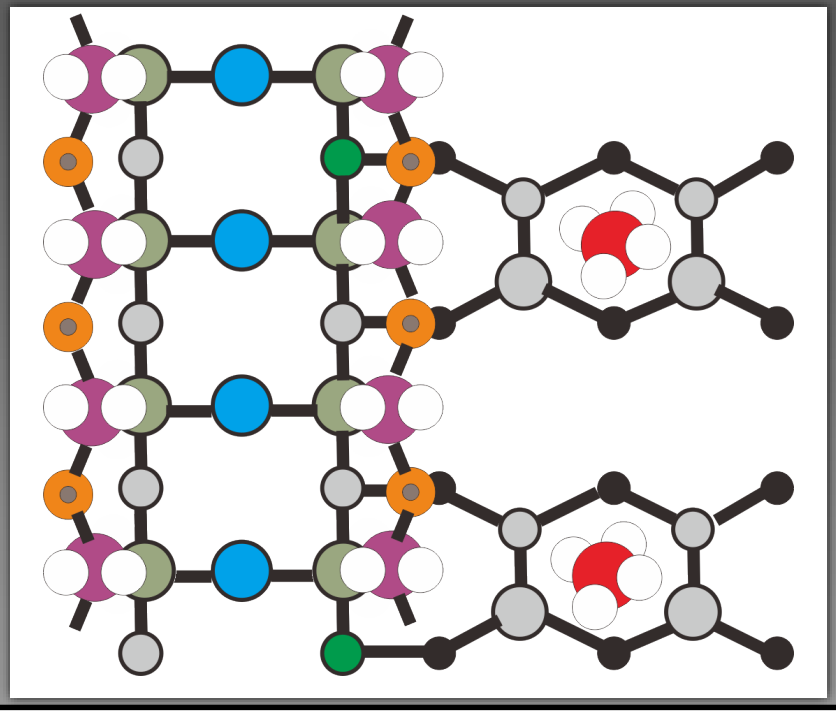
- The precursors attach partially the topmost As layer, leaving other surface atoms intact

For GaAs(111)A-2x2:

- Al sits at the the Ga-vacant site, thereby passivating the As dangling bonds
- The precursors relax the surface reconstruction, thus generating Ga dangling bonds

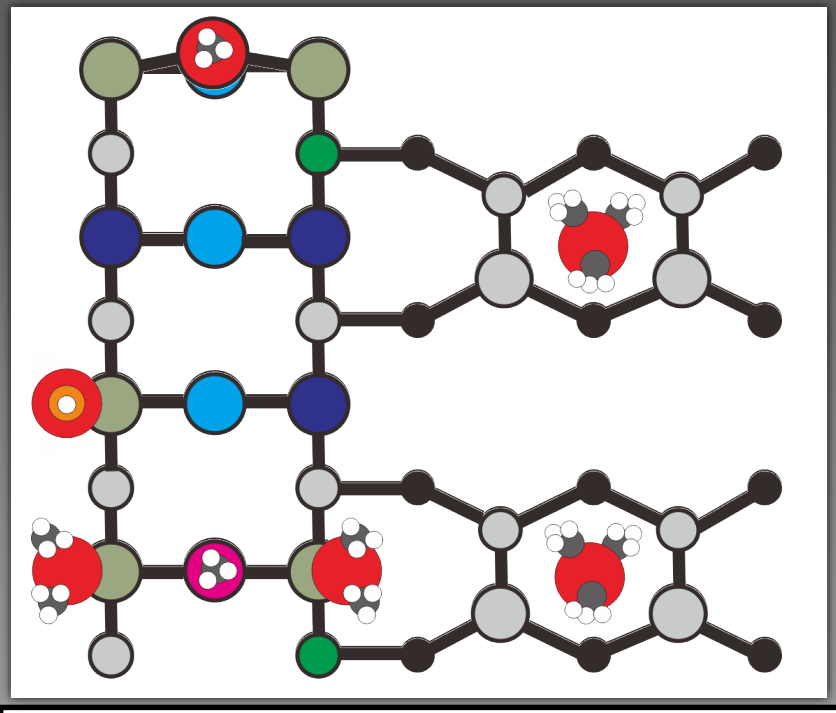
1 cycle of (TMA+H_2O)/(TEMAHf+H_2O) on In_xGa_yAs(001)-4x2

(TEMAHf+H_2O) on $In_{0.53}Ga_{0.47}As$(001)-4x2



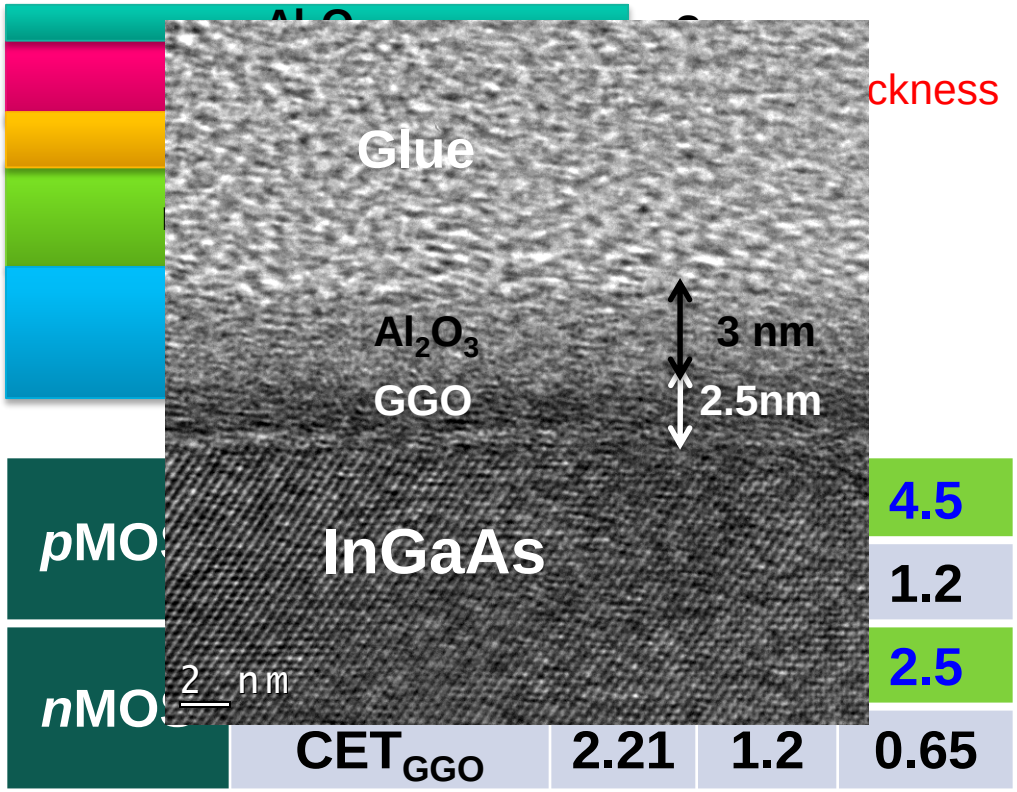
- Hf remains in the 4+ charge state
- All the top row As atoms are bonded with Hf
- The top row In atoms are not passivated
- Some top row In atoms are expelled

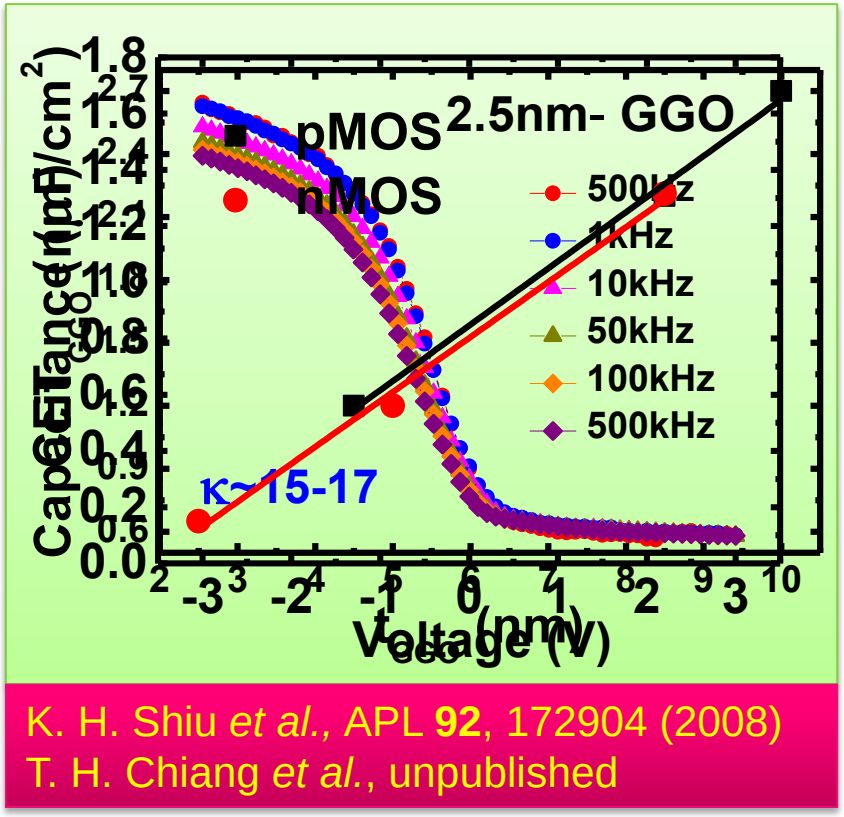
(TMA+H_2O) on $In_{0.20}Ga_{0.80}As$(001)-4x2



- Al exists in TMA, DMA, and MMA
- DMA/MMA bonds with the top row As atoms
- The top row In atoms are not passivated
- 1 cycle passivates partially the row As

GGO Scalability and Thermal Stability





K. H. Shiu *et al.*, APL **92**, 172904 (2008)
T. H. Chiang *et al.*, unpublished

- Al_2O_3 capping effectively minimized absorption of moisture in GGO
- GGO (2.5nm) dielectric constant maintains ~15 (CET~7Å)
- D_{it}'s ~ low $10^{11}(cm^{-2}eV^{-1})$ range even subjected to 900°C annealing (Conductance Method)

Ultimate CMOS - $In_{0.53}Ga_{0.47}As$

Applications:

- **Optoelectronics in Optical communication and Photon sensor (Output value >30B USD in 2013, Annual growth rate >9%)**
- **High performance CMOS technology in logic circuit (Output value >300B USD, Annual growth rate >5% in 2013)**

Challenges:

- **$In_{0.53}Ga_{0.47}As$ surface passivation with tetra-valence high κ's is recognized as "MISSION IMPOSSIBLE"**
  →The importance of high k's/$In_{0.53}Ga_{0.47}As$ interface control is addressed
- **Low re-crystallization temp. of ~600°C for pure HfO_2 restricts the thermal budget for device processing**

Experiment and accomplishments:

- ✓ **ALD Hf-based high κ oxide is commercialized in Si CMOS industry → Benefit from Mass Production and sufficiently high κ value**
- ✓ **Clean and atomically ordered fresh $In_{0.53}Ga_{0.47}As$ surface w/o chemical treatment or interfacial passiv. layer**
- ✓ **Thin ALD-HfO_2 (0.8nm) initial layer followed by ALD-HfAlO top layer to enhance thermal stability (>800°C)**
- ✓ **Best Interfacial Properties and MOS Devices Performance reported so far among the worldwide research groups**

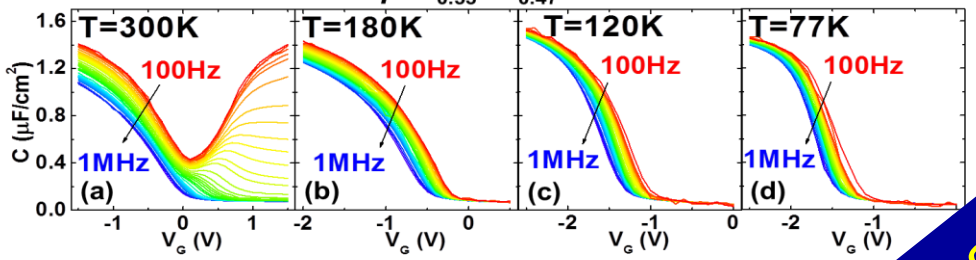
Publication:
T. D. Lin, J. Kwo, and M. Hong et al., Appl. Phys. Lett. **100**, 172110 (2012)
T. D. Lin, J. Kwo, and M. Hong et al., Appl. Phys. Lett. **103**, 253509 (2013)

Ultimate CMOS – high k/$In_{0.53}Ga_{0.47}As$

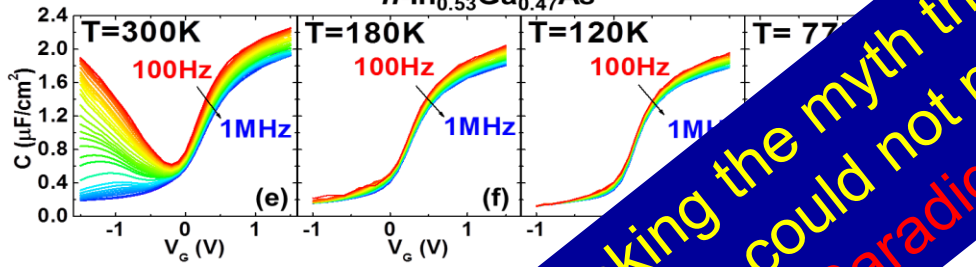
Experiment Results:

ALD-HfAlO/HfO_2 (0.8nm)/$In_{0.53}Ga_{0.47}As$

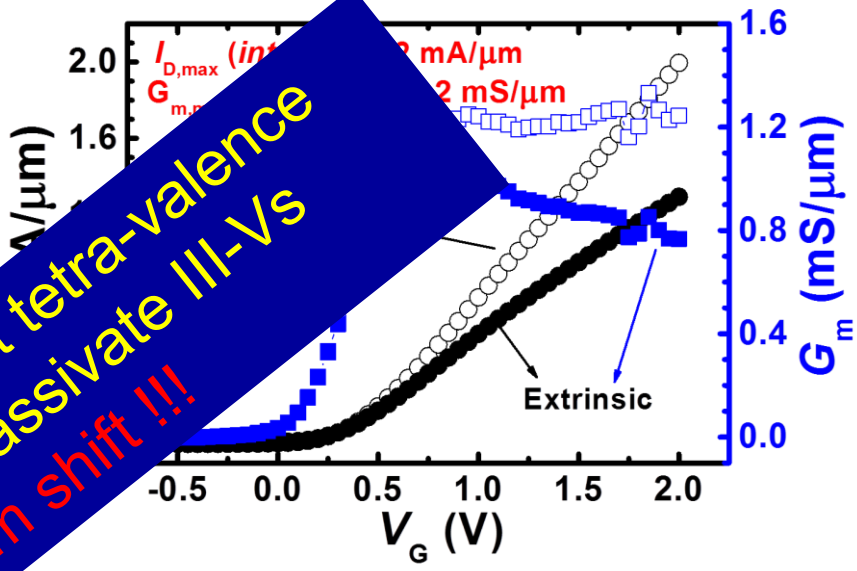
p-$In_{0.53}Ga_{0.47}As$



n-$In_{0.53}Ga_{0.47}As$



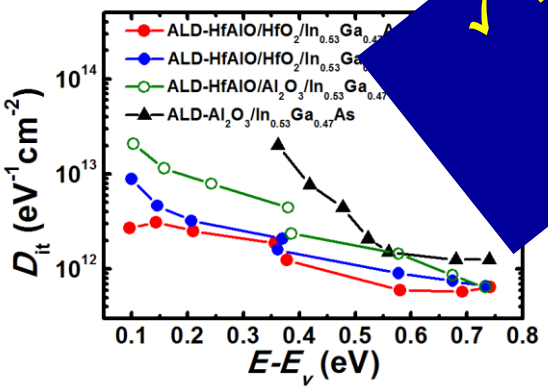
1 μm Lg Device performance



✓ Breaking the myth that tetra-valence oxide could not passivate III-Vs

✓ Paradigm shift !!!

D_{it} distribution



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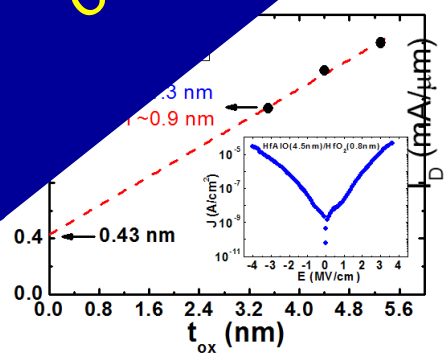

Benchmark