Research on III-V and Ge nano-electronics for science and technology beyond Si CMOS

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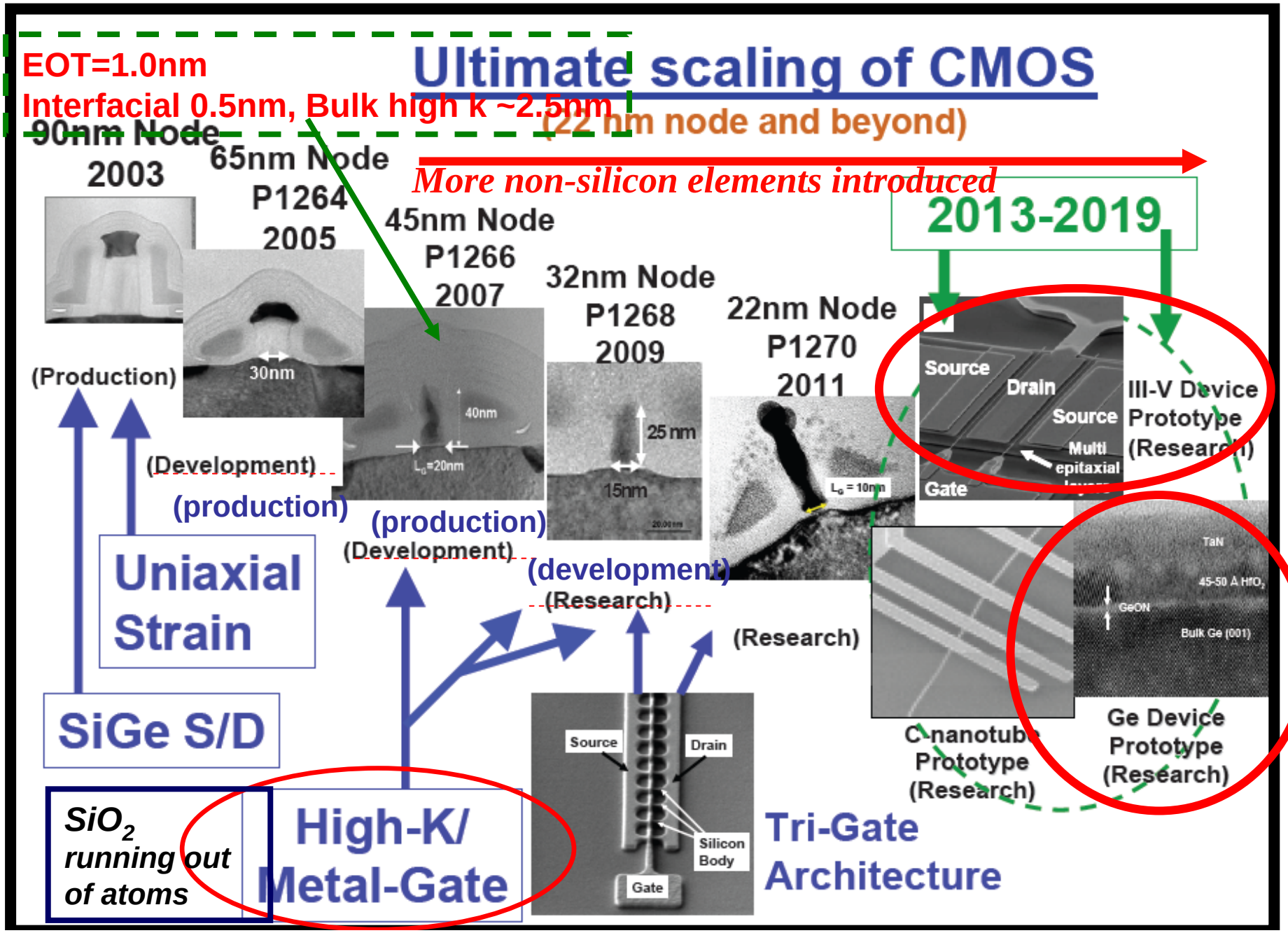
- Background on GaAs surface Fermi level unpinning
  - *Interfacial atomic manipulation*

- III-V, GaN, and Ge MOSFET with high κ + metal gates, Spintronics, graphene

- 32 and 22 nm node Si CMOS (high κ + metal gates)
  - MBE + ALD for EOT < 1.0 nm

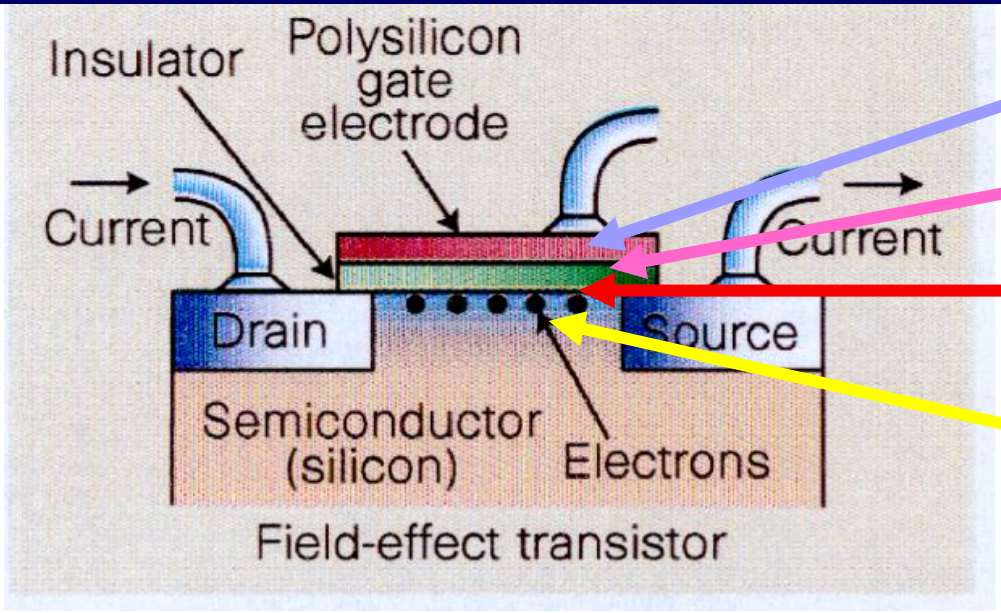
- Single crystal oxides on Si, GaN, III-V's and overgrowth of semiconductors

Intel (Sematech) Transistor Scaling and Research Roadmap



Device Scaling – Beyond 22 nm node: high k, metal gates, and high mobility channel

1960 Kahng and Atalla, Bell Labs First MOSFET



Metal gate

Higher κ gate dielectric

Oxide/semiconductor Interface ⇒ perfection

High mobility channel

Integration of IIIV, Ge with Si

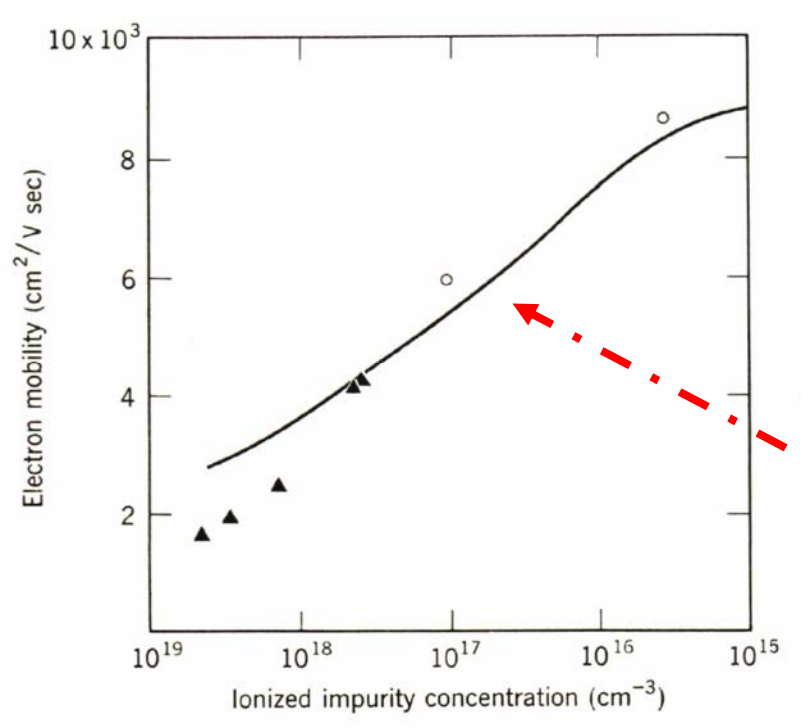
Moore's Law:
The number of transistors per square inch doubles every 18 months

Shorter gate length L
Thinner gate dielectrics t_{ox}

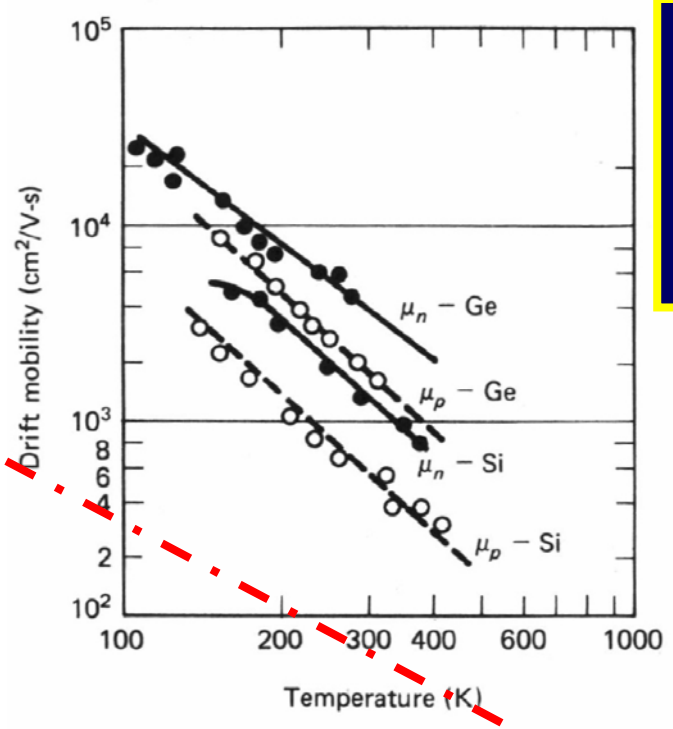
Driving force :
High speed
Lower power consumption
High package density

Electron mobilities in GaAs, Si, and Ge

GaAs



Si and Ge



Measured drift mobility in Si and Ge (F. J. Morin and J. P. Maita, Phys. Rev., 94, 1526, **(1954)** and 96, 28 (1954))

Solid curve: theory with combined polar and ionized-impurity scattering (Ehrenreich: JAP 32, 2155, 1961)
Experimental points o: Reid and Willardson: J. Electronics and Control, 5, 54 **(1958)**
▲: Weisberg, Rosi, and Herkart: Metallurgical Soc. Conf., v.5 "Properties of elemental and compound semiconductors, Interscience Publishers, New York, p.275

DRIFT MOBILITIES (cm^2/ V-s) in Ge, Si, and GaAs at 300K

	Ge		Si		GaAs	
	μ_n	μ_p	μ_n	μ_p	μ_n	μ_p
value at 300K	**3900**	1900	**1400**	470	**8500**	340
Temperature dependence	$T^{-1.66}$	$T^{-2.33}$	$T^{-2.5}$	$T^{-2.7}$	—	$T^{-2.3}$

Do we need a new methodology for GaAs passivation?

A. M. Green and W. E. Spicer
Stanford University
JVST A11(4), 1061, 1993

Sulfur passivation –Sandroff et al, Bell Labs APL51, 33, 1987
Sb passivation – Cao et al, Stanford Surf. Sci. 206, 413, 1988

"A new methodology for passivating compound semiconductors is presented in which two overlayers are used. In this approach, the first layer defines the surface electronically and the second provides long term protection."

Is it possible to have a III-V (GaAs) MOS, similar to SiO_2/Si, in which a low D_{it}, a low electrical leakage current density, thermodynamic stability at high temp. (>800 ℃), single layer of gate dielectric, no S and Sb, etc are achievable?

YES!!!

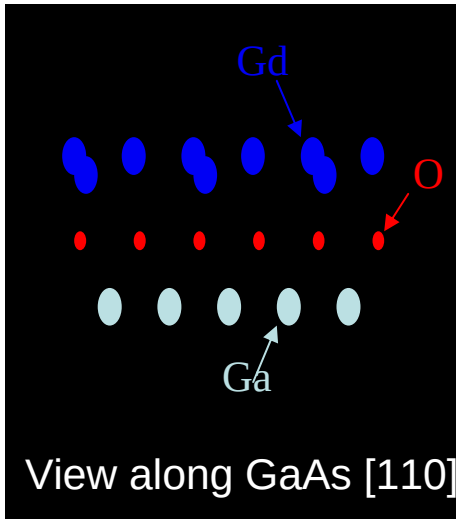
Is it necessary to have GeON as an interfacial layer in Ge MOS?

No!!!

Pioneering work of GaAs and InGaAs MOSFET's using $Ga_2O_3(Gd_2O_3)$ at Bell Labs with single overlayer

- 1994
  - novel oxide $Ga_2O_3(Gd_2O_3)$ to effectively passivate GaAs surfaces
- 1995
  - establishment of accumulation and inversion in p- and n-channels in $Ga_2O_3(Gd_2O_3)$-GaAs MOS diodes with a low D_{it} of 2-3 x 10^{10} cm^{-2} eV^{-1}(IEDM)
- 1996
  - first e-mode GaAs MOSFETs in p- and n-channels with inversion (IEDM)
  - Thermodynamically stable
- 1997
  - e-mode inversion-channel n-InGaAs/InP MOSFET with g_m= 190 mS/mm, Id = 350 mA/mm, and mobility of 470 cm^2/Vs (DRC, EDL)
- 1998
  - d-mode GaAs MOSFETs with negligible drain current drift and hysteresis (IEDM)
  - e-mode GaAs MOSFETs with improved drain current (over 100 times)
  - Dense, uniform microstructures; smooth, atomically sharp interface; low leakage currents
- 1999
  - GaAs power MOSFET
  - Single-crystal, single-domain Gd_2O_3 epitaxially grown on GaAs
- 2000
  - demonstration of GaAs CMOS inverter

Pioneer Work : Single Domain Growth of (110) Gd_2O_3 Films on (100) GaAs



Mn_2O_3 Structure

Gd_2O_3
a= 10.81Å

[001]

[1 $\bar{1}$0]

GaAs
a=5.65Å

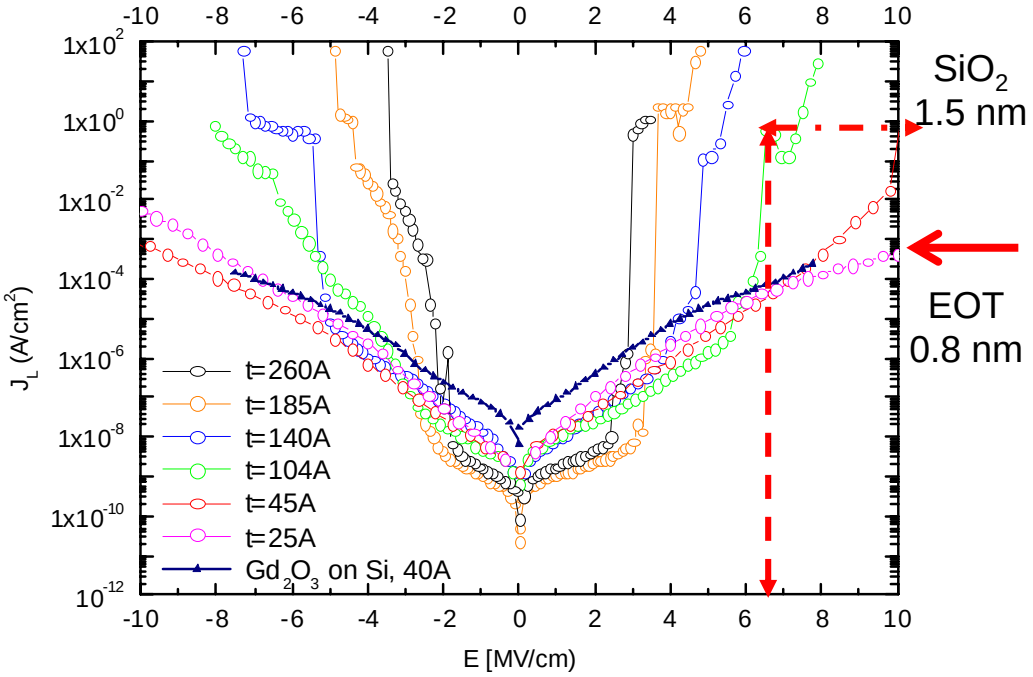
[110]

3: 4 match

[1 $\bar{1}$0]
1: 2 match

M. Hong, J. Kwo et al,
Science 283, p.1897, 1999

Gd_2O_3 (110) 25Å



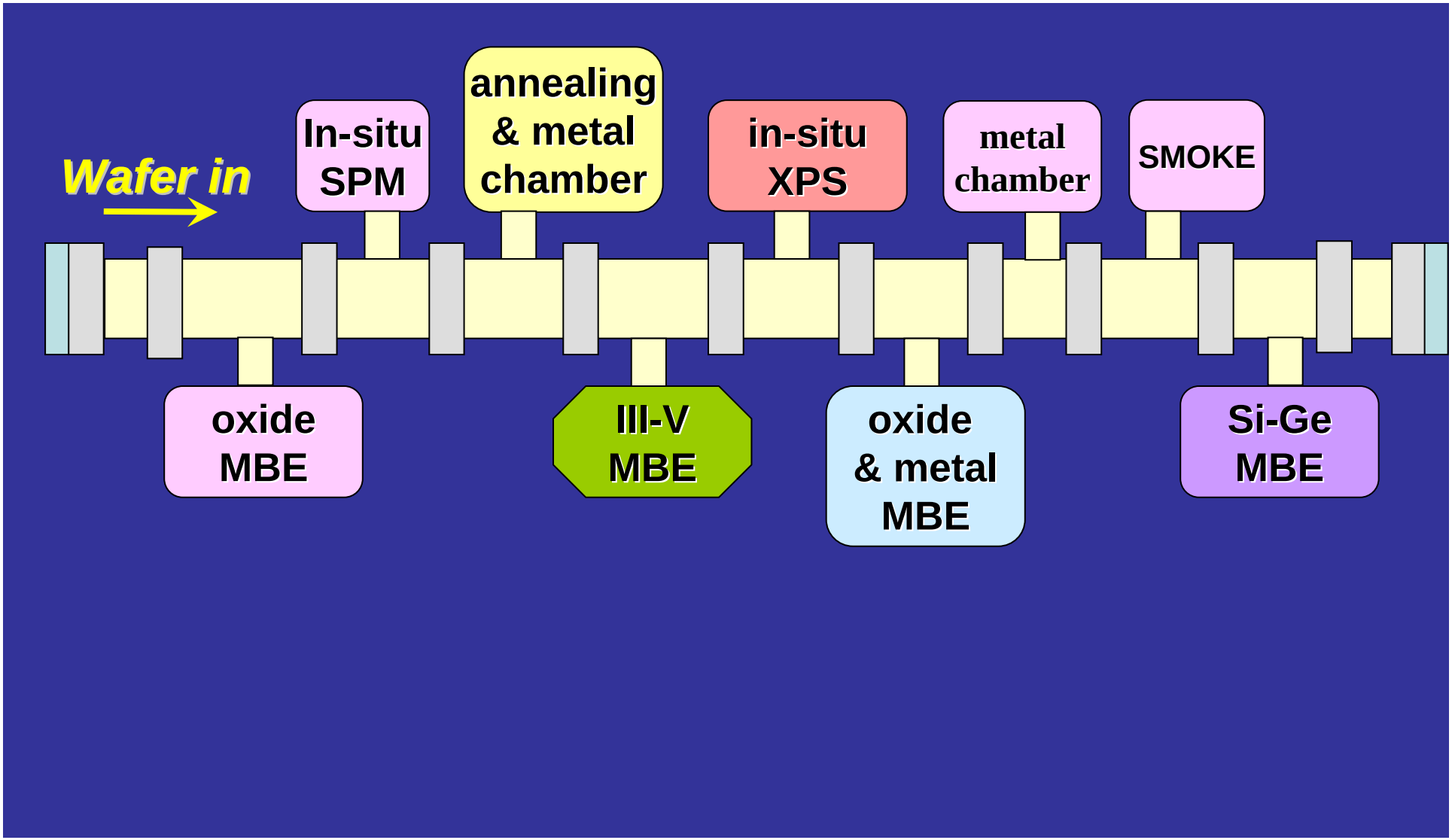
	Si	GaAs	$In_{0.53}Ga_{0.47}As$	GaN	InAs	InSb	units
Energy gap	1.12	1.43	0.75	3.40	0.354	0.17	eV
Lattice constant	5.431	5.65	5.87	3.19	6.06	6.50	Å
Electron effective mass	0.19	0.063	0.041	0.20	0.023	0.014	-
Electron mobility	1500	8500	14000	1300	25000	78000	$cm^2 V^{-1} s^{-1}$
Electron saturation velocity	1×10^7	2×10^7	8×10^6	3×10^7	3×10^7	5×10^7	$cm\ s^{-1}$
Electron mean free path	0.07	0.15	0.19	0.2	0.27	0.58	μm

- MBE – compound semiconductor growth – **A. Y. Cho** (National Medal of Science 1993 and National Medal of Technology 2007)

- MBE – metal and oxide growth – **J. Kwo** (first in discovering anti-ferromagnetic coupling through non-magnetic layer in magnetic superlattices PRL's 1985 – 1986)

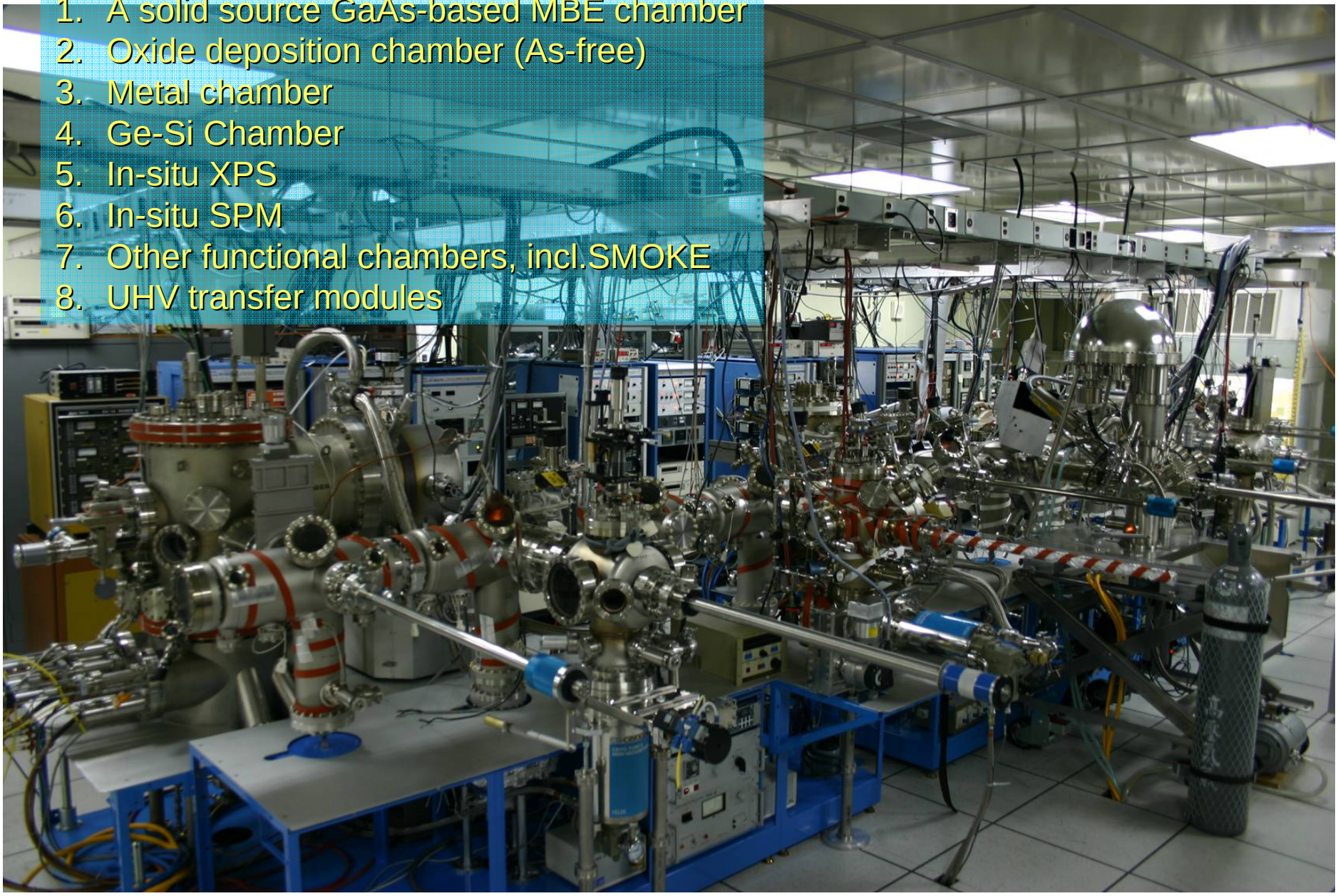
Frank Shu, UC University Professor and former President of Tsing Hua Univ

Multi-chamber MBE/in-situ analysis system



Multichamber Ultrahigh Vacuum System

1. A solid source GaAs-based MBE chamber
2. Oxide deposition chamber (As-free)
3. Metal chamber
4. Ge-Si Chamber
5. In-situ XPS
6. In-situ SPM
7. Other functional chambers, incl.SMOKE
8. UHV transfer modules



1897 J. J. Thomson discovery of electron

1947 The Transistor

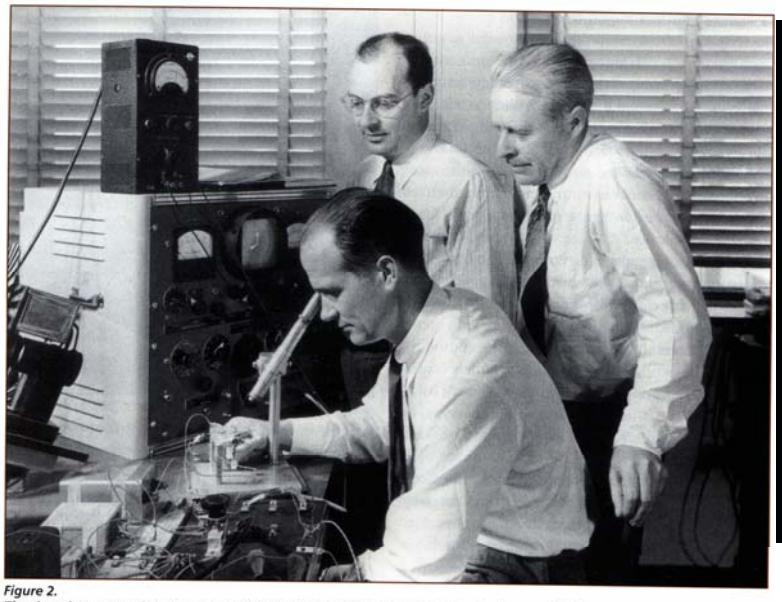
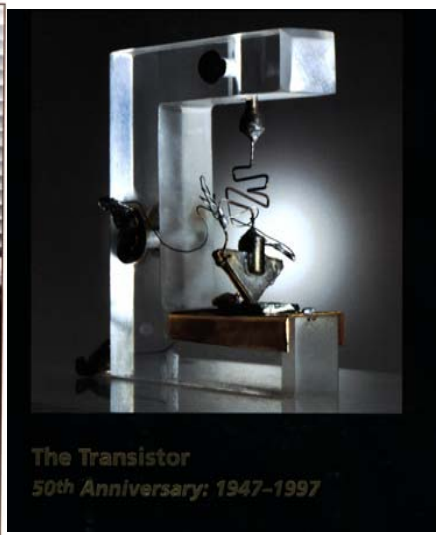


Figure 2.
The three inventors of the transistor: (left to right) William Shockley, John Bardeen, and Walter Brattain, who were awarded the 1956 Nobel Prize in physics.



2007 High k + metal gate on 45 nm node CMOS

What next – IIIV, GaN, or Ge MOS in 2017?

- Mervin Kelly, the then Director of Res. at Bell Labs, had predicted the problem and had already taken action to find a solution.
  - Although relays and vacuum tubes were apparently making all things possible in telephony, he had predicted for some years that the low speed of relays and the short life and high power consumption of tubes would eventually limit further progress in telephony and other electronic endeavors.
  - In the summer of 1945, Kelly had established a research group at Bell Labs to focus on the understanding of semiconductors. The group also had a long-term goal of creating a solid-state device that might eventually replace the tube and the relay.

- Surface Fermi level unpinning in III-V's (the Holy Grail), Ge
  - UHV deposited $Ga_2O_3(Gd_2O_3)$; ALD-HfO_2 and Al_2O_3 on InGaAs; $Ga_2O_3(Gd_2O_3)$/Ge
- Thermodynamic stability of $Ga_2O_3(Gd_2O_3)$/III-V's; Ge: temp. limit
- $Ga_2O_3(Gd_2O_3)$/InGaAs oxide scalability: EOT scalability
- YDH (yttrium doped HfO_2) – novel high k gate dielectric
- ALD/MBE approach: complete elimination of interfacial layers
- Inversion-channel GaAs-based and GaN MOSFET's
- Single crystal oxides on Si(111)
  - GaN/gamma- Al_2O_3, Sc_2O_3/Si(111); ZnO/- - -/Si (111)
- Oxides/GaN
- IETS
- In-situ SPM, SMOKE, XPS
- Spintronics
  - Spin LED; Andreev Reflection
  - Fe_3Si/GaAs, magnetic/single crystal oxides/magnetic
  - Dilute magnetic Co-HfO_2
  - Spin FET

- InGaAs, GaN, and Ge
  - Surface Fermi level unpinning
    - Necessity of interfacial layers
  - UHV deposited $Ga_2O_3(Gd_2O_3)$; ALD-HfO_2 and Al_2O_3
    - Electrical characteristics: J-E; C-V; D_{it}
    - EOT (CET) scalability
  - Thermodynamic stability: temp. limit
- Higher k dielectrics
  - YDH (yttrium doped HfO_2) – novel high k gate dielectric
- ALD/MBE approach: complete elimination of interfacial layers in Si and Ge
- Inversion-channel InGaAs, Ge, and GaN MOSFET's
- Metal gates
- Integration of InGaAs, Ge, and GaN with Si
- Single crystal oxides on Si(111)
  - GaN/gamma- Al_2O_3, Sc_2O_3/Si(111); ZnO/- - -/Si (111)
- Oxides/GaN
- IETS
- In-situ SPM, XPS