Defining New Frontiers in Electronic Devices with high k dielectrics and interfacial engineering

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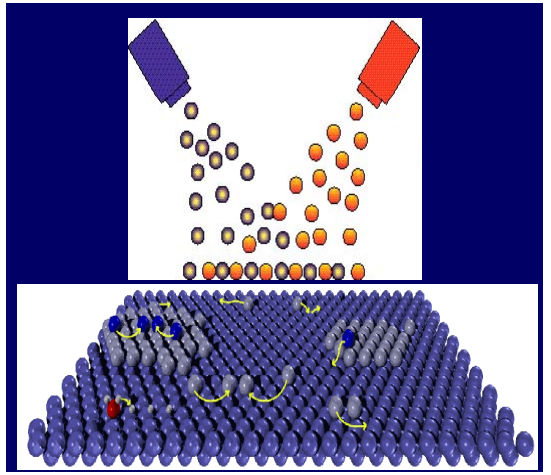
- The quest for the III-V and Ge MOSFET

- Nano single crystal oxide on semiconductor
– the structural perfection and applications for devices

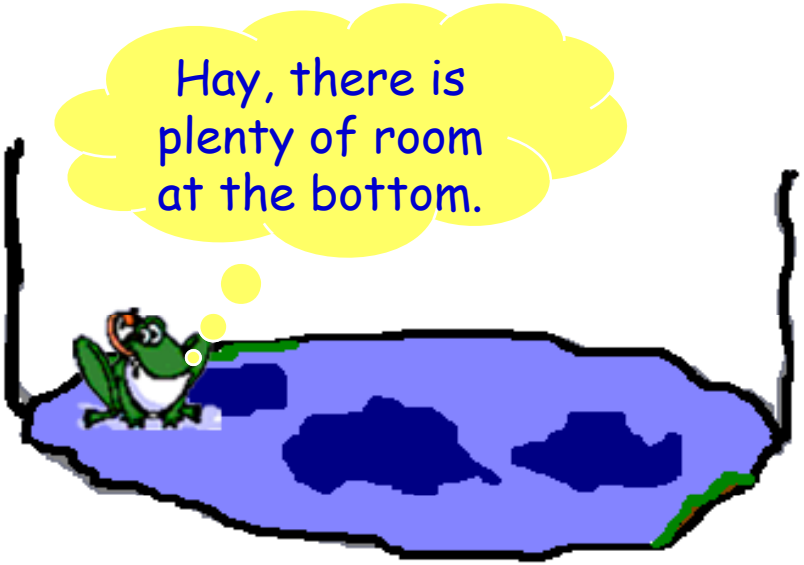
There's Plenty of Room at the Bottom

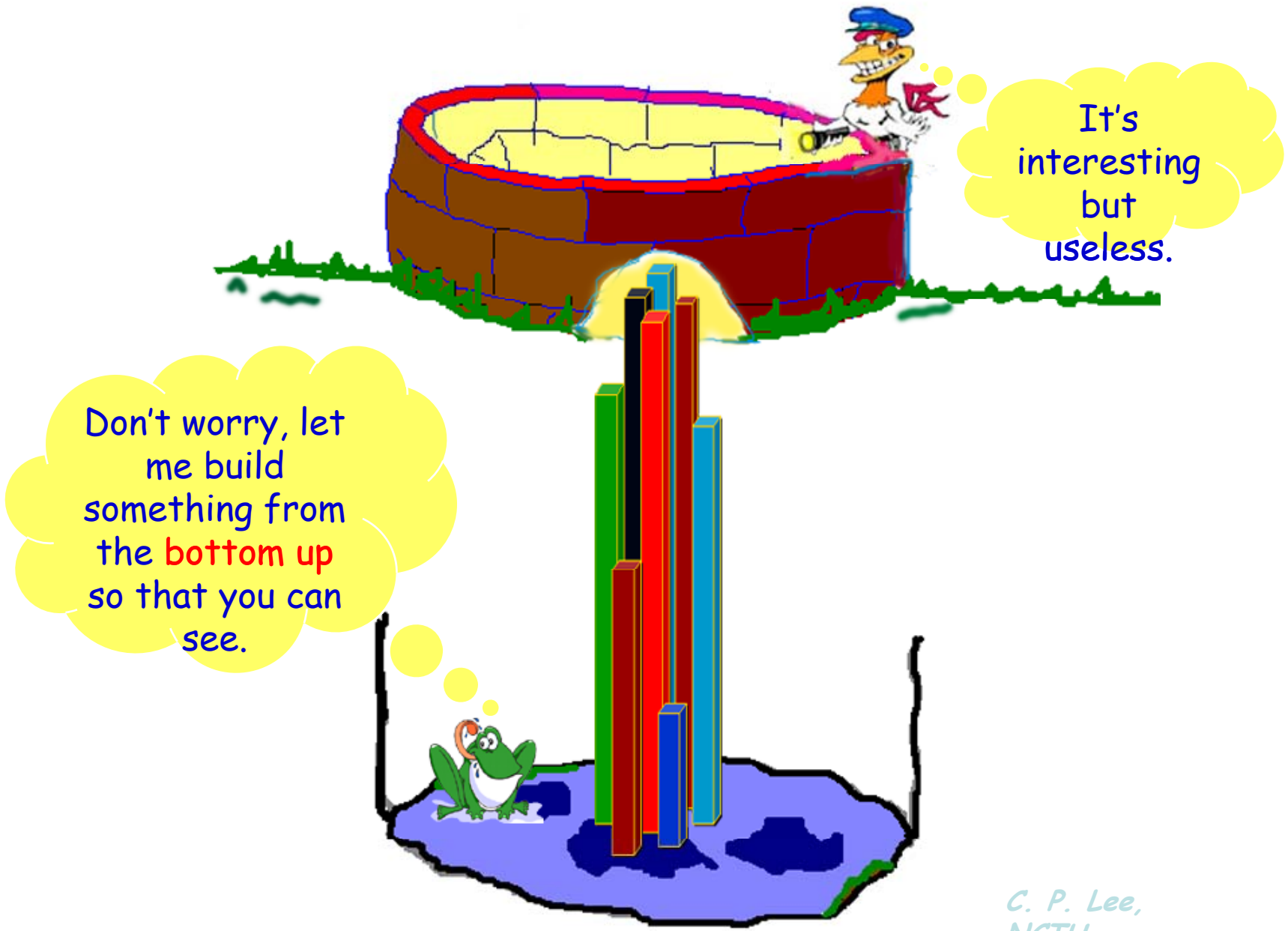
An Invitation to Enter a New Field of Physics

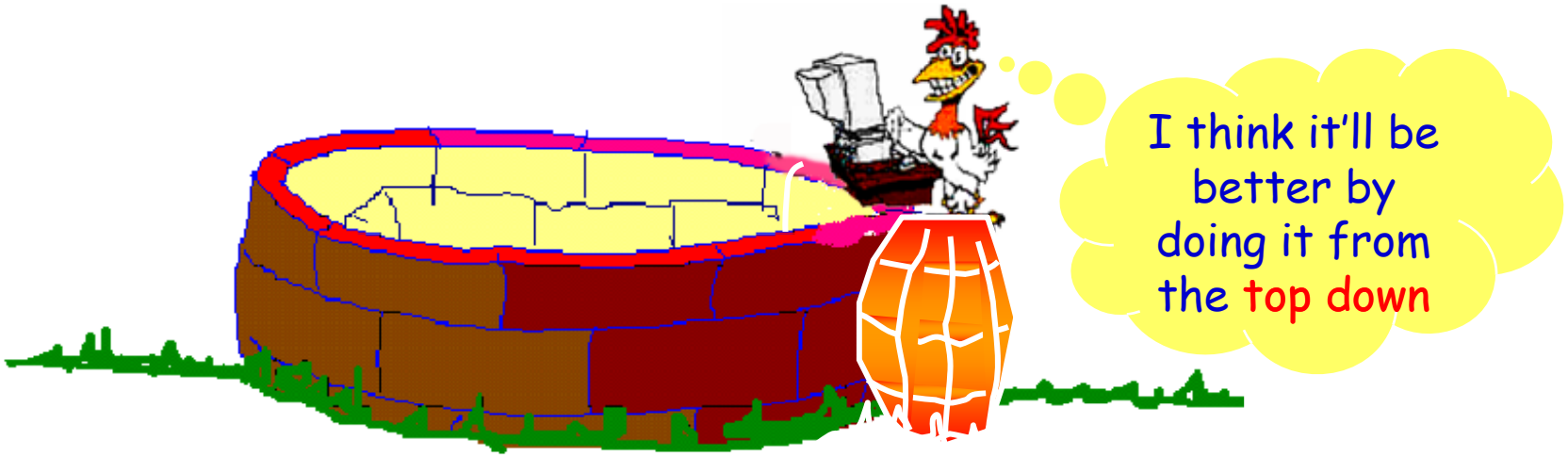
by Richard P. Feynman




Where is the
bottom ?
I can't see.


Hay, there is
plenty of room
at the bottom.


It's interesting but useless.
Don't worry, let me build something from the bottom up so that you can see.
C. P. Lee, NCTU


I think it'll be better by doing it from the top down


Stop ! It's going to land in water.

C. P. Lee,
NCTU

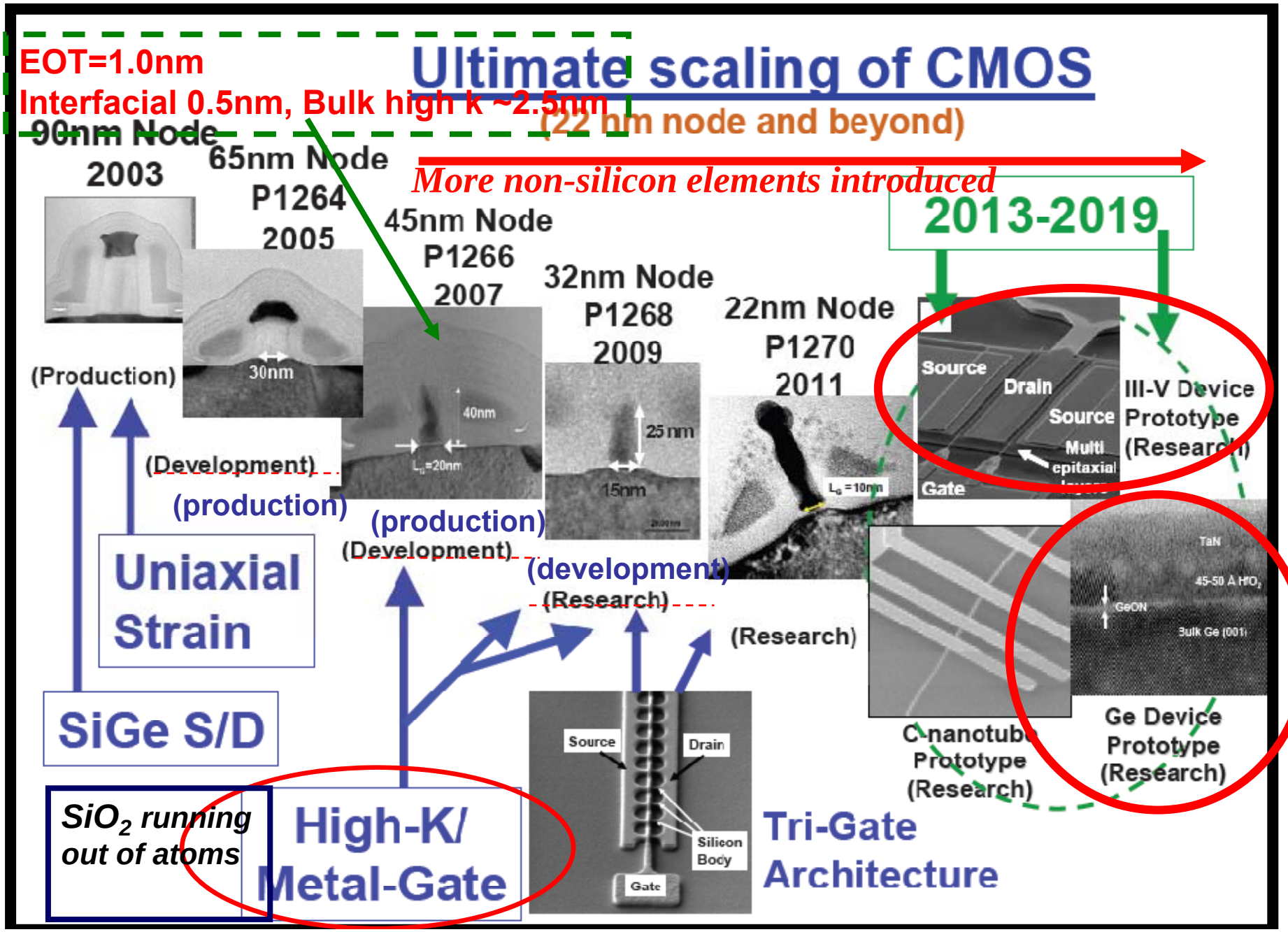
General observation

- You lead, follow, or get out of the way
  - Lee Iococa of Chrysler
- Three types of researchers
  - Leading
  - Following very closely
  - Wondering and not knowing what to do
- Either scientifically very interesting or technologically very useful. The best is to have both and the worst is to have neither.

motivation

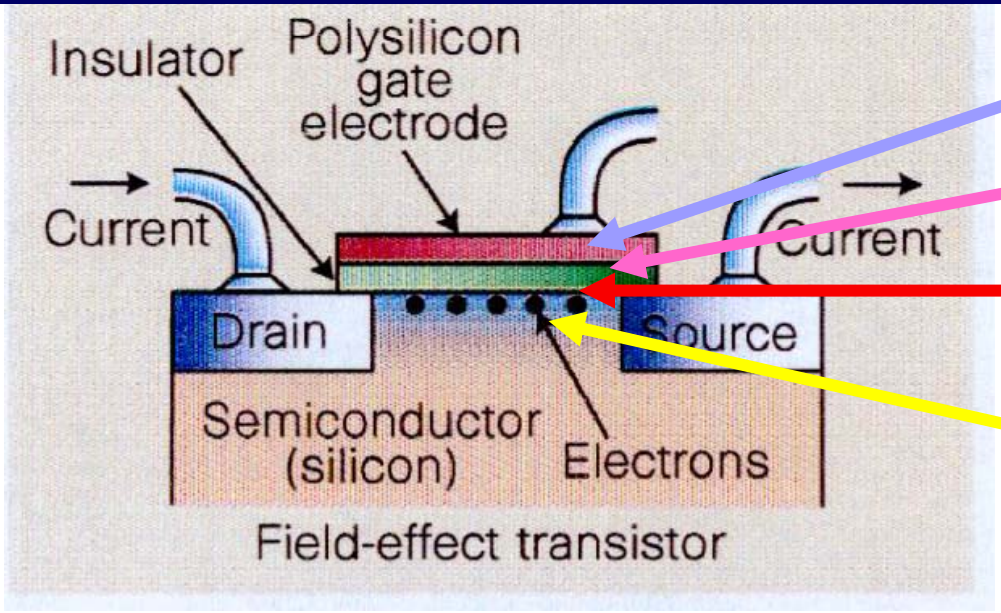
- Rapid shrinkage of transistor size in Si industry
  - devices of gate length of 65 nm in production, of 50 nm or smaller in R&D, with channel length ~ 15 nm by 2010, and SiO_2 thickness to quantum tunneling limit of 1.0nm
- Called for replacing SiO_2 with high k dielectrics
  - equivalent oxide thickness (EOT) as thin as 1.0 nm or less
- Coulomb scattering from charge trapping and phonon issue related to high k gate dielectrics leading to degraded channel mobility
  - higher mobility materials such as strained Si, Si-Ge alloys, Ge, and IIIV's
- Ge offers two times higher mobility for electrons and four times higher for holes comparing with Si
  - renewing interest in Ge-based devices. Unlike Si, lack of sufficiently stable native oxide hindering passivation of Ge surfaces, making fabrication of Ge MOSFET difficult
- III-V semiconductors, such as GaAs, InSb, GaN, and their related compounds.
  - electron mobility in III-V's much higher than those in Si and Ge
- A mature III-V MOS technology with electron mobilities at least 10 times higher than that in Si and with dielectrics having k several times higher that that of SiO_2 would certainly enable the electronic industry to continue pushing its new frontiers for a few more decades
  - bandgap engineering and direct bandgaps in the III-V's, not available in Si- and Ge-based systems, providing novel designs and making highly-performed integrated optoelectronic circuits of combining MOS and photonic devices a reality

Intel (Sematech) Transistor Scaling and Research Roadmap



Device Scaling – Beyond 22 nm node: high k, metal gates, and high mobility channel

1960 Kahng and Atalla, Bell Labs First MOSFET



Metal gate

High κ gate dielectric

Oxide/semiconductor interface

High mobility channel

Integration of IIIV, Ge with Si

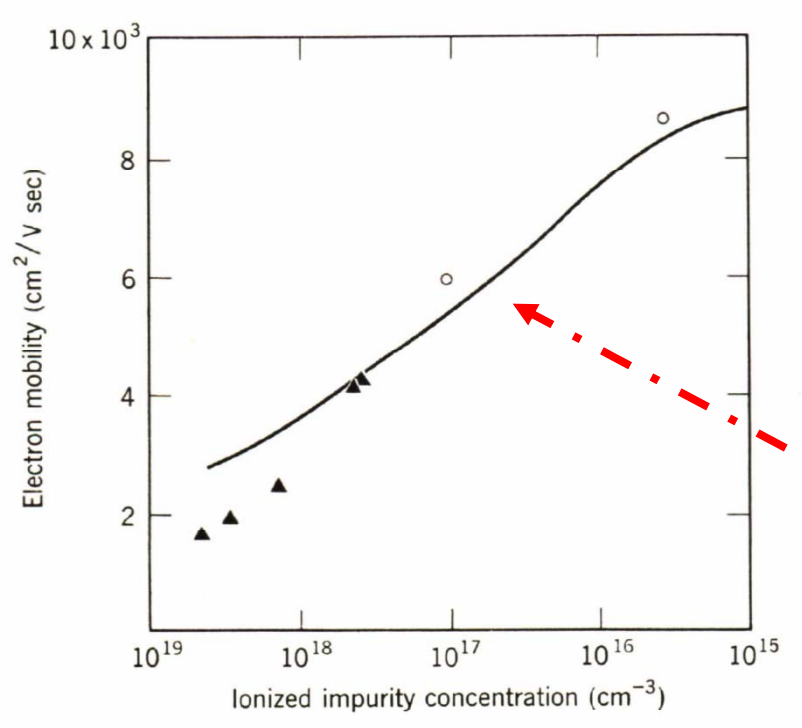
Moore's Law:
The number of transistors per square inch doubles every 18 months

Shorter gate length L
Thinner gate dielectrics t_{ox}

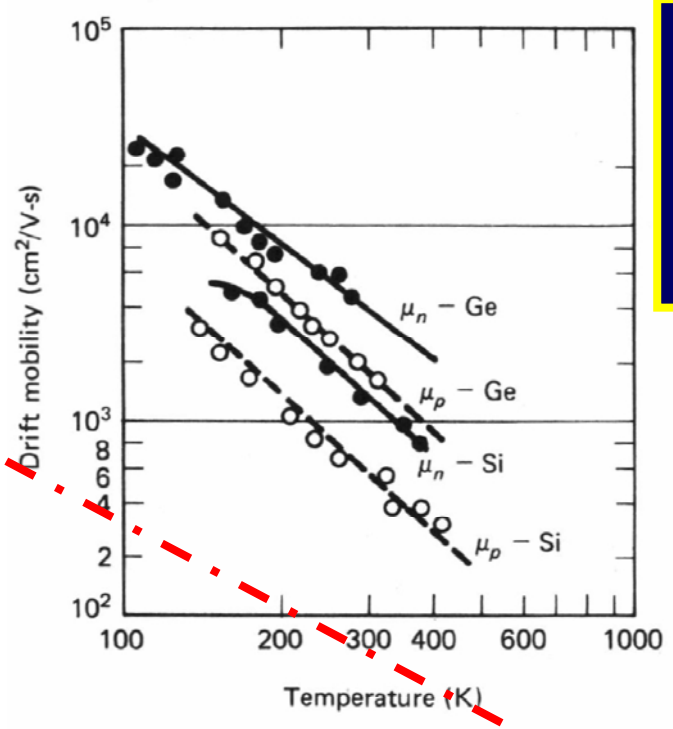
Driving force :
High speed
Lower power consumption
High package density

Electron mobilities in GaAs, Si, and Ge

GaAs



Si and Ge



Measured drift mobility in Si and Ge (F. J. Morin and J. P. Maita, Phys. Rev., 94, 1526, **(1954)** and 96, 28 (1954))

Solid curve: theory with combined polar and ionized-impurity scattering (Ehrenreich: JAP 32, 2155, 1961)
Experimental points o: Reid and Willardson: J. Electronics and Control, 5, 54 **(1958)** ▲: Weisberg, Rosi, and Herkart: Metallurgical Soc. Conf., v.5 "Properties of elemental and compound semiconductors, Interscience Publishers, New York, p.275

DRIFT MOBILITIES (cm^2/ V-s) in Ge, Si, and GaAs at 300K

	Ge		Si		GaAs	
	μ_n	μ_p	μ_n	μ_p	μ_n	μ_p
value at 300K	**3900**	1900	**1400**	470	**8500**	340
Temperature dependence	$T^{-1.66}$	$T^{-2.33}$	$T^{-2.5}$	$T^{-2.7}$	—	$T^{-2.3}$

Do we need a new methodology for GaAs passivation?

A. M. Green and W. E. Spicer
Stanford University
JVST A11(4), 1061, 1993

Sulfur passivation –Sandroff et al, Bell Labs APL51, 33, 1987
Sb passivation – Cao et al, Stanford Surf. Sci. 206, 413, 1988

"A new methodology for passivating compound semiconductors is presented in which two overlayers are used. In this approach, the first layer defines the surface electronically and the second provides long term protection."

Is it possible to have a III-V (GaAs) MOS, similar to SiO_2/Si, in which a low D_{it}, a low electrical leakage current density, thermodynamic stability at high temp. (>800 ℃), single layer of gate dielectric, no S and Sb, etc are achievable?

YES!!!

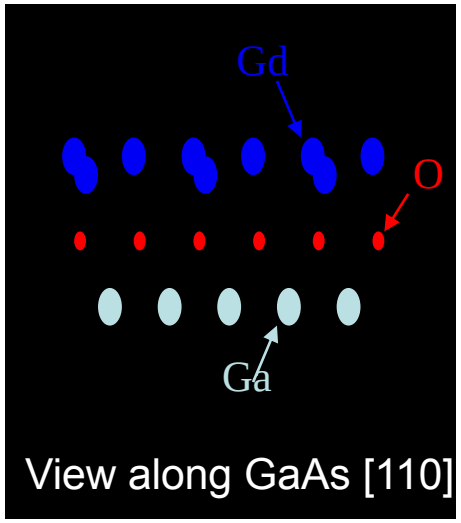
Is it necessary to have GeON as an interfacial layer in Ge MOS?

No!!!

Pioneering work of GaAs and InGaAs MOSFET's using $Ga_2O_3(Gd_2O_3)$ at Bell Labs with single overlayer

- 1994
  - novel oxide $Ga_2O_3(Gd_2O_3)$ to effectively passivate GaAs surfaces
- 1995
  - establishment of accumulation and inversion in p- and n-channels in $Ga_2O_3(Gd_2O_3)$-GaAs MOS diodes with a low D_{it} of 2-3 x 10^{10} cm^{-2} eV^{-1}(IEDM)
- 1996
  - first e-mode GaAs MOSFETs in p- and n-channels with inversion (IEDM)
  - Thermodynamically stable
- 1997
  - e-mode inversion-channel n-InGaAs/InP MOSFET with g_m= 190 mS/mm, Id = 350 mA/mm and mobility of 470 cm^2/Vs (DRC, EDL)
- 1998
  - d-mode GaAs MOSFETs with negligible drain current drift and hysteresis (IEDM)
  - e-mode GaAs MOSFETs with improved drain current (over 100 times)
  - Dense, uniform microstructures; smooth, atomically sharp interface; low leakage currents
- 1999
  - GaAs power MOSFET
  - Single-crystal, single-domain Gd_2O_3 epitaxially grown on GaAs
- 2000
  - demonstration of GaAs CMOS inverter

Pioneer Work : Single Domain Growth of (110) Gd_2O_3 Films on (100) GaAs



Mn_2O_3 Structure

(110)

Gd_2O_3
a= 10.81Å

[1 $\bar{1}$0]

[001]

(100)

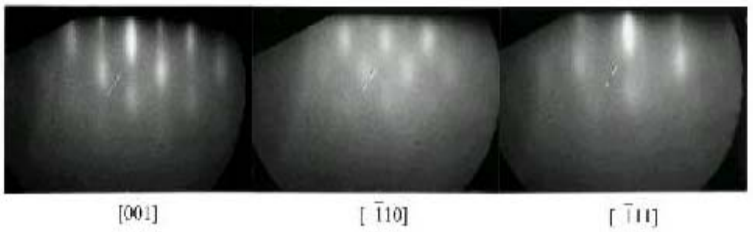
GaAs
a=5.65Å

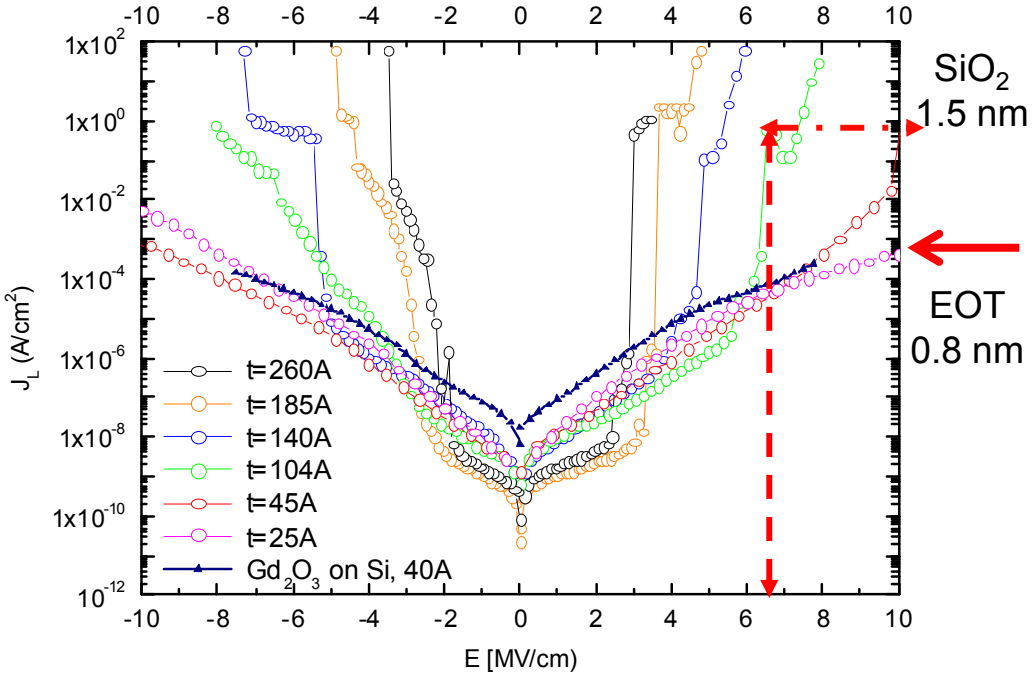
[1 $\bar{1}$0]
1: 2 match

[110]
3: 4 match

M. Hong, J. Kwo et al,
Science 283, p.1897, 1999

Gd_2O_3 (110) 25Å





- MBE – compound semiconductor growth – A. Y. Cho (National Medal of Science 1993 and National Medal of Technology 2007)

- MBE – metal and oxide growth – J. Kwo (first in discovering anti-ferromagnetic coupling through non-magnetic layer in magnetic superlattices PRL's 1985 – 1986)

Frank Shu, UC University Professor and former President of Tsing Hua Univ.

MBE – compound semiconductor growth

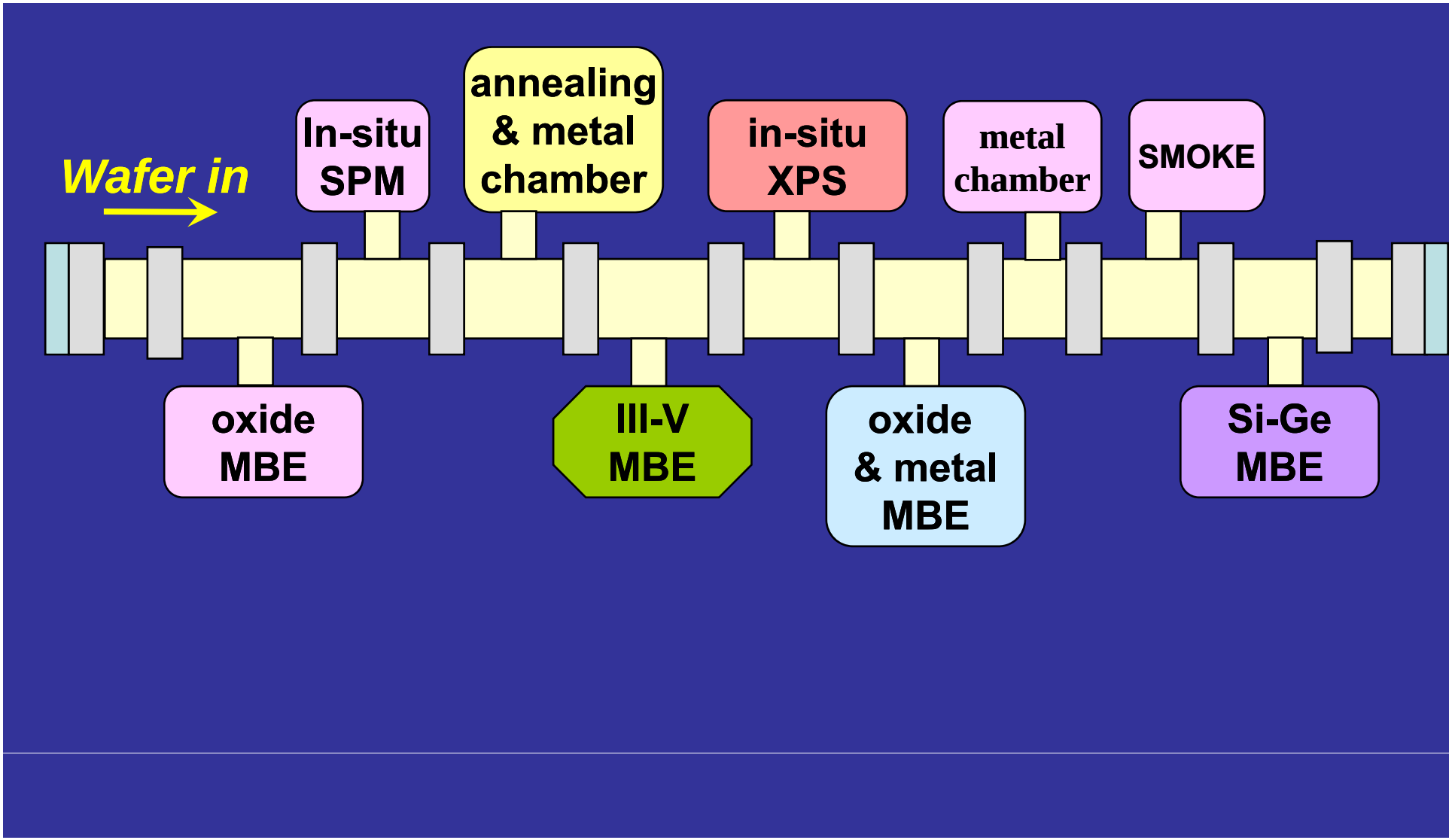
- Alfred Y. Cho (卓以和) and co-workers
- RHEED (reflection high energy electron diffraction)
- Liquid nitrogen shroud
- Load-lock chamber vs single chamber (New Jersey humid weather affecting semiconductor laser life time)
- Ion pump, cryo-pump, turbo pump, mercury pump, diffusion pump, dry pump, mechanical pump, absorption pump, etc
- Effusion cells
- Flux gages
- Manipulator
- Heaters
- GaAs wafer surface oxide absorption

MBE – metal and oxide growth

- Raynien Kwo (郭瑞年) and co-workers
- Electron mean-free path
  - In metals vs in semiconductors
- Metal superlattices
  - Historical background
    - Cu-Ni compositional multi-layers
      - Enhancement of magnetic moments and elastic modules
- Magnetism
  - Rare earth superlattices
    - Long range coupling
      - Ferro- and anti-ferro-magnetic coupling
  - GMR
- Non-alloyed ohmic contacts
- Schottky barrier
- Silicide (WSi, CoSi, etc) on Si
  - Metal base transistors
- $Fe_3(Al,Si)$, CoNi, etc on GaAs

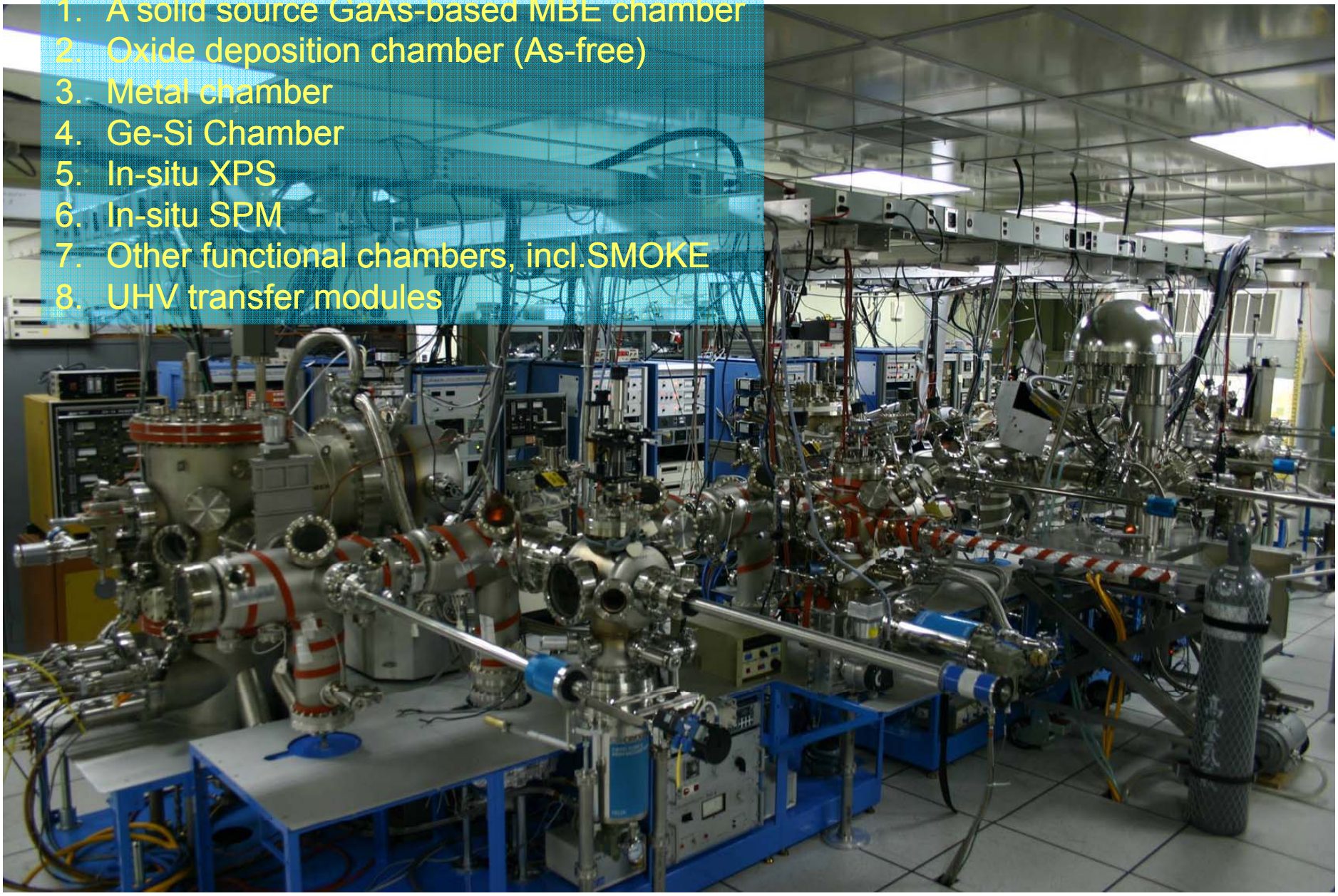
- MBE growth chamber
  - RHEED
  - Liquid nitrogen shroud
  - Load-lock chamber vs single chamber (humid weather in Taiwan)
  - Ion pump, cryo-pump, turbo pump, diffusion pump, dry pump, mechanical pump, absorption pump, etc
  - Effusion cells and e-guns
  - Charges (or source materials)
  - Flux gages
  - Manipulator
  - Heaters
  - substrates? Unlike GaAs or Si growth

Multi-chamber MBE/in-situ analysis system



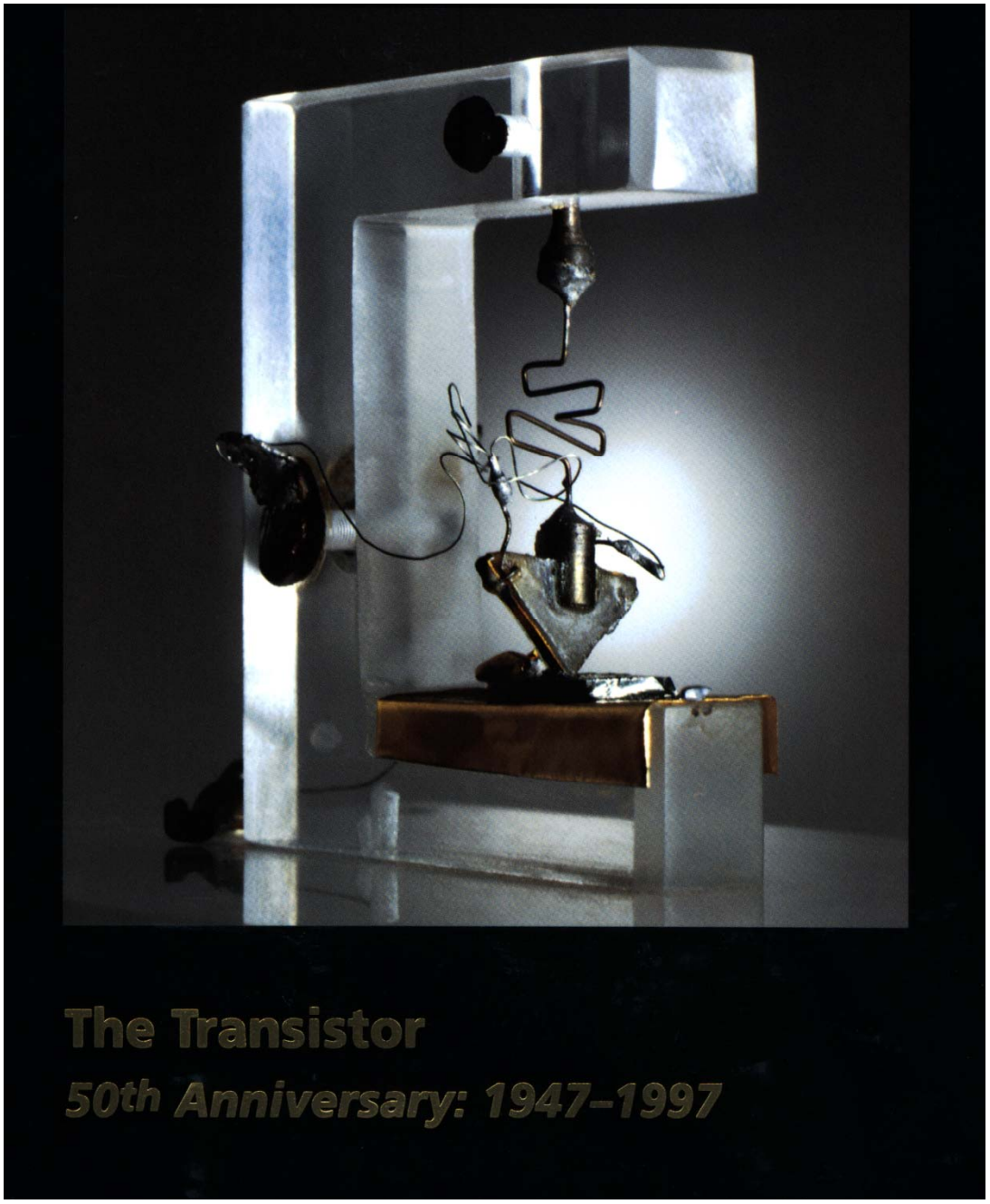
Multichamber Ultrahigh Vacuum System

1. A solid source GaAs-based MBE chamber
2. Oxide deposition chamber (As-free)
3. Metal chamber
4. Ge-Si Chamber
5. In-situ XPS
6. In-situ SPM
7. Other functional chambers, incl.SMOKE
8. UHV transfer modules



1897 J. J. Thomson

discovery of electron



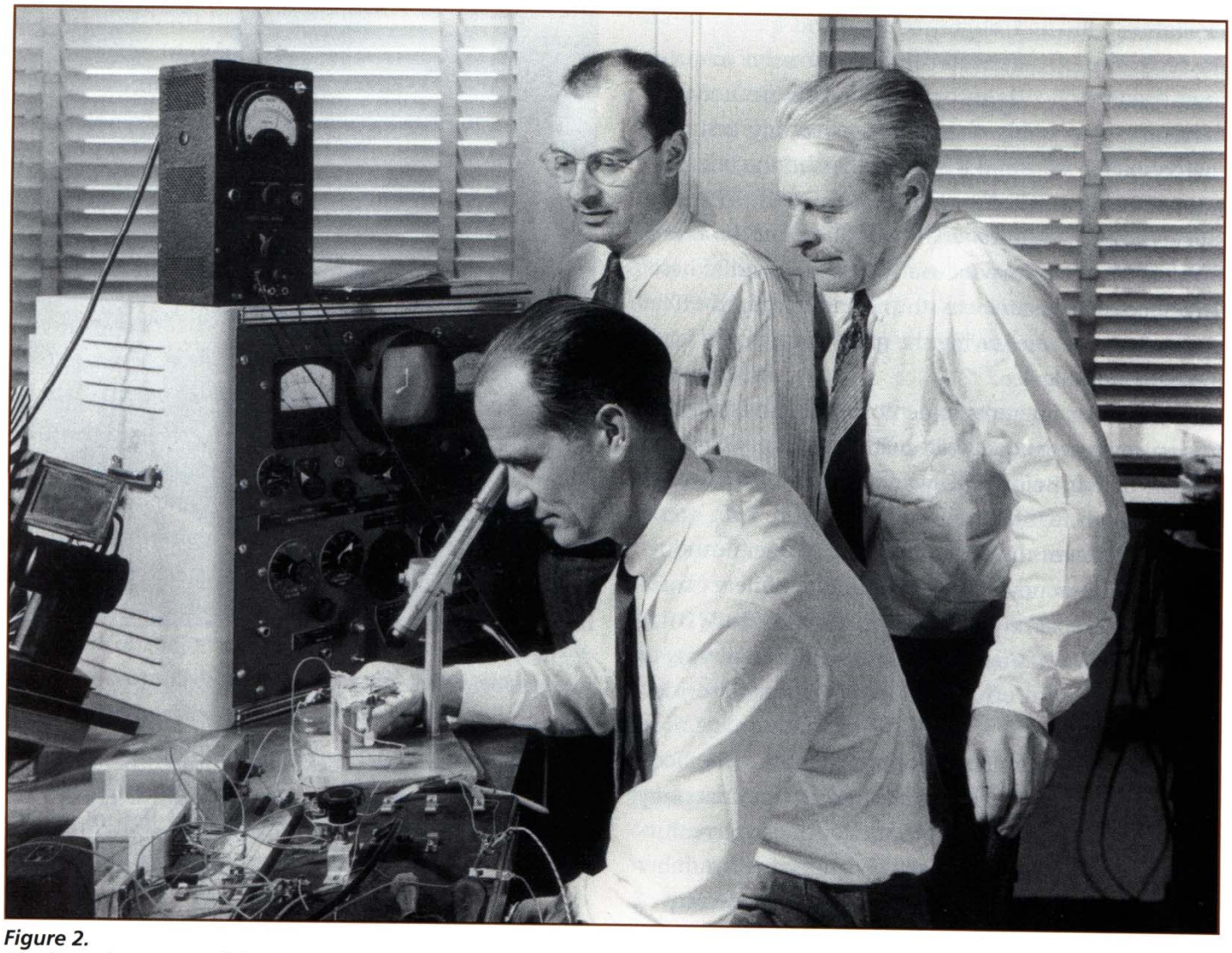


Figure 2.
The three inventors of the transistor: (left to right) William Shockley, John Bardeen, and Walter Brattain, who were awarded the 1956 Nobel Prize in physics.

William Shockley, John Bardeen, and Walter Brattain, Bell Labs

In the summer of 1947, any of a number of technical societies could have held a symposium to commemorate the 50th anniversary of J. J. Thomson's discovery of the electron. That 1947 event could surely qualify as the start of the electronics discipline and the industry that followed. It was the new understanding of the properties of the electron that created the field of electronics, and that, combined with our developing capability in the electrical, magnetic, and mechanical arts, enabled a rich array of new products and services.

The symposium would have been an upbeat event. Vacuum tube technology had fully matured with a wide range of tubes – diodes, pentodes, CRTs, klystrons, and traveling-wave tubes – in high-volume manufacture. Vacuum tubes were the key component in an array of electronic equipment that seemed to meet all conceivable information needs.

Mervin Kelly, the then Director of Research at Bell Labs who later became Bell Labs president, might well have been invited to submit a paper to the symposium. And he would also have been upbeat. Electromechanical relay technology was making possible fully automatic telephone dialing and switching. Microwave radio was providing high-quality telephone transmission across the continent. Again, available technology appeared capable of meeting conceivable needs.

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Yet Kelly would have raised a word of caution. Although relays and vacuum tubes were apparently making all things possible in telephony, he had predicted for some years that the low speed of relays and the short life and high power consumption of tubes would eventually limit further progress in telephony and other electronic endeavors.

Not only had he predicted the problem, he had already taken action to find a solution.

In the summer of 1945, Kelly had established a research group at Bell Labs to focus on the understanding of semiconductors. The group also had a long-term goal of creating a solid-state device that might eventually replace the tube and the relay.

Kelley's vision trigged one of the most remarkable technical odysseys in the history of mankind, a journey that has continued through fifty years and longer. The semiconductor odyssey produced a revolution in our society at least as profound as the introduction of steel, of steam engines and the total Industrial Revolution. Today electronics pervades our lives and affects everything we do.

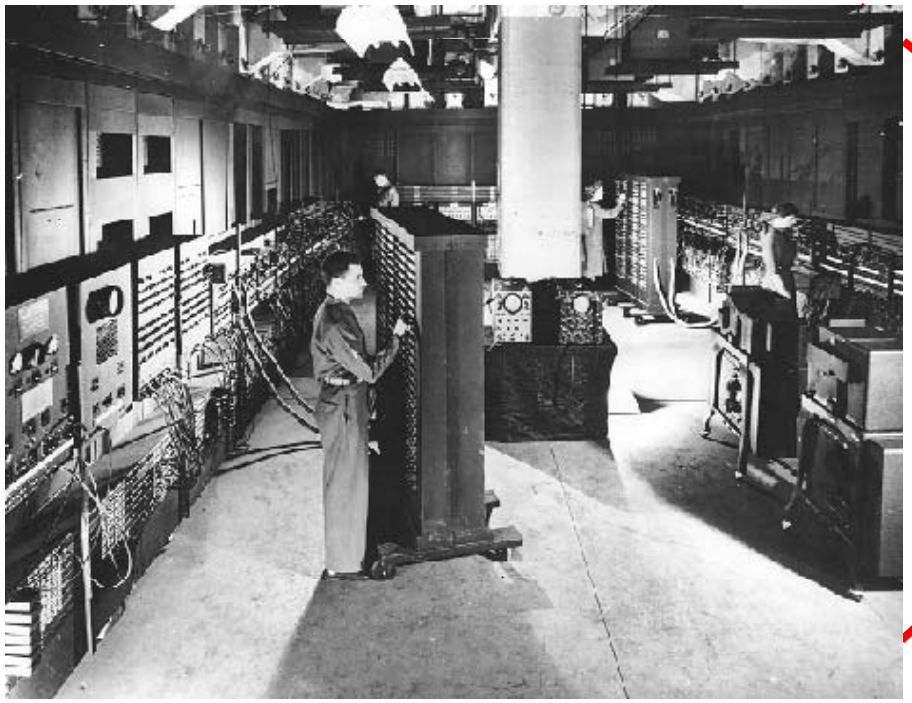
The progress made by semiconductor physics, from what was described by Wolfgang Pauli as 'Physik der Dreckeffekte' or 'dirt physics' in 1920s, over the eight decades or so of the last century is truly amazing. The technological revolution unfolded by this progress has ushered in a new epoch in human civilization. The information age is but a spin-off of this revolution. Arguably no other field of human endeavor has had such a profound and wide ranging impact on human society over the last century. The story of this march from 'dirt physics' to such subtle and complex effects as the fractional quantum Hall effect (FQHE) is full of numerous exciting thrills ranging from our deeper understanding of the defect (dirt) states and how to control them to a level where semiconductors rank among the cleanest man-made materials with unparalleled purity, so high as to exhibits ever unknown physical phenomena such as FQHE and Wigner crystallization.

(Semiconductor hetero-structures (AlGaAs-GaAs) made by MBE.)

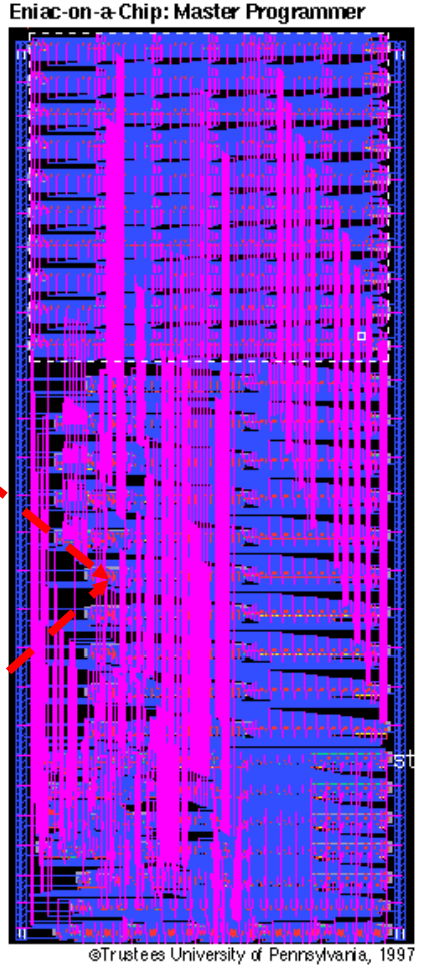
But what has really reached the common man out of this progress is the phenomenal range of electronic applications which have unleashed a flood of consumer goods and communication gadgets, starting from the wireless radio to the present day personal computer and the mobile phone, coupled with the software resolution engendered by the Internet.

I think that there's a world market for about 5 computers.

Thomas J. Waston, Sr.
IBM Chairman of the Board, ca1946



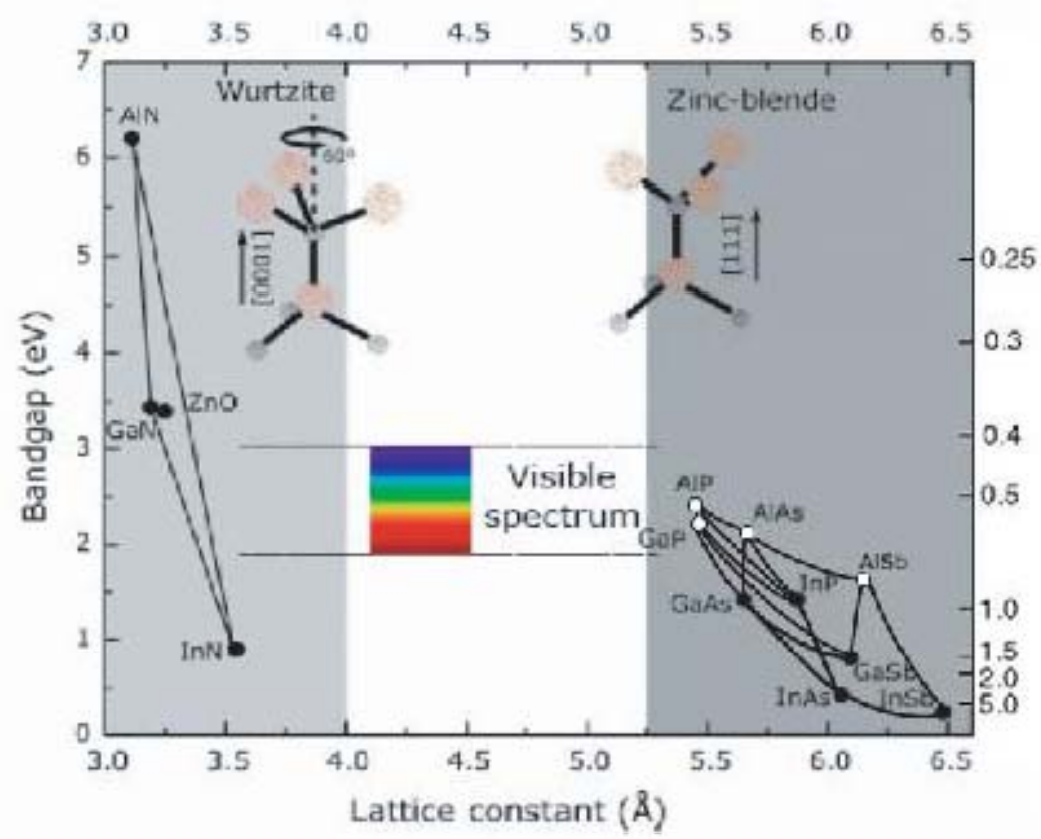
The ENIAC machine occupied a room 30 x 50 ft. (van Pelt Library, U Penn)



Size: **7.44mm x 5.29mm**; 174,569 transistors; 0.5 um CMOS technology

Advantage of GaN-based electronic devices

High Temperature, High Power and High Frequency Applications



	Si	GaAs	GaN
Bandgap(eV)@300 ° C	1.1 indirect	1.4 direct	3.4 direct
Electron mobility (cm2/V · s),RT	1400	8500	1000(bul 2000(2D
Hole Mobility (cm2/V · s),RT	600	400	30
Saturation velocity (cm/s),10^7	1	2	2.5
Breakdown field(V/cm), 10^6	0.3	0.4	>5
Thermal conductivity (W/cm)	1.5	0.5	1.5
Melting temperature(K)	1690	1510	>1700

- High temperature applications due to intrinsic wide band gap
- High breakdown field for power applications
- Excellent electron transport properties
- Heterostructure available

The drive for alternative high k dielectrics (for replacing SiO_2) and metal gates initiated a decade ago has resulted in a recent ***Intel's news announcement of high k + metal gate transistor breakthrough on 45 nm microprocessors,*** indeed a scientific and technological achievement. The high k dielectrics have shown impressive properties with an equivalent oxide thickness (EOT), defined as teq (k_{SiO2} /k_{oxide}), as thin as or even less than 1.0 nm. These relevant parameters include dielectric constant, band gap, conduction band offset, leakage, mobility, and good thermodynamic stability in contact with Si up to 1000ºC. However, Coulomb scattering from charge trapping and the phonon issue related to high k gate dielectrics leads to degraded channel mobility.

It is adamant with consensus that beyond the 22 nm node technology, higher mobility-channel materials such as III-V compound semiconductors and Ge have to be employed.

	Si	GaAs/$In_{0.2}Ga_{0.8}As$	InP/ $In_{0.53}Ga_{0.47}As$/ $In_{0.7}Ga_{0.3}As$	GaN	InAs	InSb	units
Energy gap	1.12	1.43	0.75	3.40	0.354	0.17	eV
Lattice constant	5.431	5.65	5.87	3.19	6.06	6.50	Å
Electron effective mass	0.19	0.063	0.041	0.20	0.023	0.014	-
Electron mobility	1500	8500	14000	1300	25000	78000	$cm^2 V^{-1} s^{-1}$
Electron saturation velocity	1×10^7	2×10^7	8×10^6	3×10^7	3×10^7	5×10^7	$cm\ s^{-1}$
Electron mean free path	0.07	0.15	0.19	0.2	0.27	0.58	μm

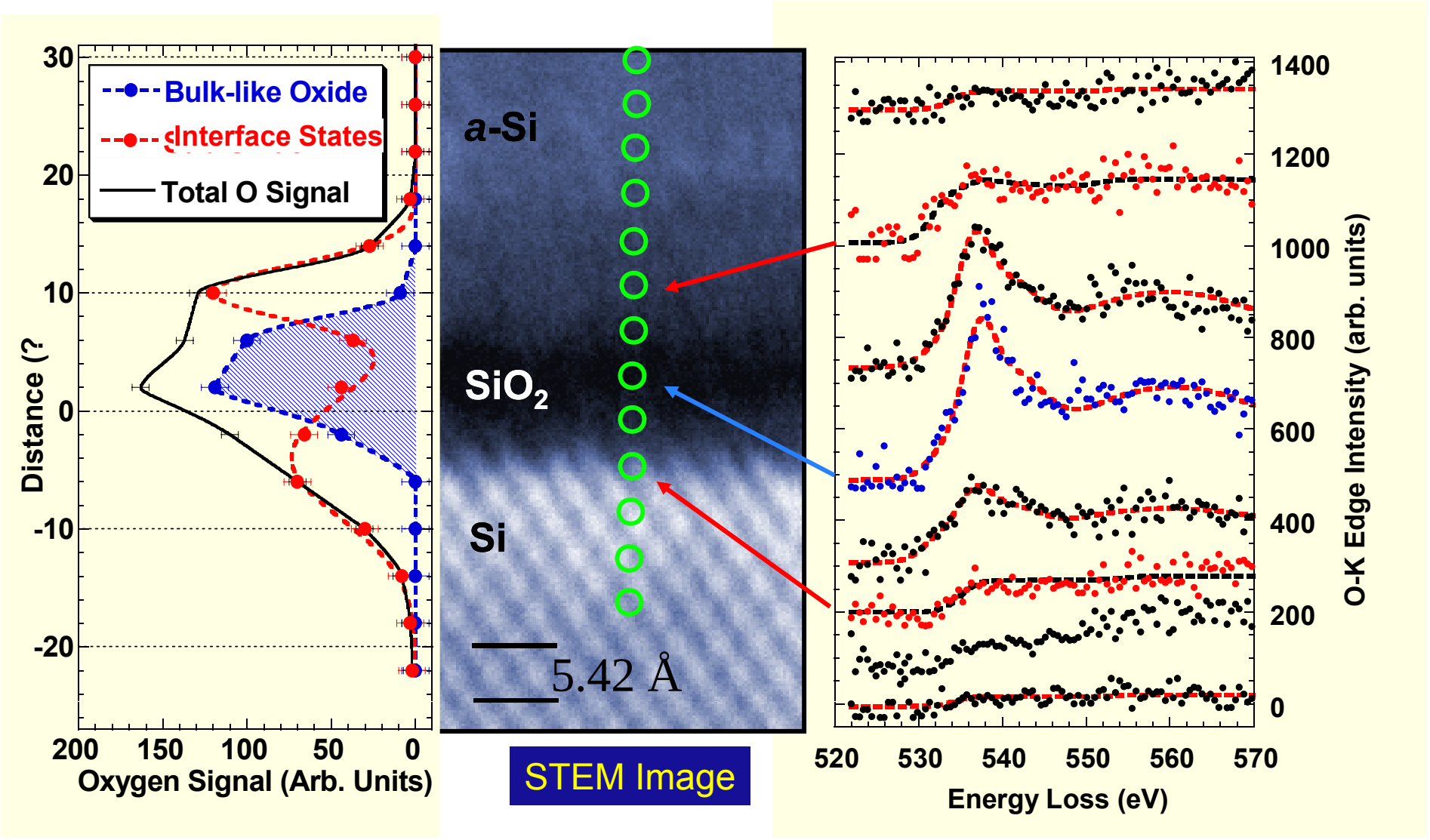
Motivation

- Rapid shrinkage of transistor size in Si industry
  - 65 nm node in production, 50 nm or smaller in R&D, with channel length ~ 10 nm by 2010, and SiO_2 thickness to quantum tunneling limit of 1.0nm
  - Called for replacing SiO_2 with high k dielectrics; EOT as thin as 1.0 nm or less
  - Coulomb scattering and phonon issue related to high k gate dielectrics leading to degraded channel mobility
  - higher mobility materials such as **Ge**, and **III-V's**
- Ge MOSFET
  - Ge offers **two times higher mobility for electrons** and **four times higher for holes** comparing with Si
  - lack of stable native oxide hindering Ge passivation, making fabrication of Ge MOSFET difficult
- III-V MOSFET (III-V's: GaAs, InSb, InAs, GaN,….)
  - **electron mobility in III-V's much higher than those in Si and Ge**
  - A mature III-V MOS technology with electron mobilities at least 10 times higher than that in Si and with dielectrics having k several times higher that of SiO_2 would certainly enable the electronic industry to continue pushing its new frontiers for a few more decades
  - **bandgap engineering and direct bandgaps in the III-V's**, not available in Si- and Ge-based systems, providing novel designs and making highly-performed **integrated optoelectronic circuits of combining MOS and photonic devices a reality**

Oxygen Bonding from EELS (Chemistry on an Atomic Scale)

Nominal 1.1 nm SiO_2: 0.8 - 1 nm Bulk SiO_2

1.6 nm wide oxygen profile



CMOS scaling, When do we stop ?

Reliability: 25 22 18 16 Å

processing and yield issue

Tunneling : 15 Å

Design Issue: chosen for 1A/cm^2 leakage
I_{on}/I_{off} >> 1 at 12 Å

Bonding:

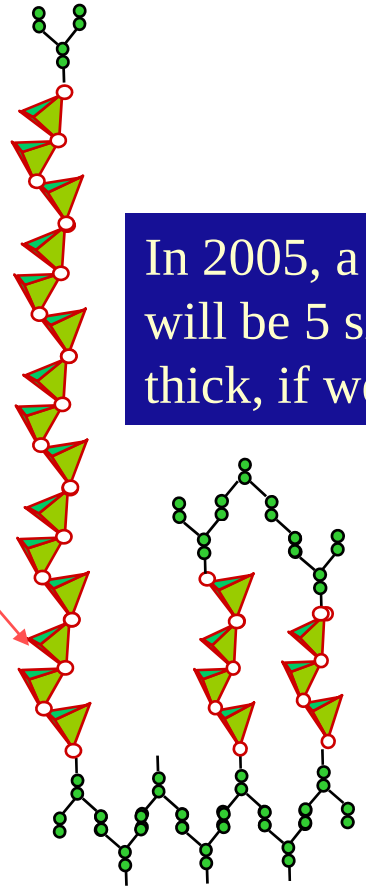
Fundamental Issues---

- How many atoms do we need to get bulk-like properties?

EELS -- Minimal 4 atomic layers !!

- Is the interface electronically abrupt?
- Can we control roughness?

In 1997, a gate oxide was 25 silicon atoms thick.

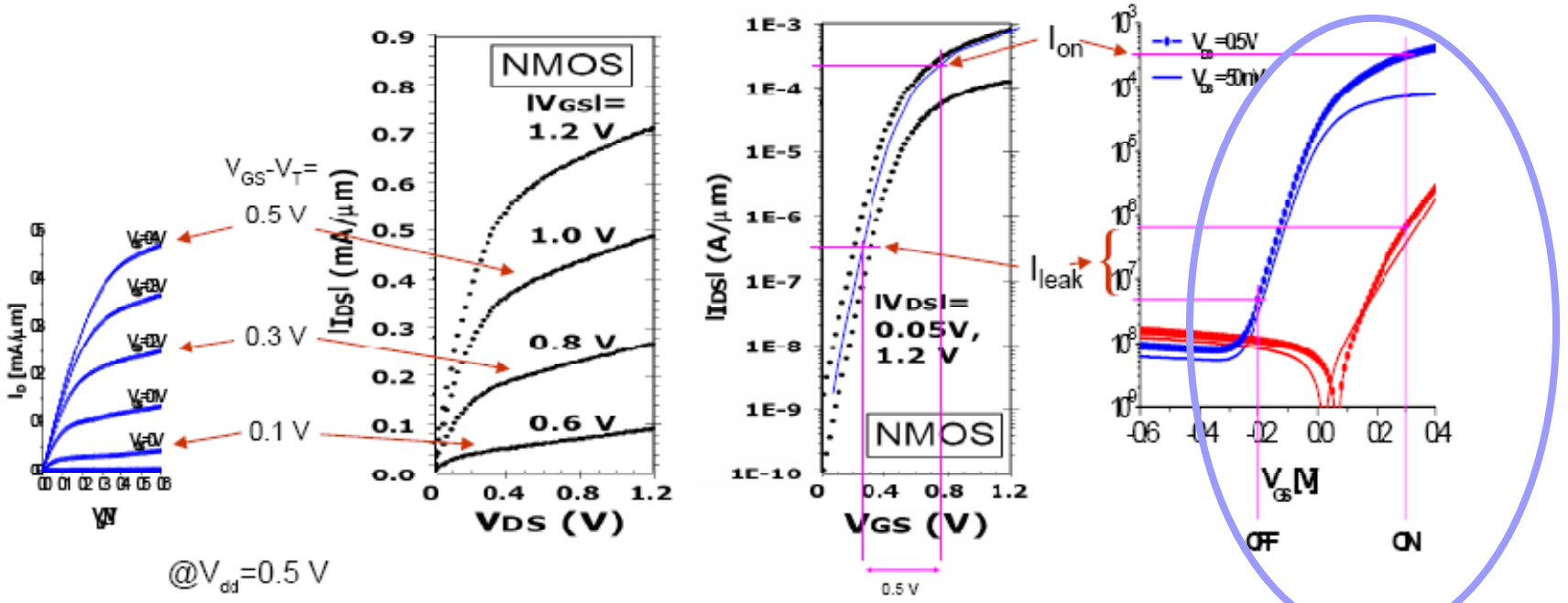


In 2005, a gate oxide will be 5 silicon atoms thick, if we still use SiO_2

and at least 2 of those 5 atoms will be at the interfaces.

Comparison with 65 nm CMOS

Intel's 65 nm low-power CMOS (IEDM '05)



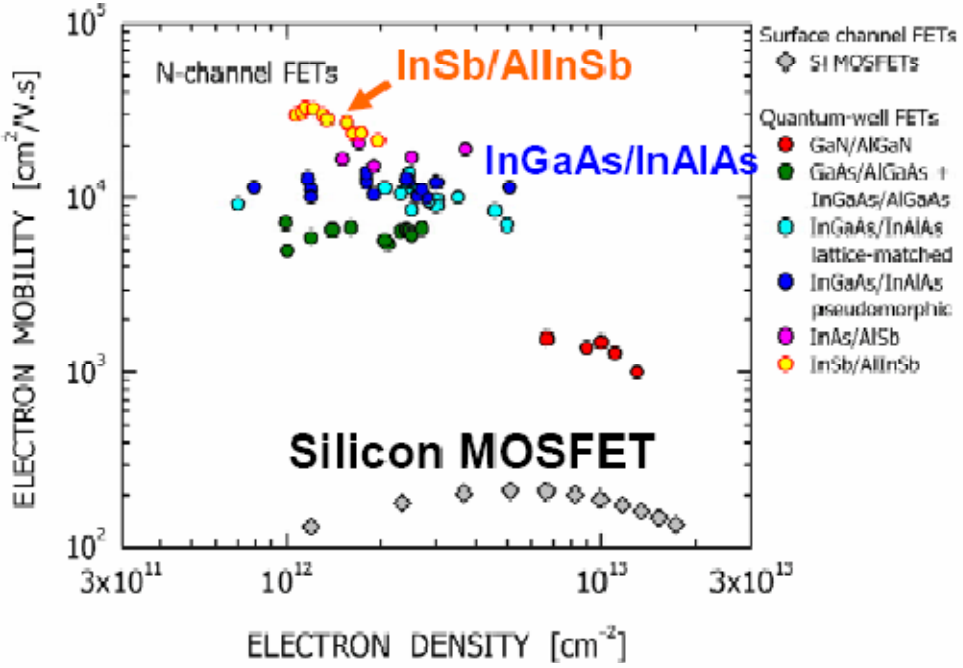
	L_g (nm)	I_{on} (mA/mm)	I_{leak} (nA/mm)	S (mV/dec)	DIBL (mV/V)
InGaAs HEMT	60	320	330	70	44
65 nm CMOS (low power)	55	220	330	90	80

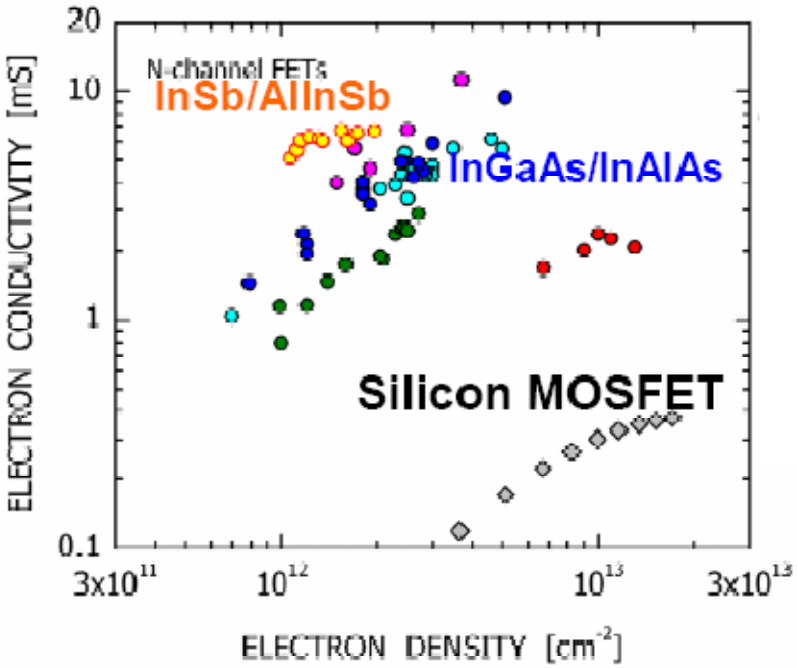
For the same I_{leak}, 60 nm InGaAs HEMT yields 45% more I_{ON} than 65 nm CMOS

J. A. del Alamo, D.-H. Kim, and N. Waldron, **Intel III-V CMOS Conference, Sept. 9, 2006**

A III-V MOS will make I_{on}/I_{off} ratio to $>10^7$, acceptable in the IC industry

Why III-V Research for Future Logic Applications?

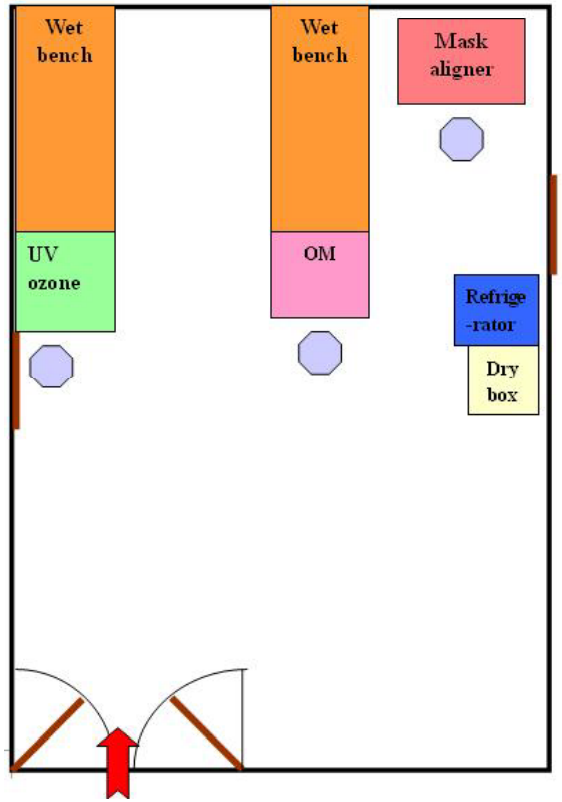


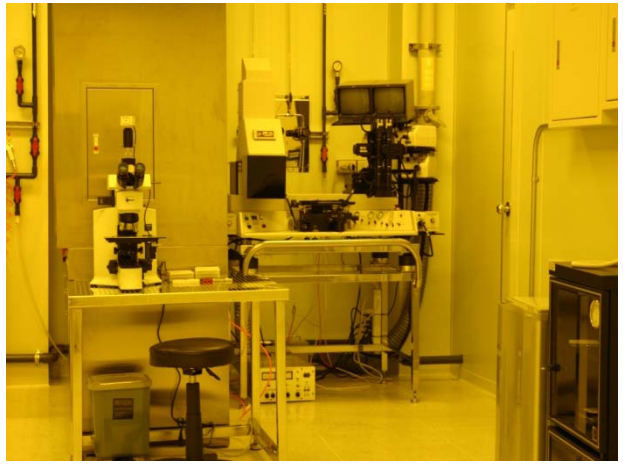


- III-V has been used in commercial communication & optoelectronics products for a long time
- III-V quantum-wells show ~100X higher electron mobility and ~20X higher electron conductivity than Si ➔ [potentially high-speed + low-power]
- Top-down patterning as opposed to bottom-up chemical synthesis
- III-V will NOT replace Si; it will need to be integrated onto Si

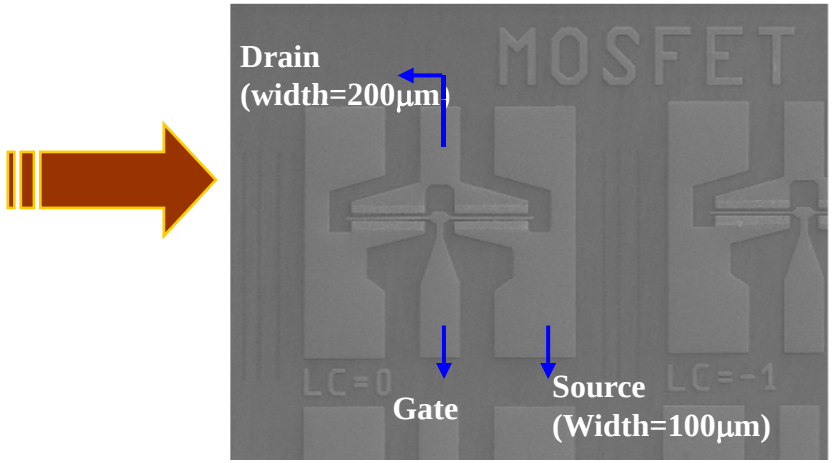
R. Chau
Intel Senior Fellow
2006 DRC

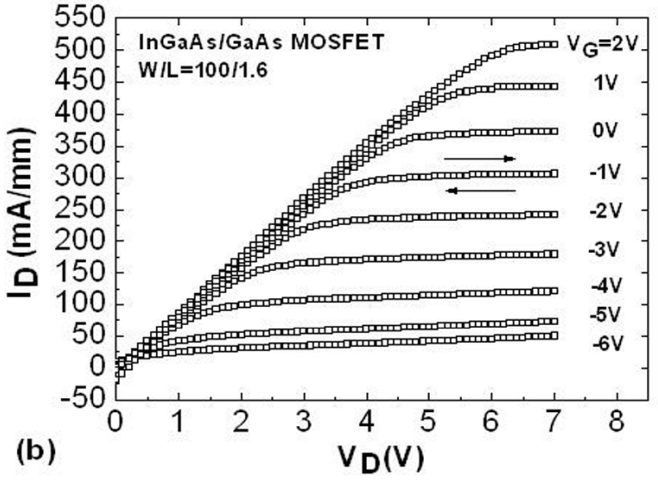
III-V Nano Electronics Processing Lab





- **ABM mask aligner →** sub-micro gate length capability
- **UV-ozone →** surface cleaning
- **Olympus OM→** image catch and sub-micro measurement capability
- **ULVAC ICP-RIE →** dry etch of metal gates (***move in soon)***





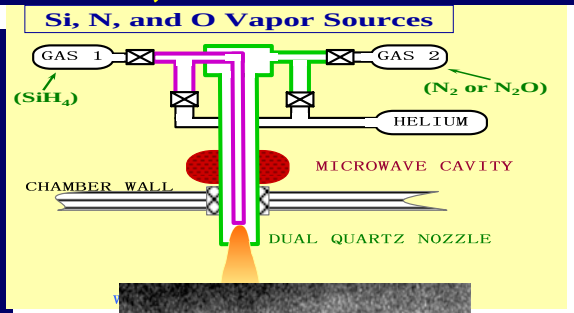
$Ga_2O_3(Gd_2O_3)$ and JVD (MAD) Si_3N_4 on InGaAs

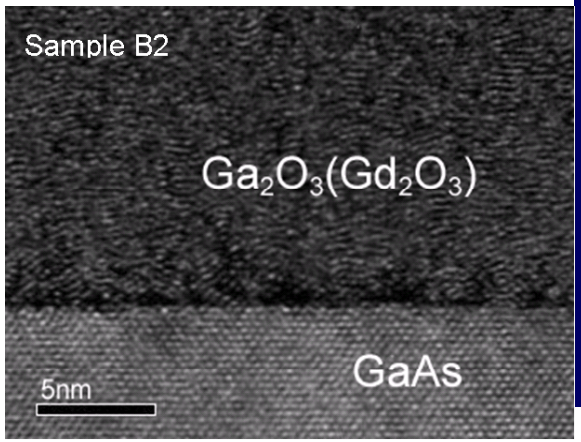
Intel J. F. Zheng, W. Tsai, Natl Tsinghua- M. Hong, J. Kwo, Yale – T.P. Ma

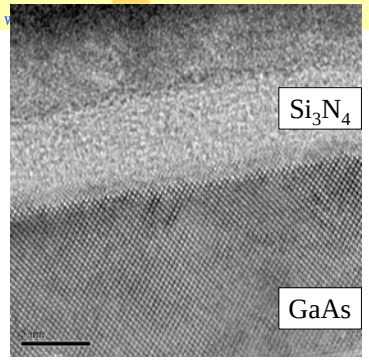
GGG Stable up to 800C for process integration

A new dual dielectric approach:

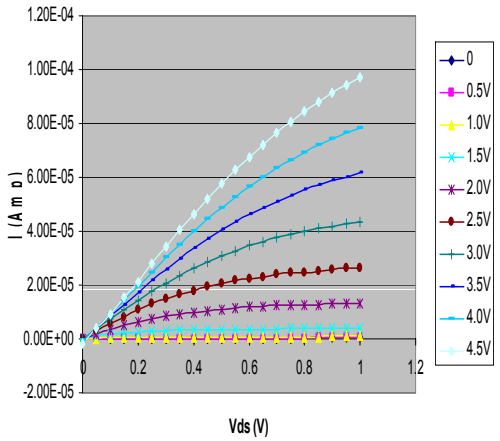
1. **GGG dielectric is part of the MBE channel grown – unpin Fermi level**
2. **A second dielectric can be high-k to reduce EOT toward few nm**
3. **Principle of proof dual dielectric approach with 5nm EOT GGG and trap less JVD (MAD) Si_3N_4 (after high temperature PDA)**

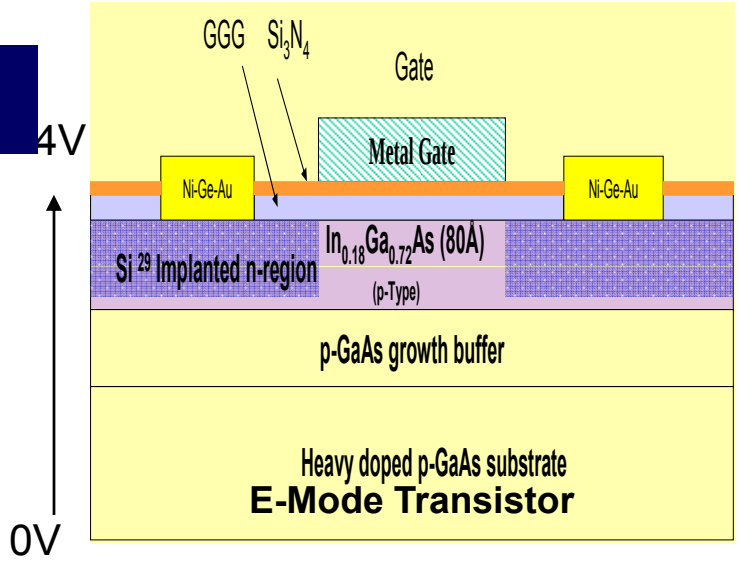




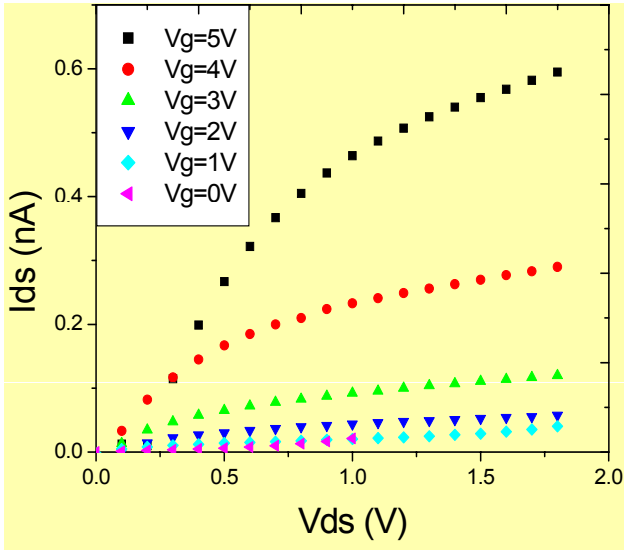


Enhancement Mode with inversion using GGG

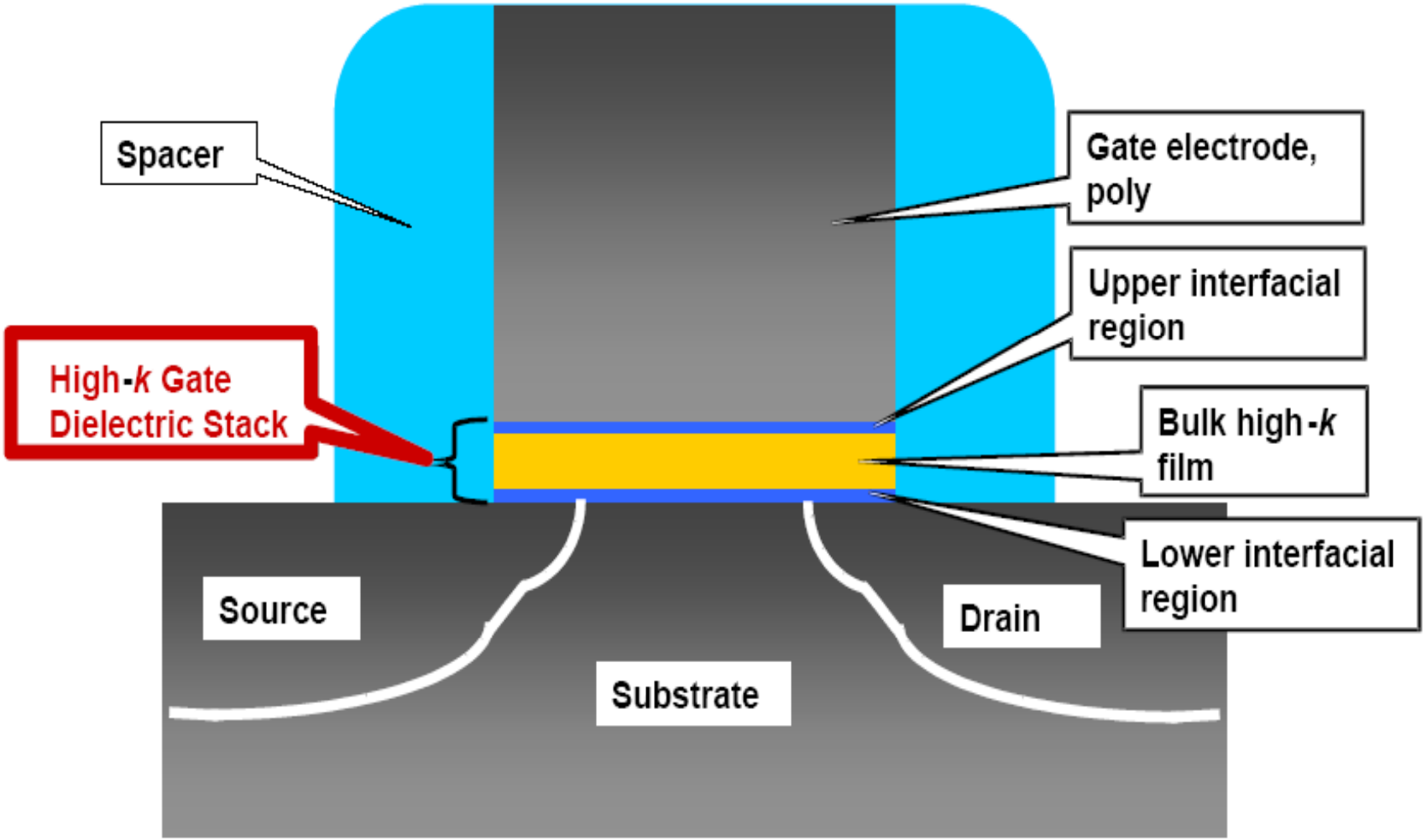




Enhancement Mode with inversion using Si_3N_4



High κ Gate Dielectric MOSFET



NOVEL GATE DIELECTRICS FOR III-V SEMICONDUCTORS

How to passivate GaAs surface? **Previous efforts over thirty five years !**

❖ **Previous Efforts**

- Anodic, thermal, and plasma oxidation of GaAs
- Wet or dry GaAs surface cleaning followed by deposition of various dielectrics

Growth using single chamber

- AlGaAs doped with O or Cr, Cho and Cassey 1978
- Native oxides or Al2O3 on GaAs during the same growth, i.e. introduction of oxygen in III-V MBE chamber, Ploog et al 1979
- ZnSe (lattice constant of 5.67Å and a E_g 2.7 eV) on GaAs, Yao et al, 1979
- Si on InGaAs or GaAs, IBM at Zurich 1990 (?) and Morkoc et al, 1996

❖ **Our Breakthrough** Growth using multiple chambers

- Novel gate oxides $Ga_2O_3(Gd_2O_3)$ and Gd_2O_3 in-situ deposited by e-beam evaporation with low D_{it}
- Have applied to GaAs, InGaAs, AlGaAs, InP, GaN, and Si

THE KEY is to clean GaAs surface and to identify a dielectric being thermodynamically and electronically stable, and showing low D_{it} with GaAs.

NOVEL DIELECTRICS FOR III-V SEMICONDUCTORS

Effective Passivation of GaAs

- **GaAs MOSFET**
  - **Advantages**
    - inherent higher electron mobility and semi-insulating GaAs substrates, comparing with Si-based MOSFET
      - Rich band gap engineering in compound semiconductors
    - low power consumption and circuit simplicity of CMOS, comparing with GaAs MESFET, HEMT
  - **Applications**
    - new generation of digital GaAs IC's of high speed and low power for communication and computer industries
- Other electronic applications
  - High power devices in MESFET, HEMT, and high speed devices in HBT
- Laser facet coatings and other photonic applications

ULTRAHIGH VACUUM DEPOSITION OF OXIDES

Initial thinking: to attain Ga_2O_3 film for passivation

High-purity single crystal $Ga_5Gd_3O_{12}$ (GGG) source

Evaporation (sublime) by e-beam

Gd_2O_3 ionic oxide
T_m > 4000K

Ga_2O_3 more covalent oxide
T_m ~ 2000K

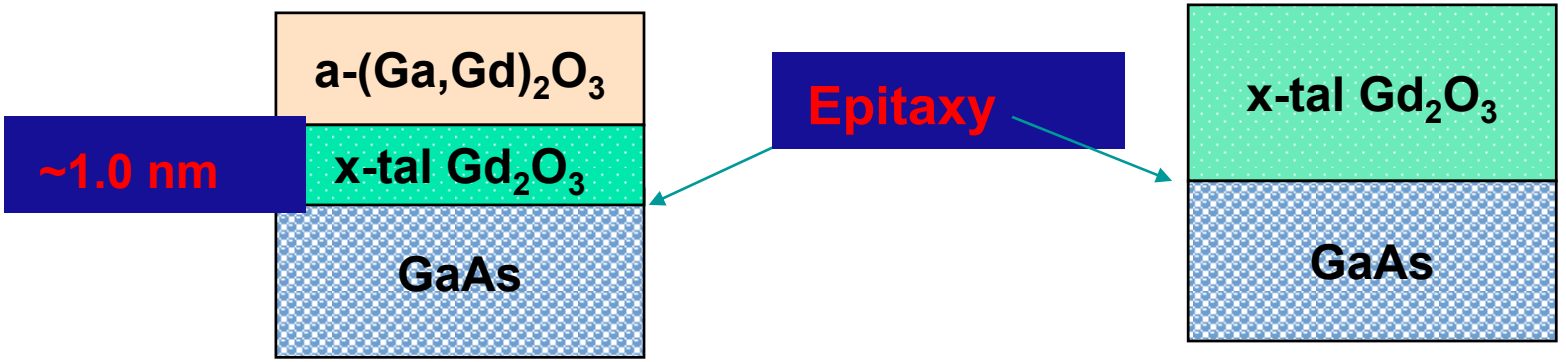
Ga_2O_3 evaporated mostly, and formed amorphous Ga_2O_3 film

Mixed Oxide $(Ga,Gd)_2O_x$

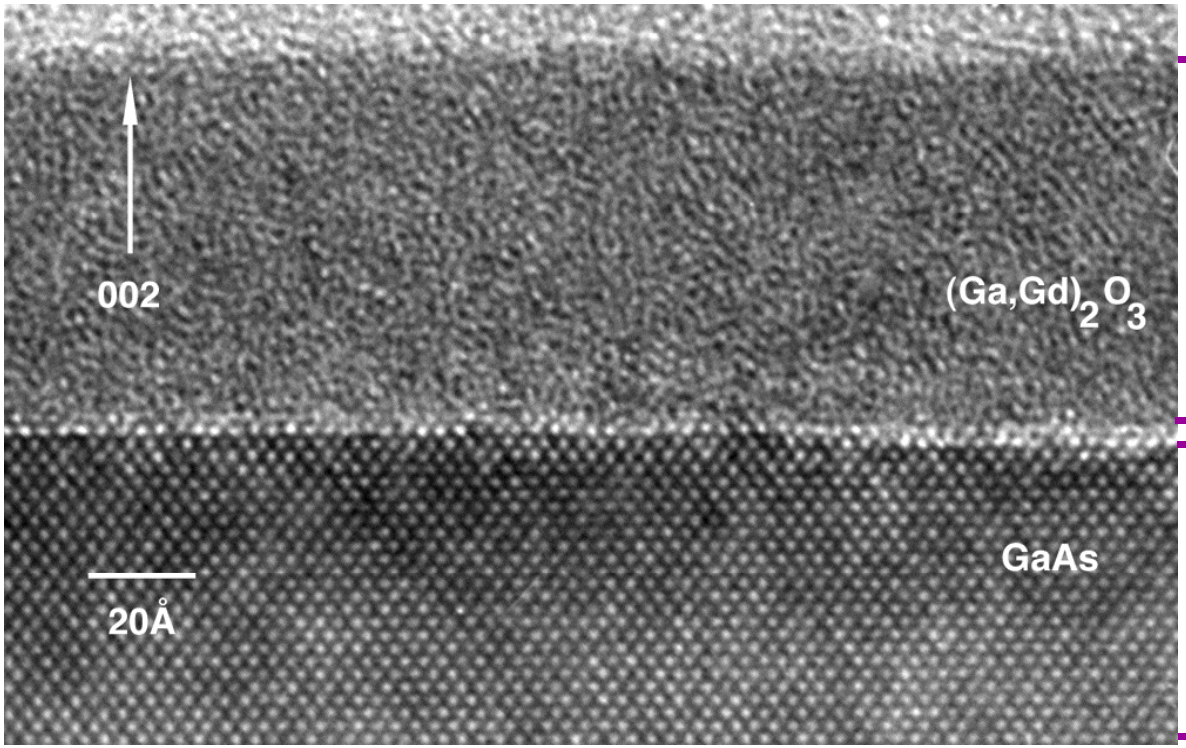
Gd/(Ga+Gd) > 20%
Gd^{+3} stabilize Ga^{+3}

Pure Gd_2O_3 Film

Single domain, epitaxial film in (110) Mn_2O_3 structure



High Resolution TEM of $Ga_2O_3(Gd_2O_3)$ on GaAs



Amorphous region

Some crystalline phase at interface

Single crystal GaAs

Single crystal Gd_2O_3 on GaAs - Epitaxial interfacial structure

Not a Mn_2O_3 structure at interface
Stacking sequence similar to that of GaAs

- Nature – Materials 2002 Oct issue cover paper
- "New Phase Formation of Gd_2O_3 films on GaAs (100)", J. Vac. Sci. Technol. B 19(4), p. 1434, 2001.
- " Direct atomic structure determination of epitaxially grown films: Gd_2O_3 on GaAs(100) " PRB 66, 205311, 2002 (12 pages)
- A new X-ray method for the direct determination of epitaxial structures, coherent Bragg rod analysis (COBRA)