AOARD

Nano-electronics of high κ dielectrics on high mobility channel semiconductors for key technologies beyond Si CMOS

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J. Kwo and **M. Hong**

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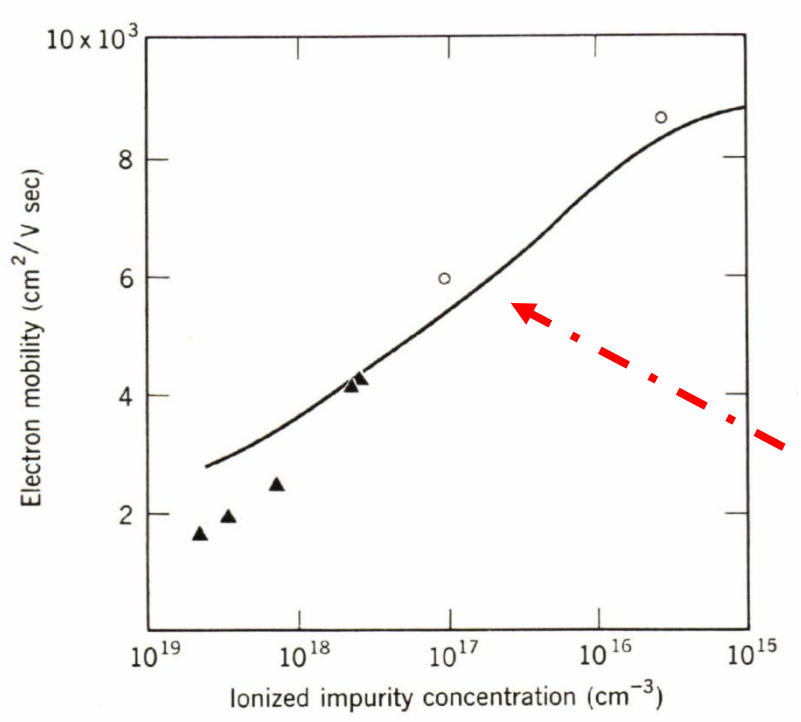
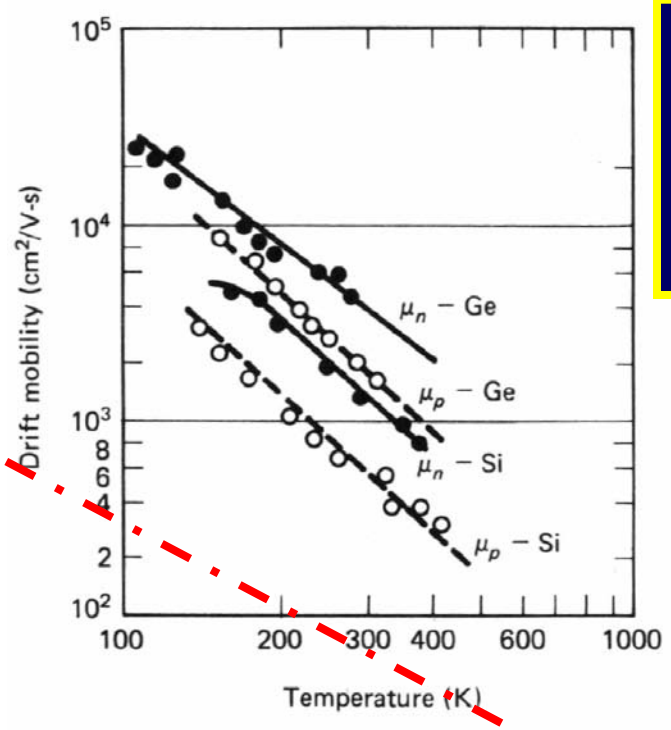
Electron mobilities in GaAs, Si, and Ge

GaAs



Si and Ge



Measured drift mobility in Si and Ge (F. J. Morin and J. P. Maita, Phys. Rev., 94, 1526, **(1954)** and 96, 28 (1954))

Solid curve: theory with combined polar and ionized-impurity scattering (Ehrenreich: JAP 32, 2155, 1961)
Experimental points o: Reid and Willardson: J. Electronics and Control, 5, 54 **(1958)** ▲: Weisberg, Rosi, and Herkart: Metallurgical Soc. Conf., v.5 "Properties of elemental and compound semiconductors, Interscience Publishers, New York, p.275

DRIFT MOBILITIES (cm^2/ V-s) in Ge, Si, and GaAs at 300K

	Ge		Si		GaAs	
	μ_n	μ_p	μ_n	μ_p	μ_n	μ_p
value at 300K	**3900**	1900	**1400**	470	**8500**	340
Temperature dependence	$T^{-1.66}$	$T^{-2.33}$	$T^{-2.5}$	$T^{-2.7}$	—	$T^{-2.3}$

Background leading to unpin surface Fermi level in III-V compound semiconductors

- Late 1980s to early 1990s, problems in then AT&T's pump lasers (980 nm) for undersea optical fiber cable (trans-Atlantic)
- Semiconductor facet (HR, AR) coating
  - Reducing defects between InGaAs (GaAs) and coating dielectrics
- Passivation of the facets
- Electronic passivation much more stringent than optical passivation
  - (110) vs (100) of InGaAs (GaAs)

Pioneering work of GaAs and InGaAs MOSFET's using $Ga_2O_3(Gd_2O_3)$ at Bell Labs w/o 2 overlayers

- 1994
  - novel oxide $Ga_2O_3(Gd_2O_3)$ to effectively passivate GaAs surfaces
- 1995
  - establishment of accumulation and inversion in p- and n-channels in $Ga_2O_3(Gd_2O_3)$-GaAs MOS diodes with a low D_{it} of 2-3 x 10^{10} cm^{-2} eV^{-1}(IEDM)
- 1996
  - first e-mode GaAs MOSFETs in p- and n-channels with inversion (IEDM)
  - Thermodynamically stable
- 1997
  - e-mode inversion-channel n-InGaAs/InP MOSFET with g_m= 190 mS/mm, Id = 350 mA/mm, and mobility of 470 cm^2/Vs (DRC, EDL)
- 1998
  - d-mode GaAs MOSFETs with negligible drain current drift and hysteresis (IEDM)
  - e-mode GaAs MOSFETs with improved drain current (over 100 times)
  - Dense, uniform microstructures; smooth, atomically sharp interface; low leakage currents
- 1999
  - GaAs power MOSFET
  - Single-crystal, single-domain Gd_2O_3 epitaxially grown on GaAs
- 2000
  - demonstration of GaAs CMOS inverter

1897 J. J. Thomson discovery of electron

1947 The Transistor

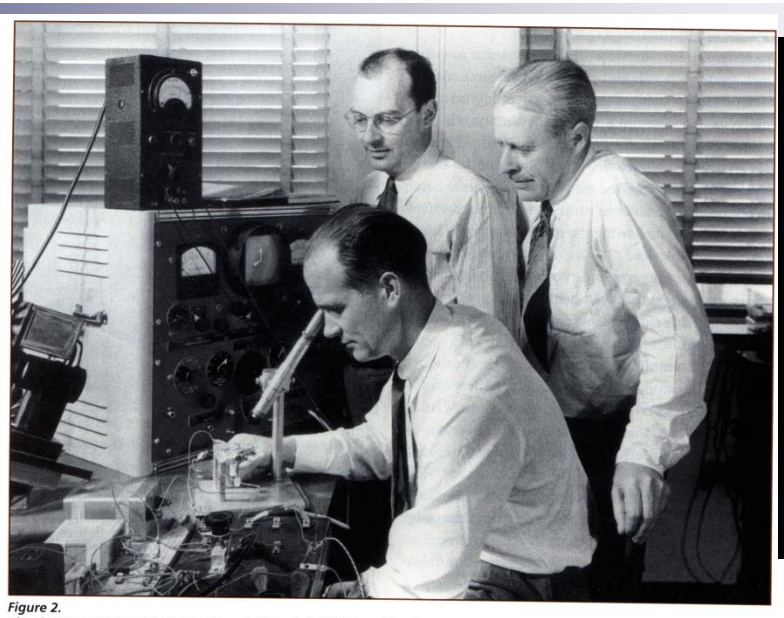
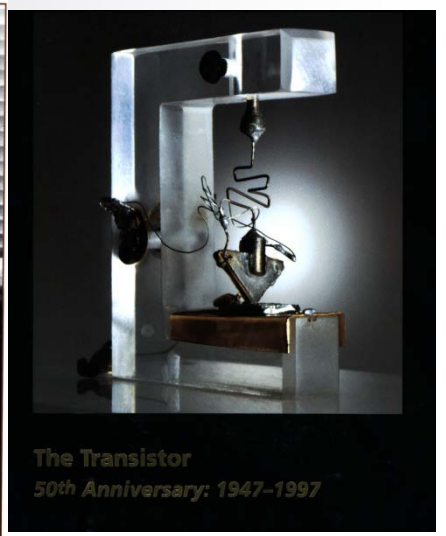


Figure 2.
The three inventors of the transistor: (left to right) William Shockley, John Bardeen, and Walter Brattain, who were awarded the 1956 Nobel Prize in physics.



2007 High k + metal gate on Si for 45 nm node CMOS

What next – III-V InGaAs, GaN, Ge MOS ?

- Mervin Kelly, the then Director of Res. at Bell Labs, had predicted the problem and had already taken action to find a solution.
  - Although relays and vacuum tubes were apparently making all things possible in telephony, he had predicted for some years that the low speed of relays and the short life and high power consumption of tubes would eventually limit further progress in telephony and other electronic endeavors.
  - In the summer of 1945, Kelly had established a research group at Bell Labs to focus on the understanding of semiconductors. The group also had a long-term goal of creating a solid-state device that might eventually replace the tube and the relay.

For Chip Makers, Hybrids May Be a Way Forward – NYTimes (Dec. 2009)

By John Markoff

Searching for new ways to make computers that run faster and use less power, the chip industry is once again eyeing some **exotic** materials that can offer great speed, but have been more costly and difficult to manufacture than silicon.

The materials, so-called **III-V** semiconductors, include compounds like **gallium arsenide and indium phosphide.** The have found their way into military and communications uses, but have largely been relegated to niches by more standard silicon-based manufacturing processes.

The legendary supercomputer designer Seymour Cray used gallium arsenide in his Cray 3 and Cray 4 designs. In general, though, the materials have not had the low-power characteristics that have mad
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working chips at the next step down, 32 nanometers. Intel can now place about one billion transistors in its most advanced microprocessors, and the next step toward smaller scale, which will double the number of transistors available to circuit designers, will probably take place toward the end of 2009.

- ✓**exotic** materials compounds like **gallium arsenide and indium phosphide**
- ✓**a new kind of hybrid chip, integrating radio or optical communications III-V-based transistors at lower power without losing all of their speed advantages**
- ✓**MOSFET**, Not MESFET, HEMT
- ✓**four chip generations**

It might be **four chip generations**, however, before Intel adds the new hybrid approach to its commercial chips, said Mike Mayberry, the company's director of components research.

The new technology could have widespread applications in consumer electronics products.

During a news conference on Monday, industry executives expressed optimism about the new technique, which they said was still years away from commercialization.

Outline

Motivation

- Why InGaAs, Ge? Why MOSFET?

Experimental

- Novel
- Chara
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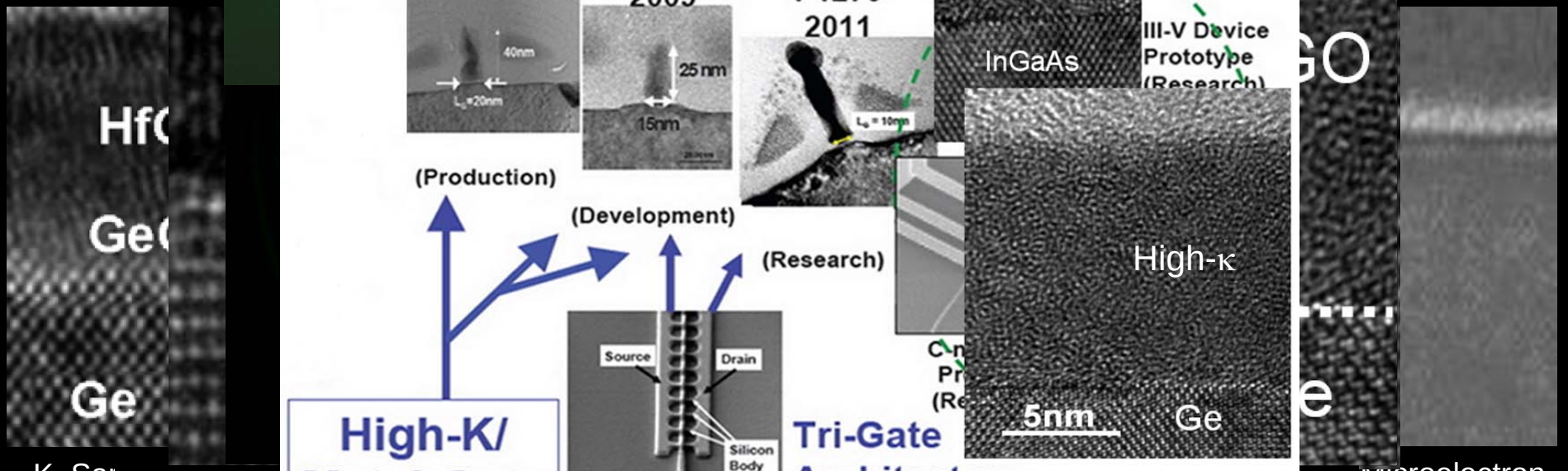
AR-XPS)



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Microelectron.
5). (IMEC)

Do we need a new methodology for GaAs passivation?

A. M. Green and W. E. Spicer
Stanford University
JVST A11(4), 1061, 1993

Sulfur passivation –Sandroff et al, Bell Labs APL51, 33, 1987
Sb passivation – Cao et al, Stanford Surf. Sci. 206, 413, 1988

"A new methodology for passivating compound semiconductors is presented in which two overlayers are used. In this approach, the first layer defines the surface electronically and the second provides long term protection."

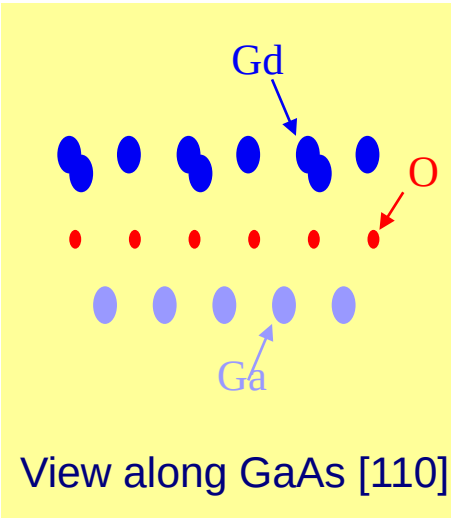
Is it possible to have a III-V (GaAs) MOS, similar to SiO_2/Si, in which a low D_{it}, a low J, thermodynamic stability at high temp. (>800℃), single layer of gate dielectric, no S and Sb, etc are achievable?

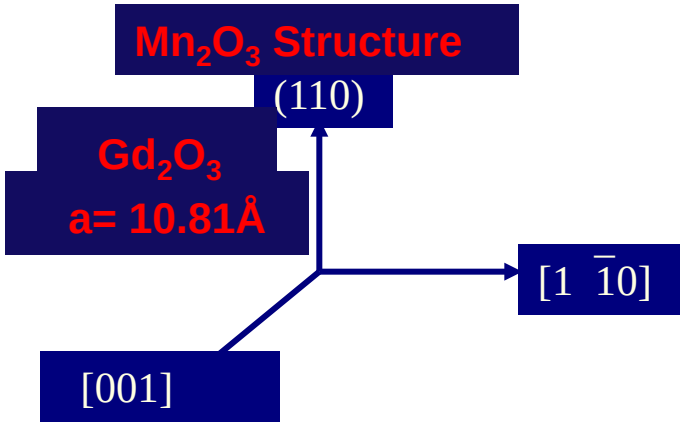
YES!!!

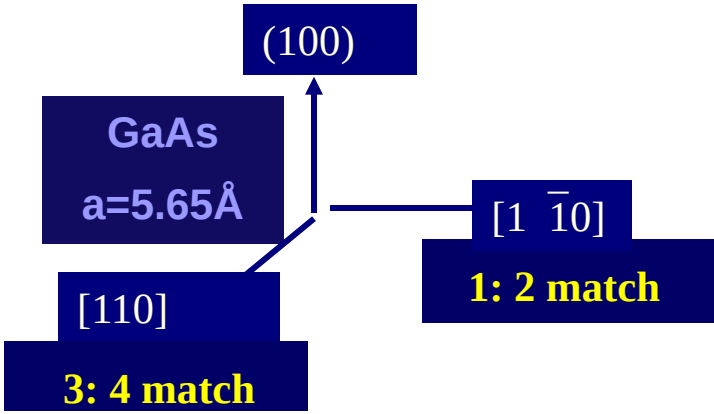
Is it necessary to have GeON as an interfacial layer in Ge MOS?

No!!!

Pioneer Work : Single Crystal Gd_2O_3 Films on GaAs

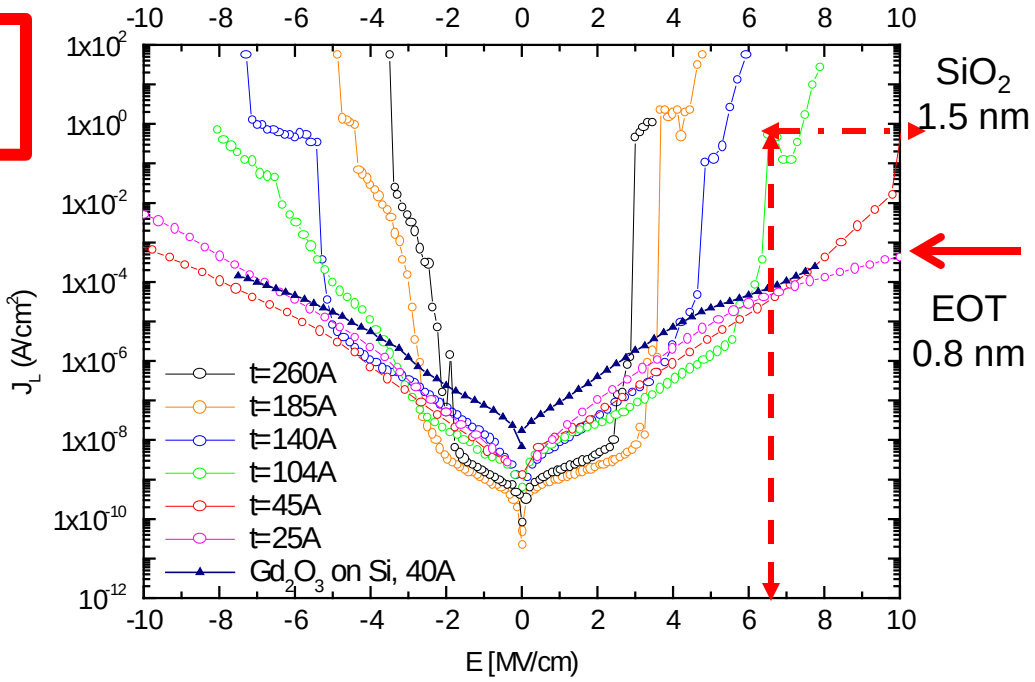




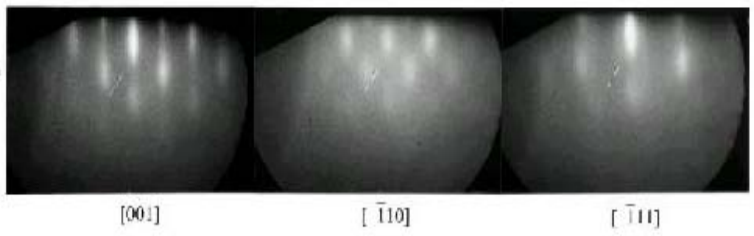


Low D_{it}'s and low J_L

M. Hong, J. Kwo et al, Science 283, p.1897, 1999



Gd_2O_3 (110) 25Å



ULTRAHIGH VACUUM DEPOSITION OF OXIDES

Initial thinking: to attain Ga_2O_3 film for passivation

High-purity single crystal $Ga_5Gd_3O_{12}$ (GGG) source

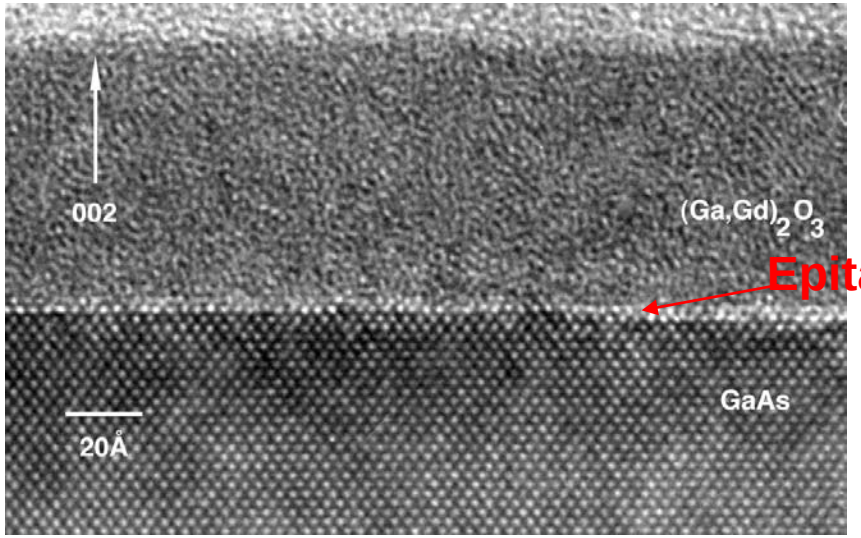
Evaporation (sublime) by e-beam

Gd_2O_3 ionic oxide
T_m > 4000K

Ga_2O_3 more covalent oxide
T_m ~ 2000K

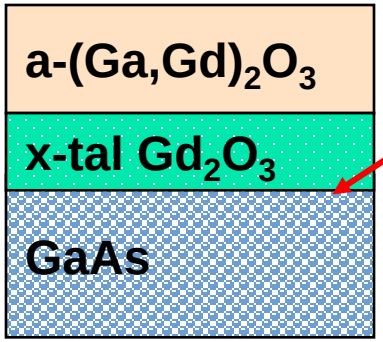
Ga_2O_3 evaporated mostly, and formed amorphous Ga_2O_3 film

$(Ga,Gd)_2O_3$



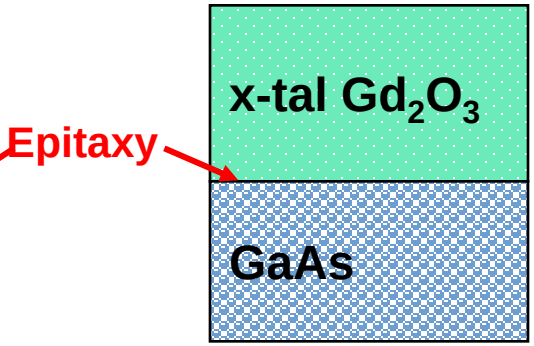
Mixed Oxide $(Ga,Gd)_2O_3$

Gd/(Ga+Gd) > 20%
Gd^{+3} stabilize Ga^{+3}

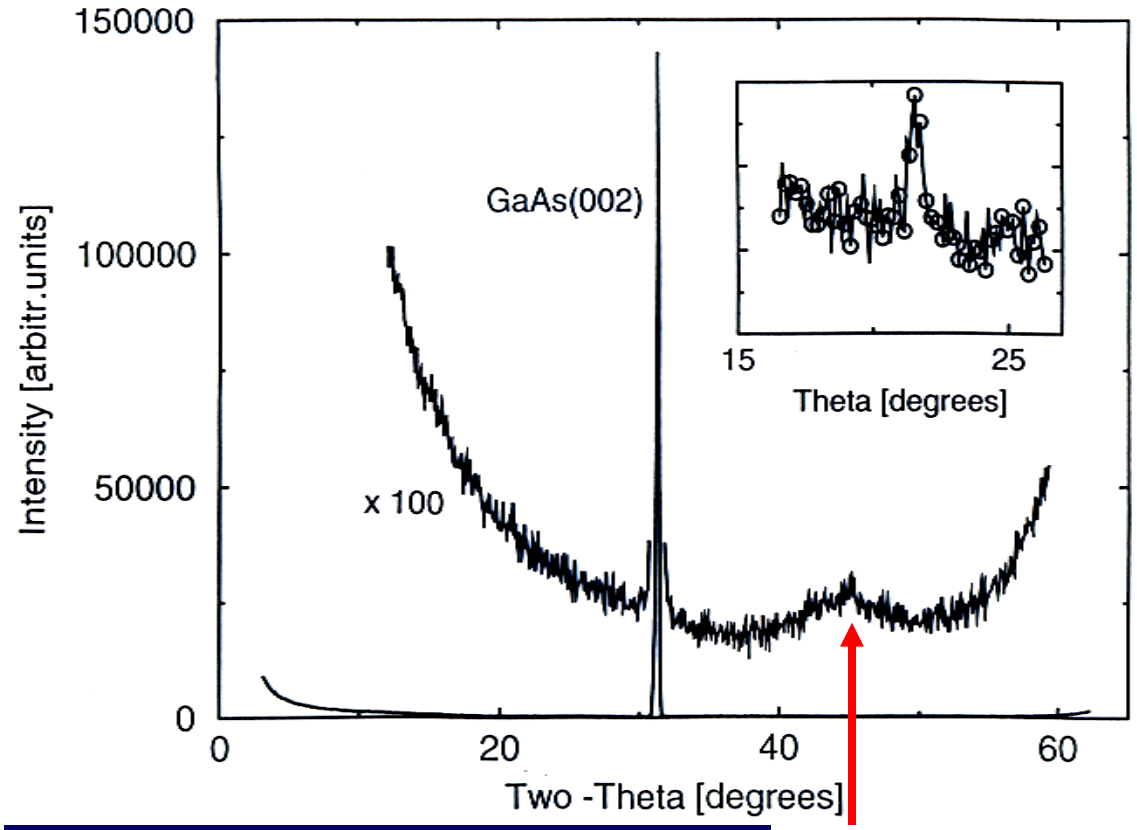


Pure Gd_2O_3 Film

Single domain, epitaxial film in (110) Mn_2O_3 structure

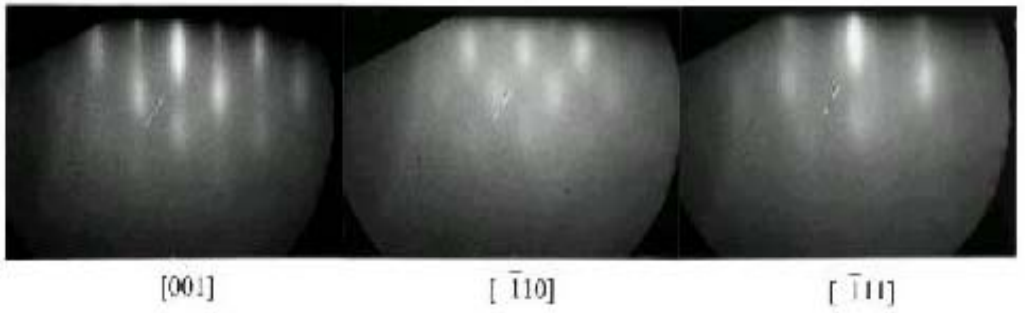


Initial growth of $Ga_2O_3(Gd_2O_3)$ 1.1 nm thick



X-ray diffraction of normal scan and rocking curve

In-situ RHEED pattern showing a single crystal growth

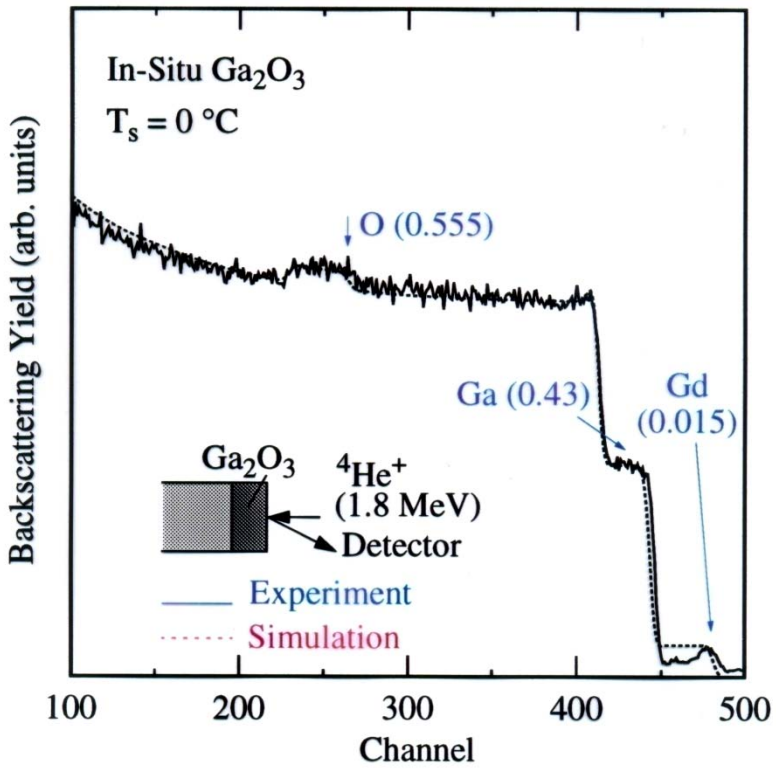


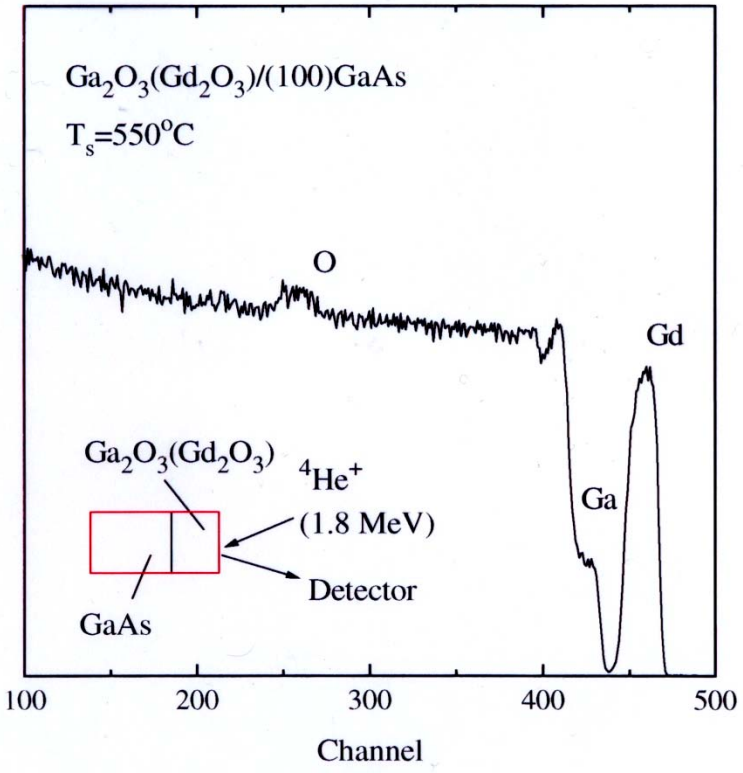
- MBE – compound semiconductor growth – A. Y. Cho (National Medal of Science 1993 and National Medal of Technology 2007)

- MBE – metal and oxide growth – J. Kwo (first in discovering anti-ferromagnetic coupling through non-magnetic layer in magnetic superlattices PRL's 1985 – 1986)

Frank Shu, UC University Professor and former President of Tsing Hua Univ.

Growth of $Ga_2O_3(Gd_2O_3)$ films using e-beam evaporation from $Ga_5Gd_3O_{12}$ target – RBS studies

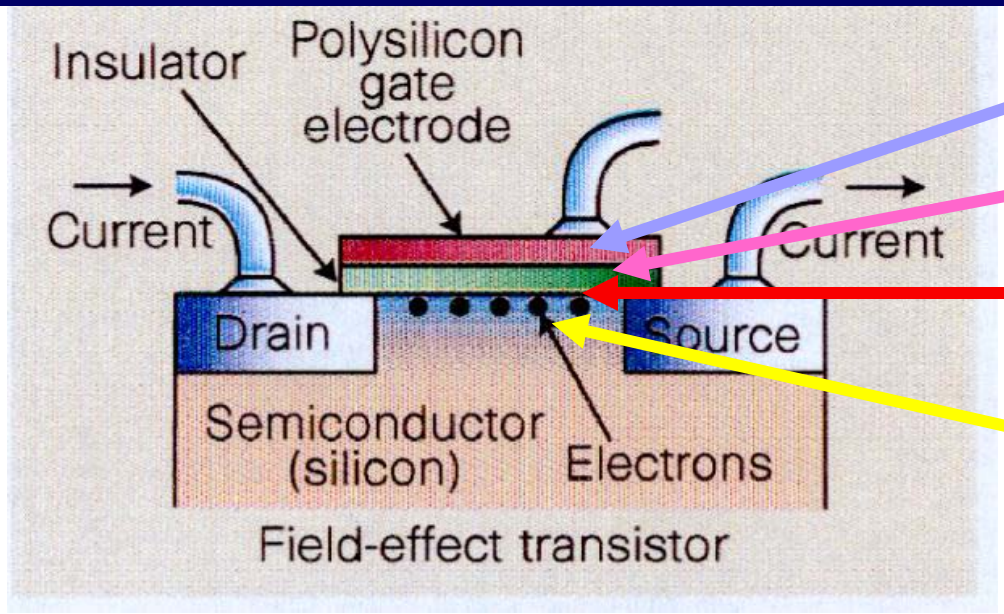




Identified the essential role of Gd_2O_3
The Gd/(Ga+Gd) ratio needs to be greater than 20%
The electropositive Gd^{+3} may stabilize Ga^{+3} in the film

Device Scaling – Beyond 22-16 nm node: high κ, metal gates, and high mobility channel

1960 Kahng and Atalla, Bell Labs First MOSFET



Metal gate

High κ gate dielectric

Oxide/semiconductor interface

High mobility channel

Integration of IIIV, Ge, GaN with Si

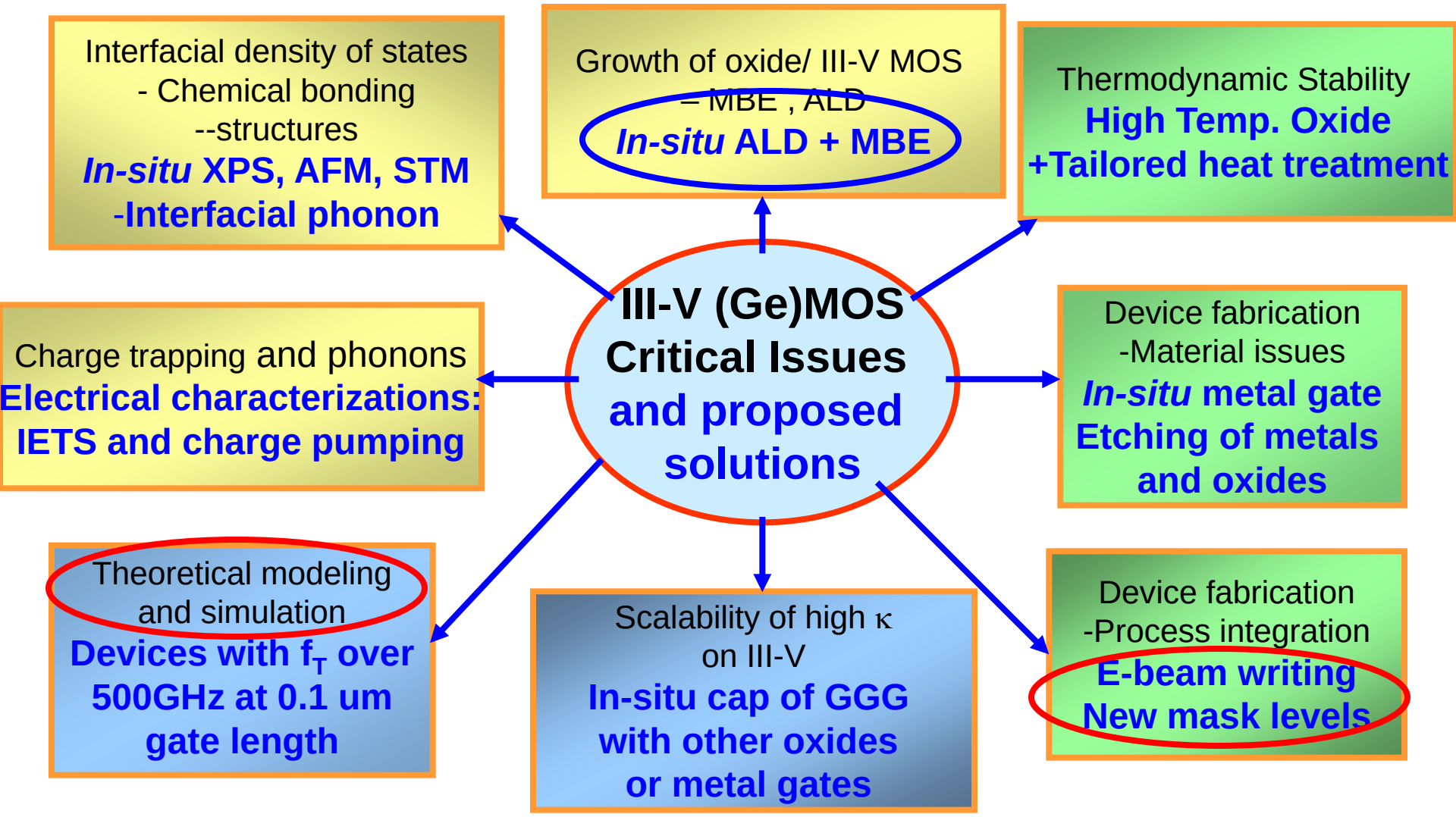
Moore's Law:
The number of transistors per square inch doubles every 18 months

Shorter gate length L
Thinner gate dielectrics t_{ox}

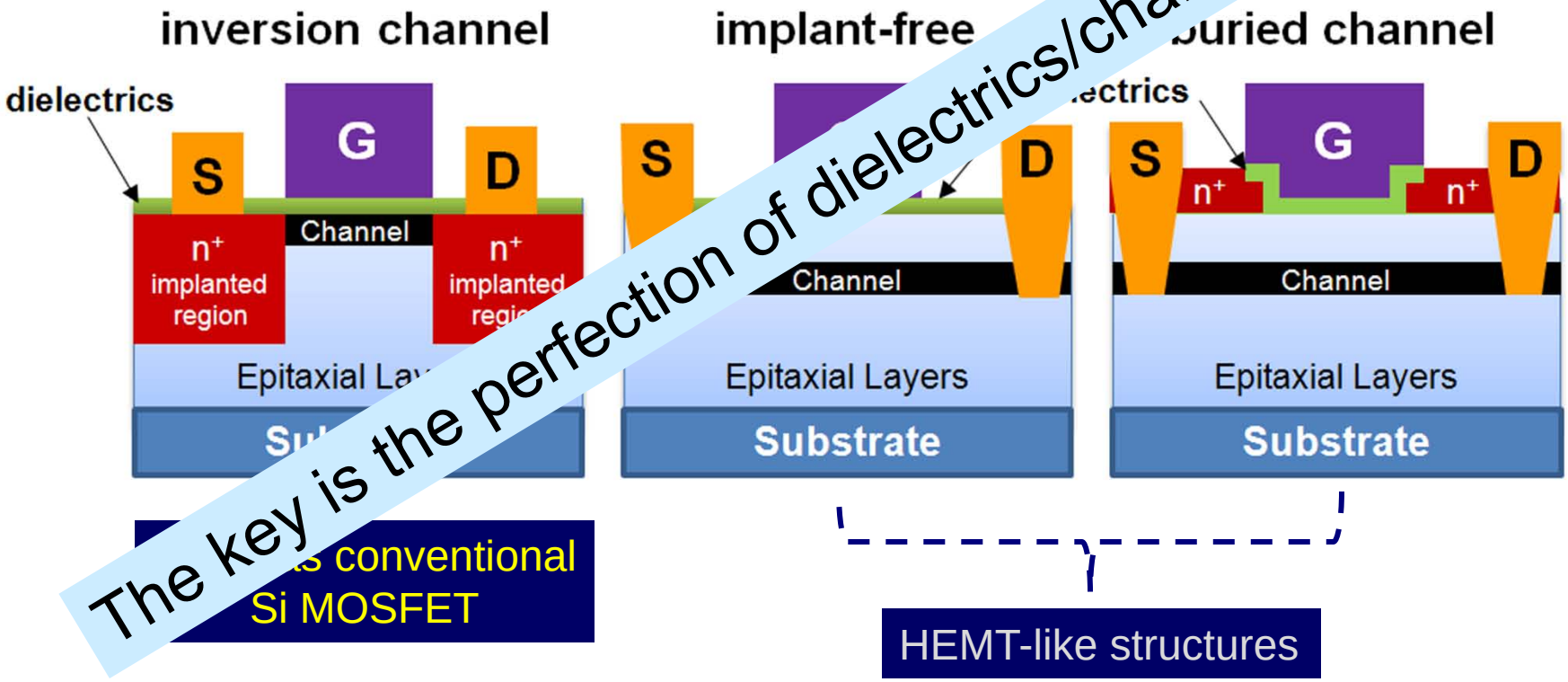
Driving force :
High speed
Lower power consumption
High package density

	Si	GaAs	$In_{0.53}Ga_{0.47}As$	GaN	InAs	InSb	units
Energy gap	1.12	1.43	0.75	3.40	0.354	0.17	eV
Lattice constant	5.431	5.65	5.87	3.19	6.06	6.50	Å
Electron effective mass	0.19	0.063	0.041	0.20	0.023	0.014	-
Electron mobility	1500	8500	14000	1300	25000	78000	$cm^2 V^{-1} s^{-1}$
Electron saturation velocity	1×10^7	2×10^7	8×10^6	3×10^7	3×10^7	5×10^7	$cm\ s^{-1}$
Electron mean free path	0.07	0.15	0.19	0.2	0.27	0.58	μm

Proposed Solutions to Challenges of III-V (Ge) MOSFET

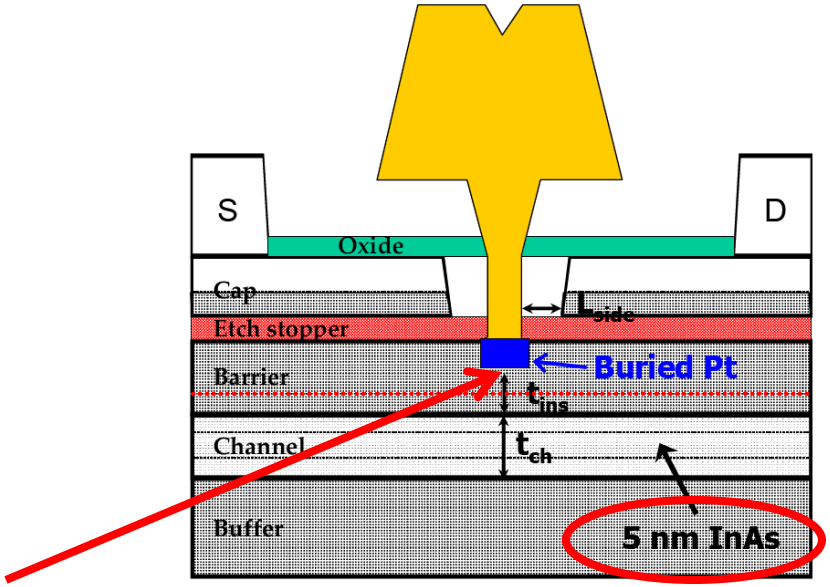


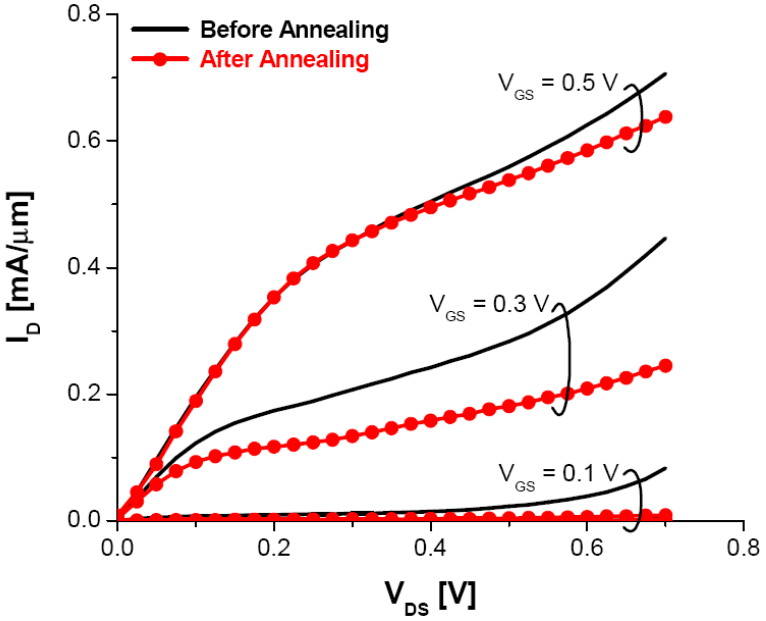
Enhancement-mode devices

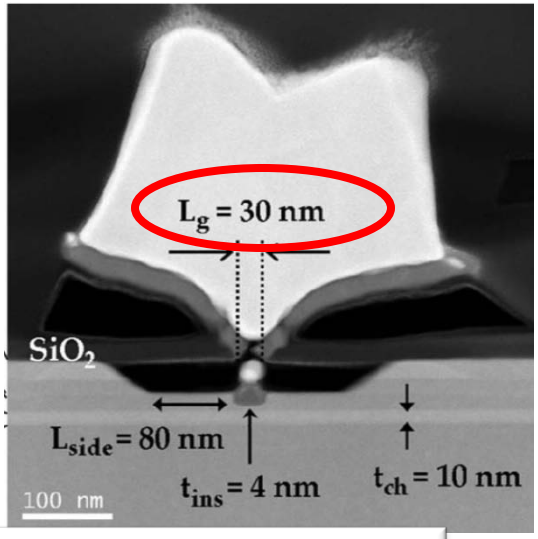


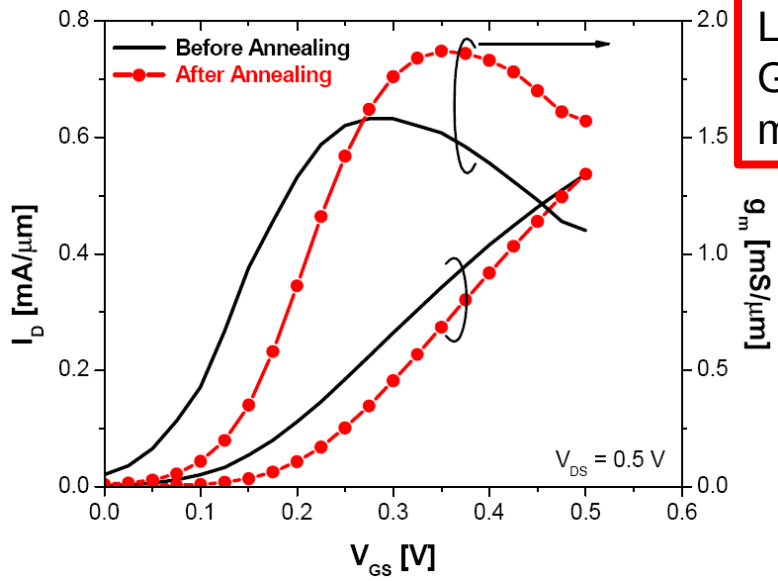
The key is the perfection of dielectrics/channel interface

Buried Channel Transistor - HEMT





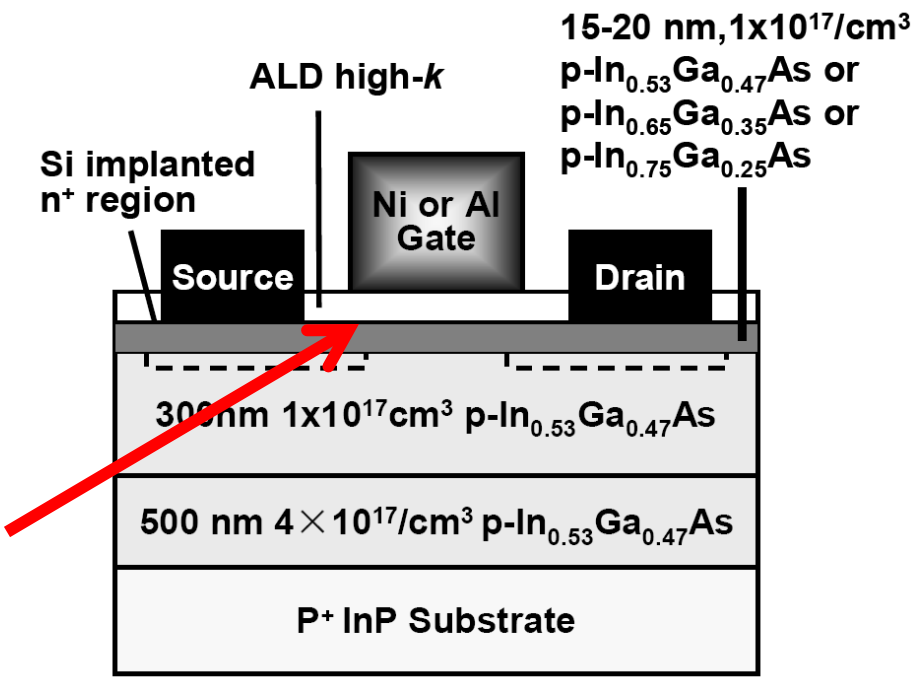




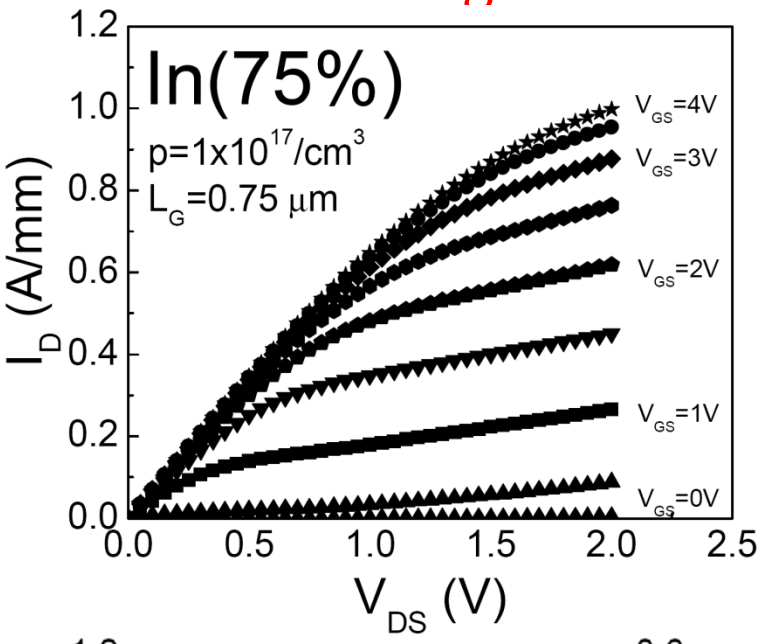
L_g = 30 nm
G_m = 1.8-1.9 mS/μm

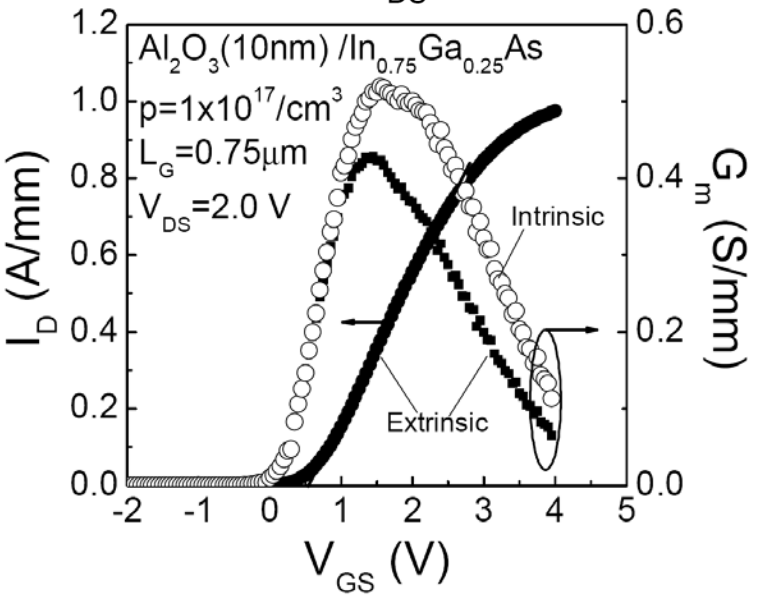
D. –H. Kim et al., IEEE EDL, p. 830, (2008)
D. –H. Kim et al., IEDM, p. 719, (2008)

Surface channel InGaAs MOSFET with non-self-aligned Process



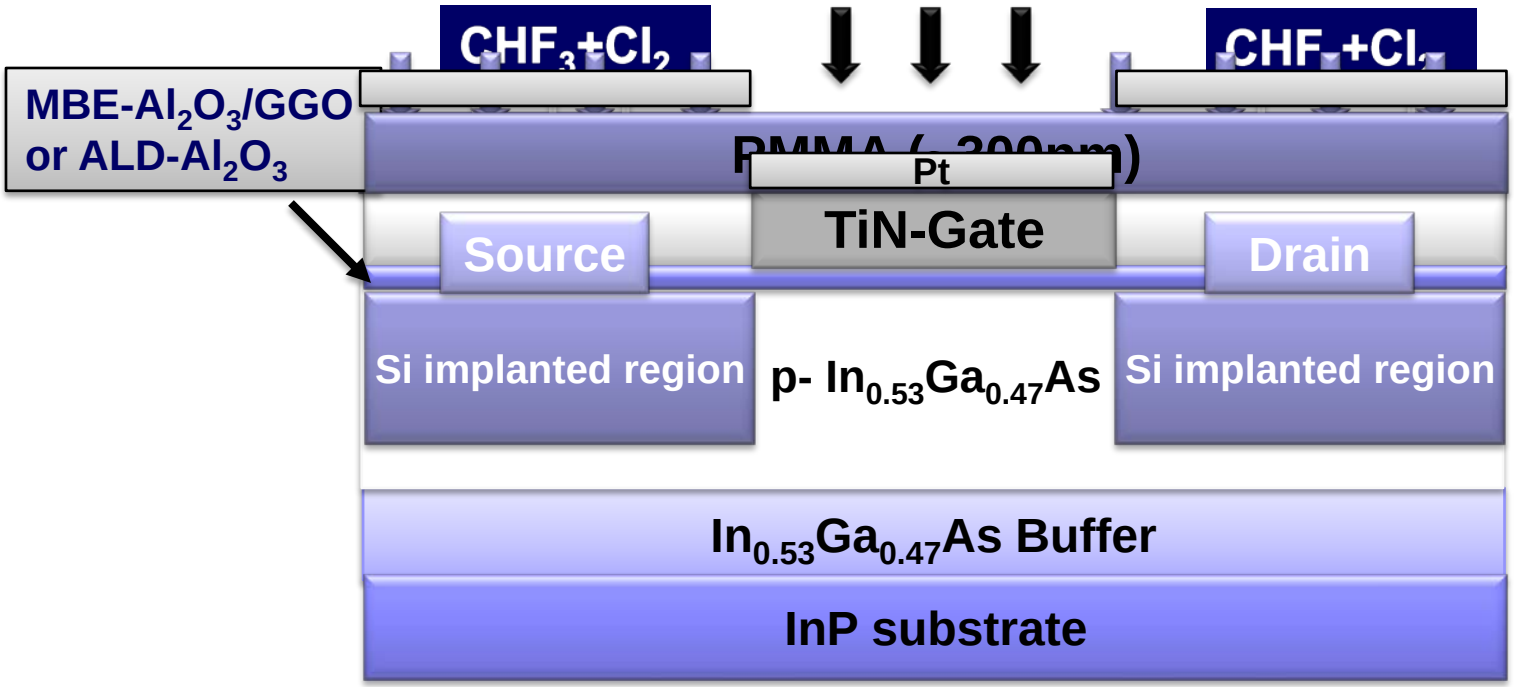
1) NH_4OH surface pretreatment
2) ALD Al_2O_3 30nm as an encapsulation layer
2) S/D patterning and Si implantation (30KeV/1E14 & 80KeV/1E14)
3) S/D activation using RTA (700-800°C 10s in N_2)
4) ALD re-growth: Al_2O_3
5) PDA: 400-600°C 30s in N_2
6) S/D contact patterning and Au/Ge/Ni ohmic metal evaporation and 400°C metallization
7) Gate patterning and Ni/Au or Al/Au evaporation





Y. Xuan et al., IEDM, p. 371, (2008)

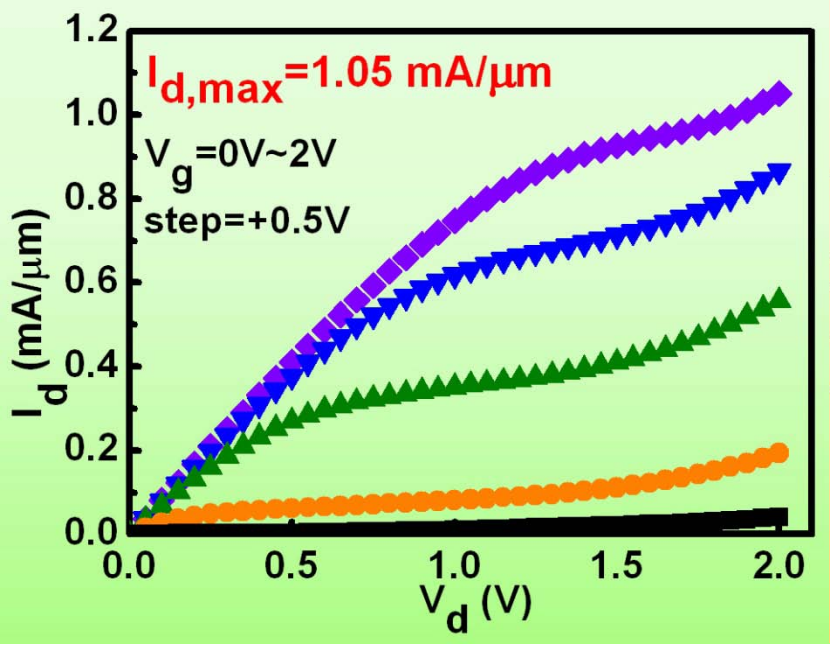
Self-aligned inversion-channel InGaAs MOSFET

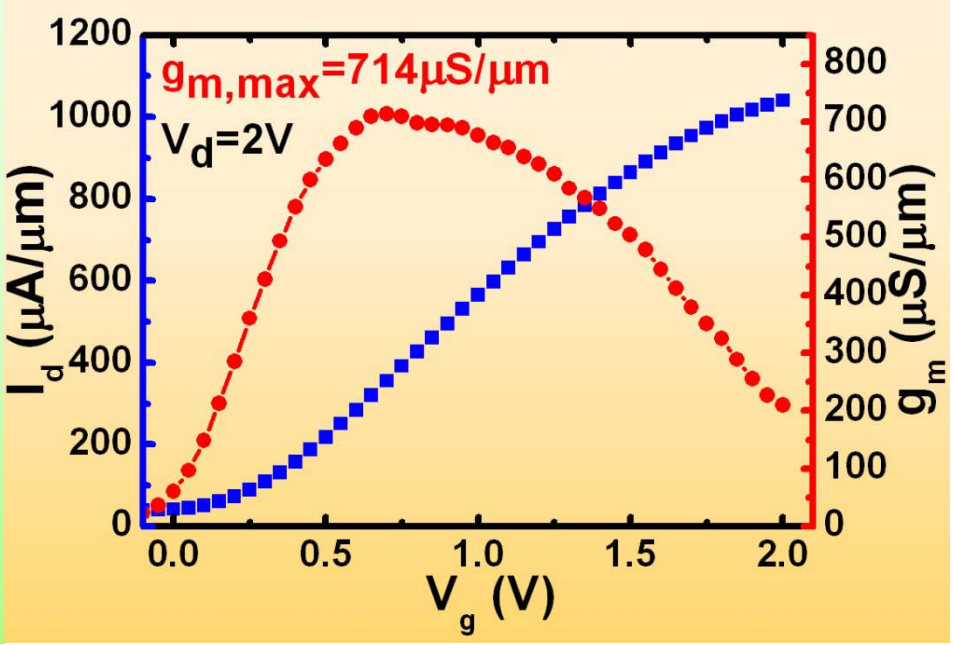


1. TiN sputtering
2. PMMA coating, E-beam writing, and hard mask deposition
3. Dry-etching
4. S/D patterning, implantation & activation
5. S/D contact region patterning, wet-etching of oxide, contact metal deposition, lift-off & ohmic alloying

Output & Sub-threshold Characteristics

Self-aligned inversion-channel TiN/Al_2O_3/GGO/$In_{0.53}Ga_{0.47}As$/InP MOSFET

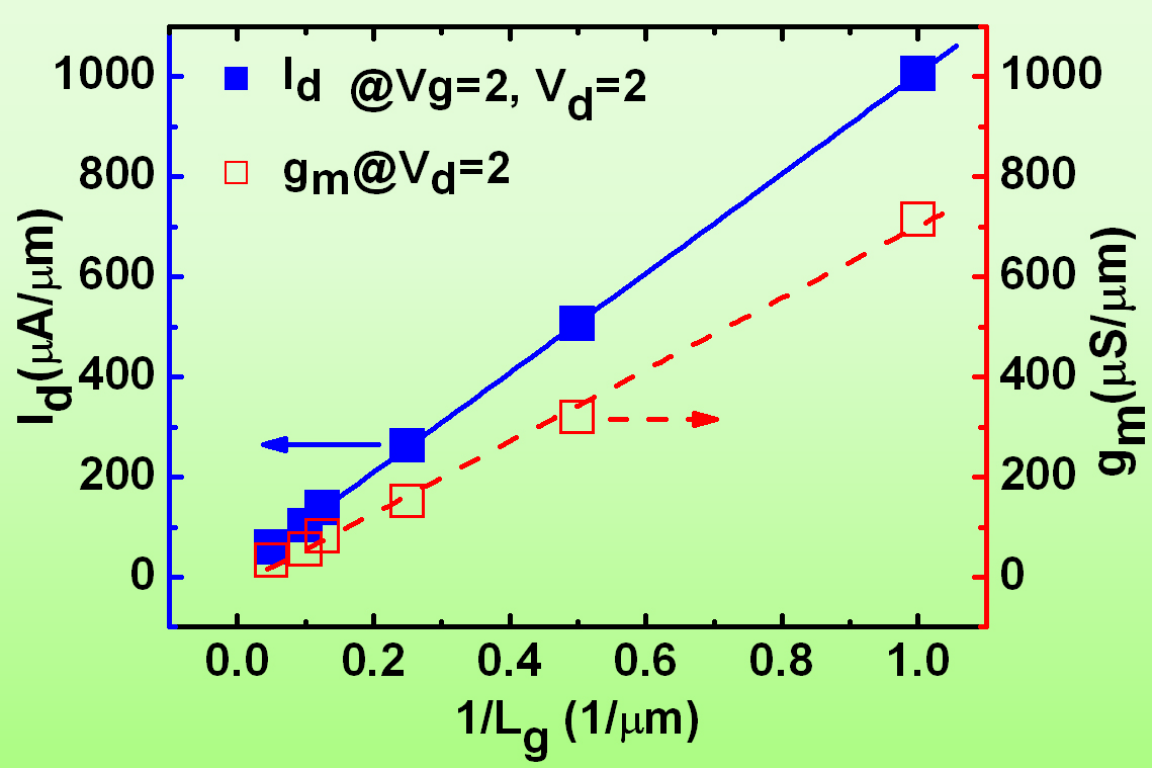




1. t_{TiN}= 160nm, $t_{Al_2O_3}$=2nm, t_{GGO}=5nm, W/L=10/1μm
2. $I_{d,max}$=1.05 mA/μm @V_g=2V, V_d=2V
3. $g_{m,max}$=714 μS/μm @V_g=0.7V, V_d=2V
4. V_{th}~0.2V, μ_{FE}=1300 $cm^2/V{\cdot}s$ (from transconductance analysis)

Si NMOSFET
90nm node
L_g~45nm
$I_{d,sat}$~1 mA/μm

Performance Trend

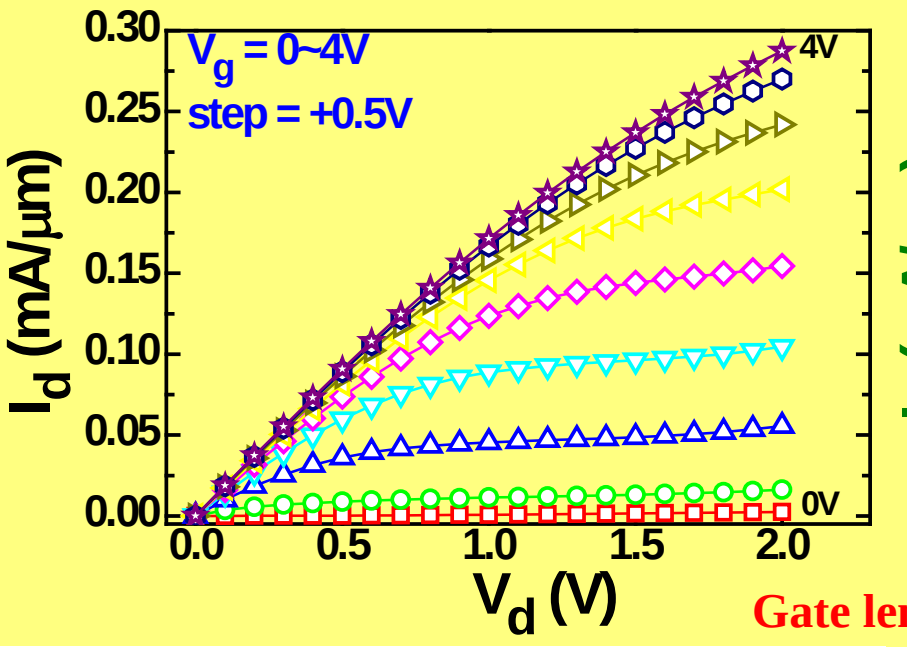


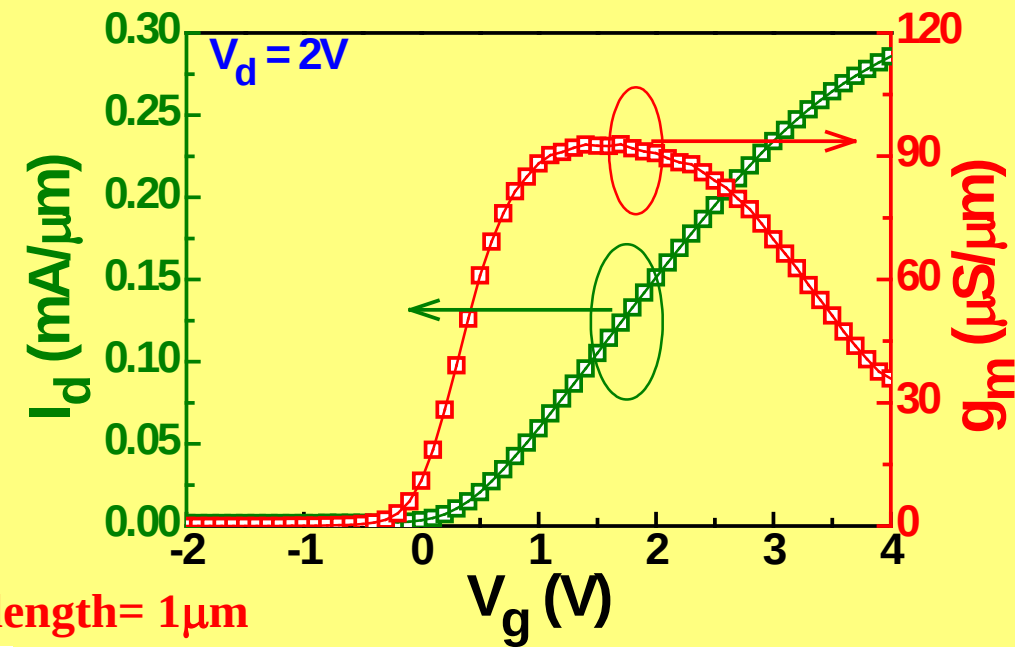
Performance for Si 32 nm node
$I_{d,sat}$ = 1.5-1.6 mA/μm

Estimated Performance For L_g=0.5μm

L_g	20μm	10μm	8μm	4μm	2μm	1μm	0.5μm	0.35 μm
$I_{d,sat}$ (μA/μm)	60	104	140	263	506	1050	~2mA/μm	~3mA/μm
$g_{m,max}$ (μS/μm)	34	56	81	152	320	714	~1.4mS/μm	~2.1mS/μm

ALD-Al_2O_3 on $In_{0.53}Ga_{0.47}As$ MOSFETs

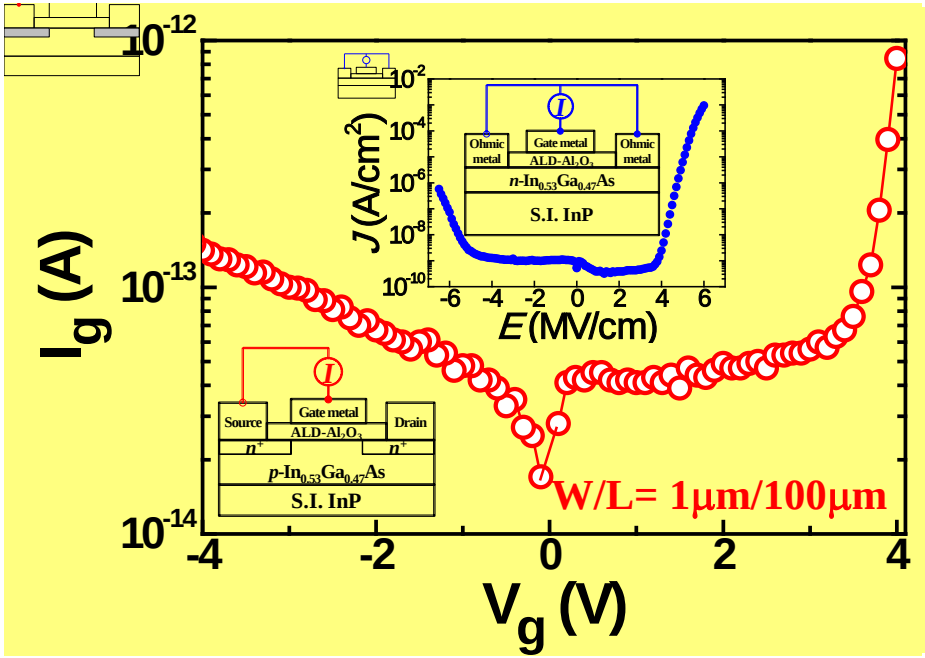


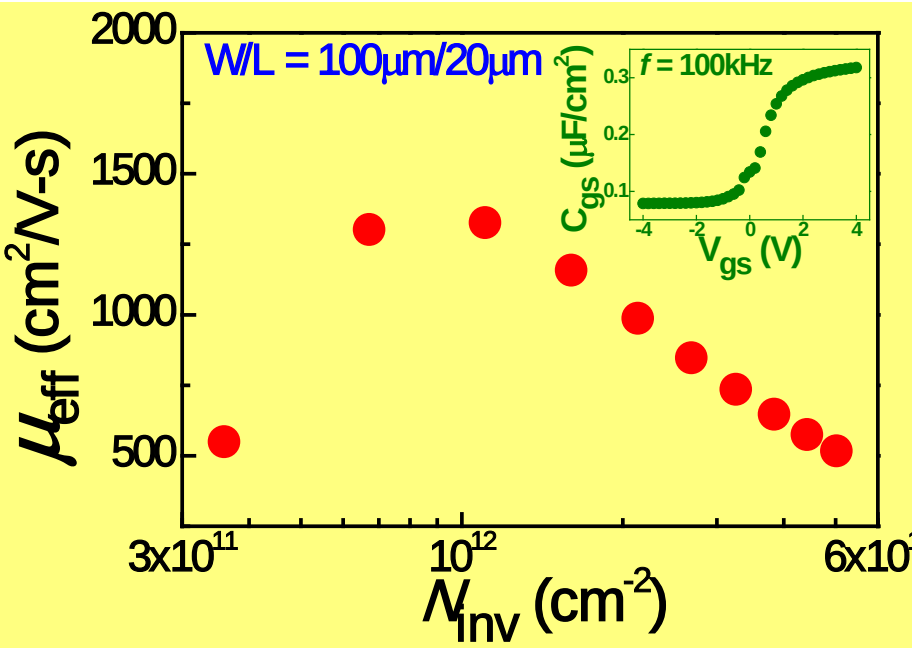


Gate length= 1μm

- Short air-exposure between ALD-Al_2O_3 and InGaAs
- Self-aligned process
- $I_{d,max}$= 288 mA/μm @V_g= 4V, V_d= 2V
- g_m= 93 μS/μm @V_g=1.6V, V_d=2V

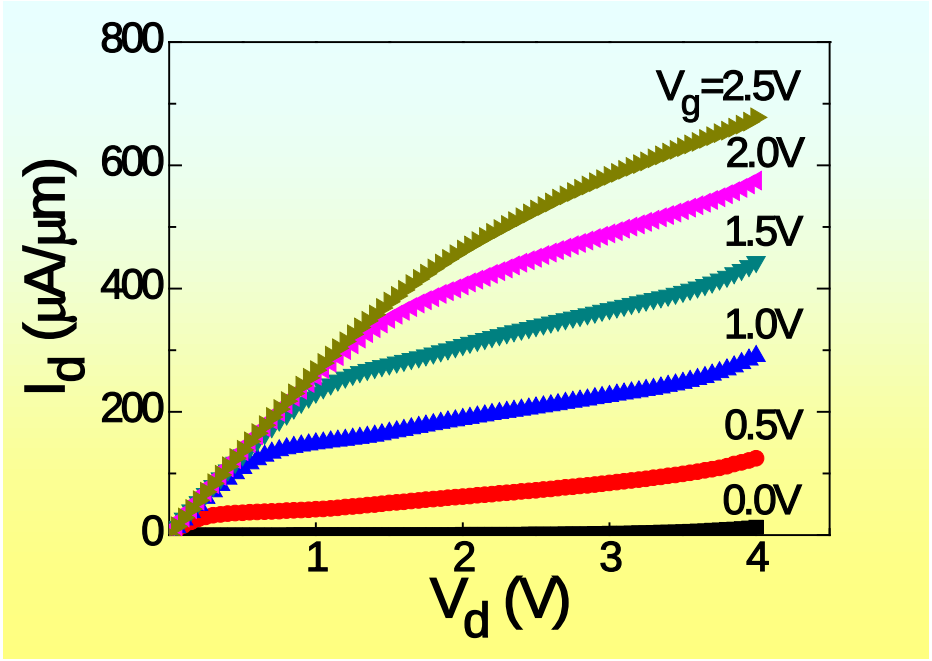
ALD-Al_2O_3 on $In_{0.53}Ga_{0.47}As$ MOSFETs

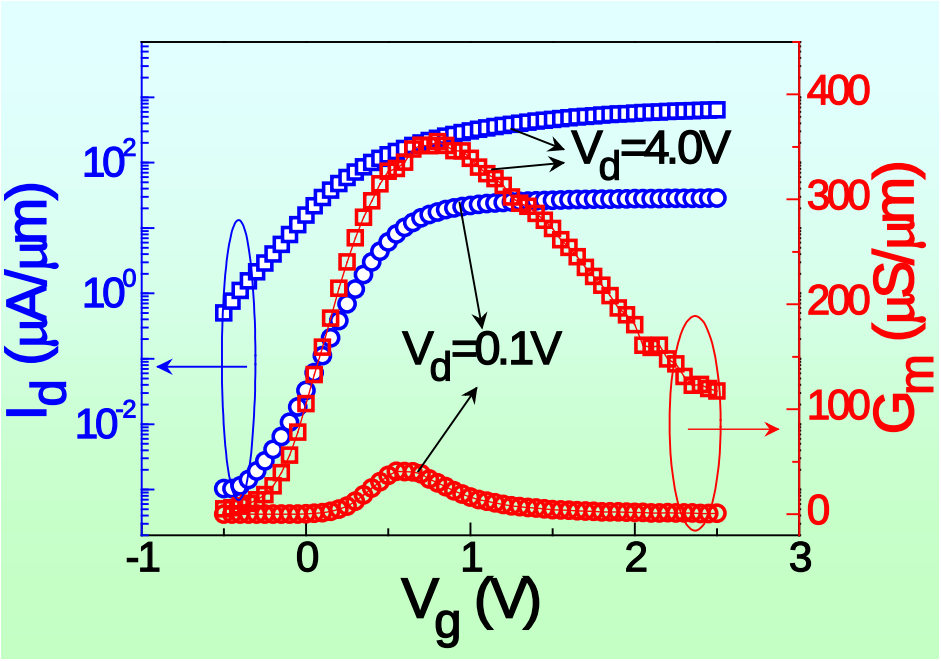




- Low leakage current density for TiN/ALD-Al_2O_3/InGaAs withstanding dopant activation temp up to 750°C for 15 sec
- Gate-to-source leakage current <10^{-12}A @V_g= 4V
- High peak electron mobility of 1330 cm^2/V-s (split-CV)

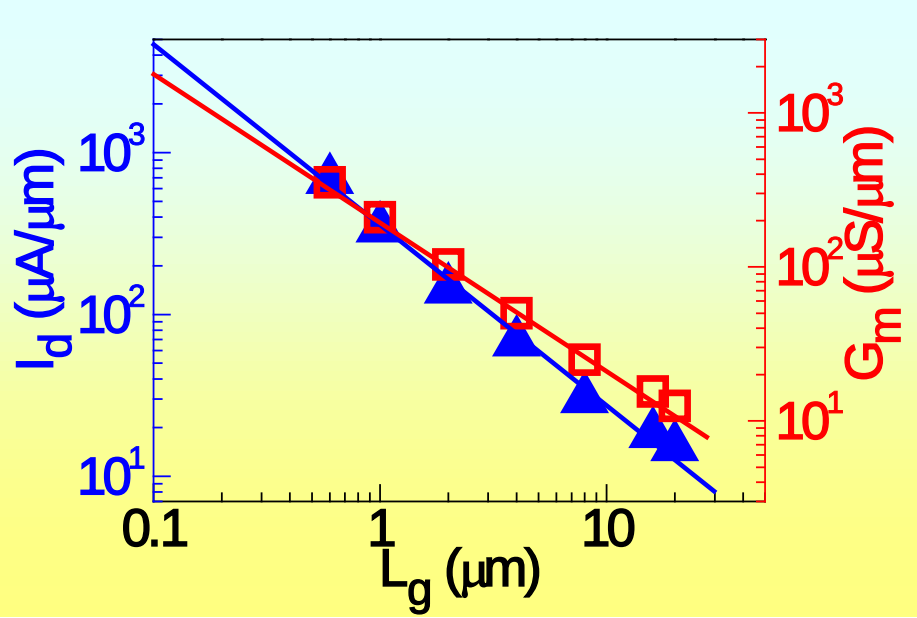
Sub-micron Gate Length
ALD- $Al_2O_3/In_{0.53}Ga_{0.47}As$/InP MOSFET

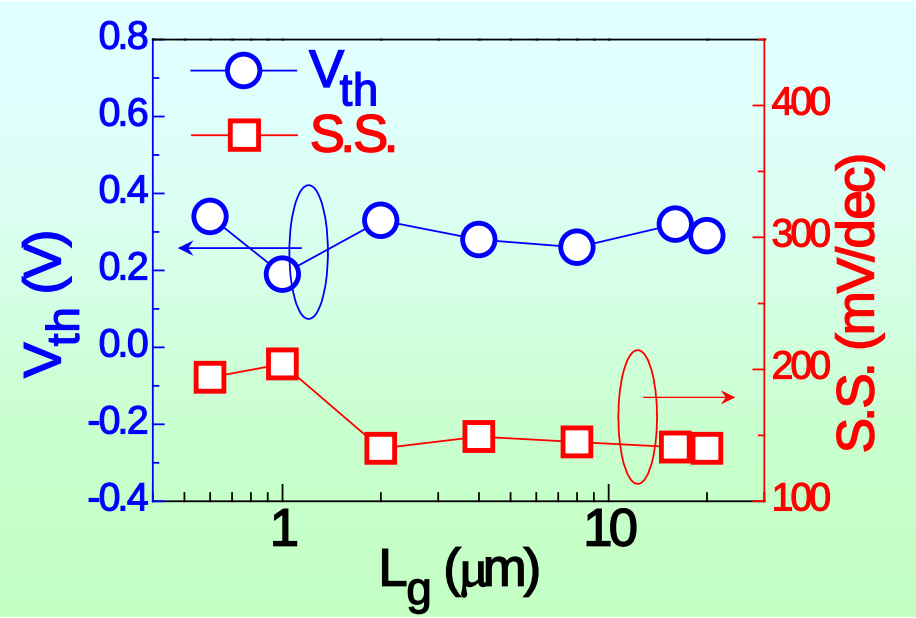




- W/L= 100/0.6μm, t_{ox}= 6nm, CET ~3nm
- $I_{d,max}$= **678 μA/μm** @V_g= 2.5V, V_d= 4V
- $g_{m,max}$= **354 μS/μm** @V_g= 0.8V, V_d= 4V
- V_{th}= 0.35V, I_{on}/I_{off}= 1.7×10^3

Sub-micron Gate Length
ALD- $Al_2O_3/In_{0.53}Ga_{0.47}As$/InP MOSFET





channel doping (cm^{-3})	T_{ox} (CET) [nm]	SIC* (cm^{-3})	T_a ** (°C)	R_s *** (Ω/□)	ρ_c **** (Ω · cm^2)	$I_{d,max}$ (μA/μm) @L_g=1μm	G_m (μS/μm) @L_g=1μm	I_{on}/I_{off} @V_{ds}=2V	S.S. (mV/dec)	DIBL (mV/V)
5×10^{16}	10(5)	5×10^{18}	650	717	1.28×10^{-5}	164	60	$<10^2$	164	111
5×10^{16}	10(5)	5×10^{18}	750	428.2	1.23×10^{-5}	280	90	$\sim10^2$	273	44
5×10^{16}	10(5)	1×10^{19}	650	223.8	2.95×10^{-6}	272	91.5	$\sim10^2$	151	80
5×10^{16}	10(5)	1×10^{19}	750	216.4	4.81×10^{-7}	288	93	$\sim10^2$	275	50
1×10^{17}	6(3)	1×10^{20}	650	66.6	3.05×10^{-6}	678 @L_g=0.6μm	354 @L_g=0.6μm	1.7×10^3	194	75

*simulated implanted-ion concentration, **activation temperature, *** sheet resistance, ****specific contact resistance

E-mode III-V MOSFETs
Benchmark

- Natl Tsing-Hua Univ.
- Univ. Singapore
- Bell Labs
- Purdue Univ.
- Freescale Univ. Glasgow
- IBM

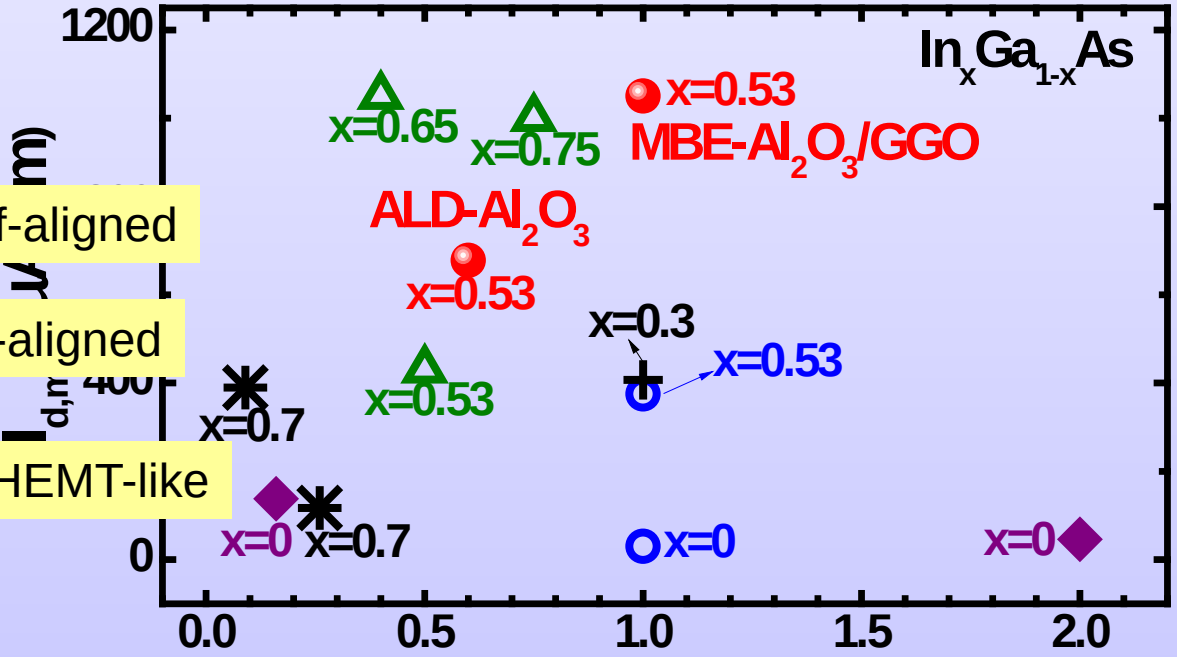
Self-aligned

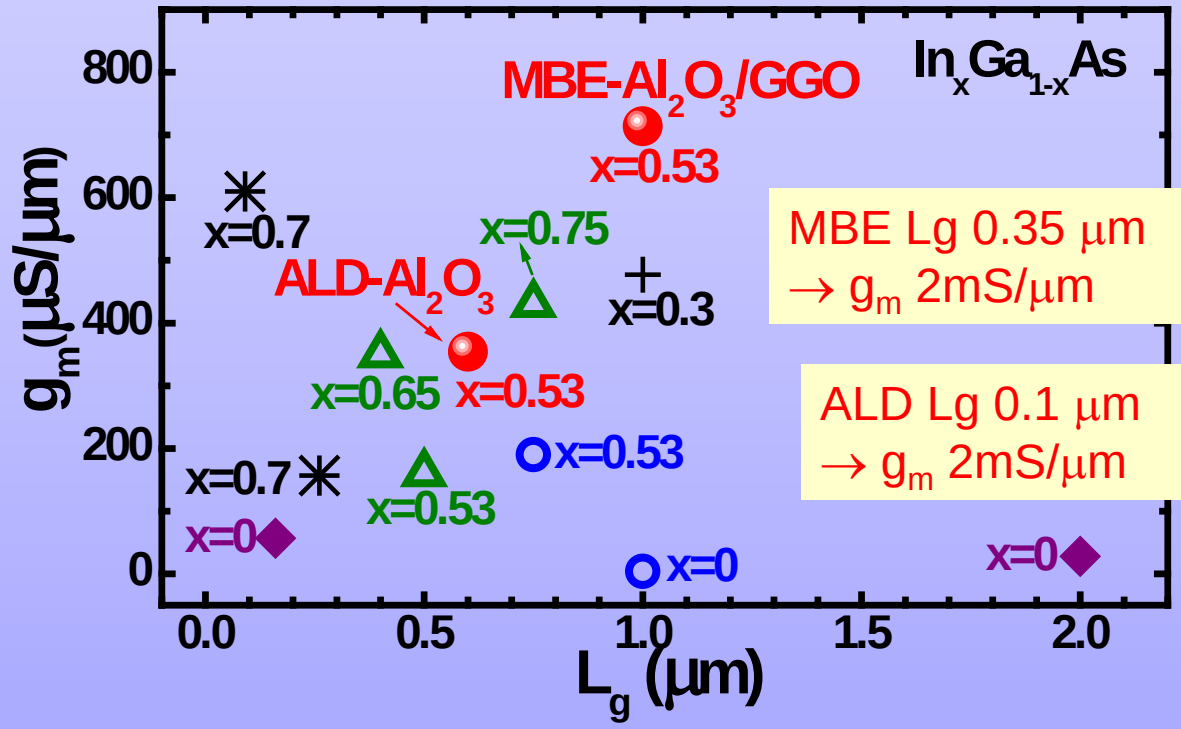
Non-self-aligned

HEMT-like

MBE-Al_2O_3/GGO/$In_{0.53}Ga_{0.47}As$
L_g=1μm
I_d= 1.05 mA/μm
g_m= 714 μS/μm
T. D. Lin et al.,
APL 93, 033516 (2008)

ALD-Al_2O_3/$In_{0.53}Ga_{0.47}As$
L_g=0.6μm
I_d= 678 μA/μm
g_m= 354 μS/μm





MBE Lg 0.35 μm
→ g_m 2mS/μm

ALD Lg 0.1 μm
→ g_m 2mS/μm

Key – high κ's/InGaAs interface

- Toward Fermi-level Unpinning and have achieved it
- GGO scalability and high-temperature thermodynamic stability of GGO/InGaAs
- Energy parameters
- MOSCAPs with different work function metals

Key – high κ's/InGaAs interface

- Toward Fermi-level Unpinning and have achieved it
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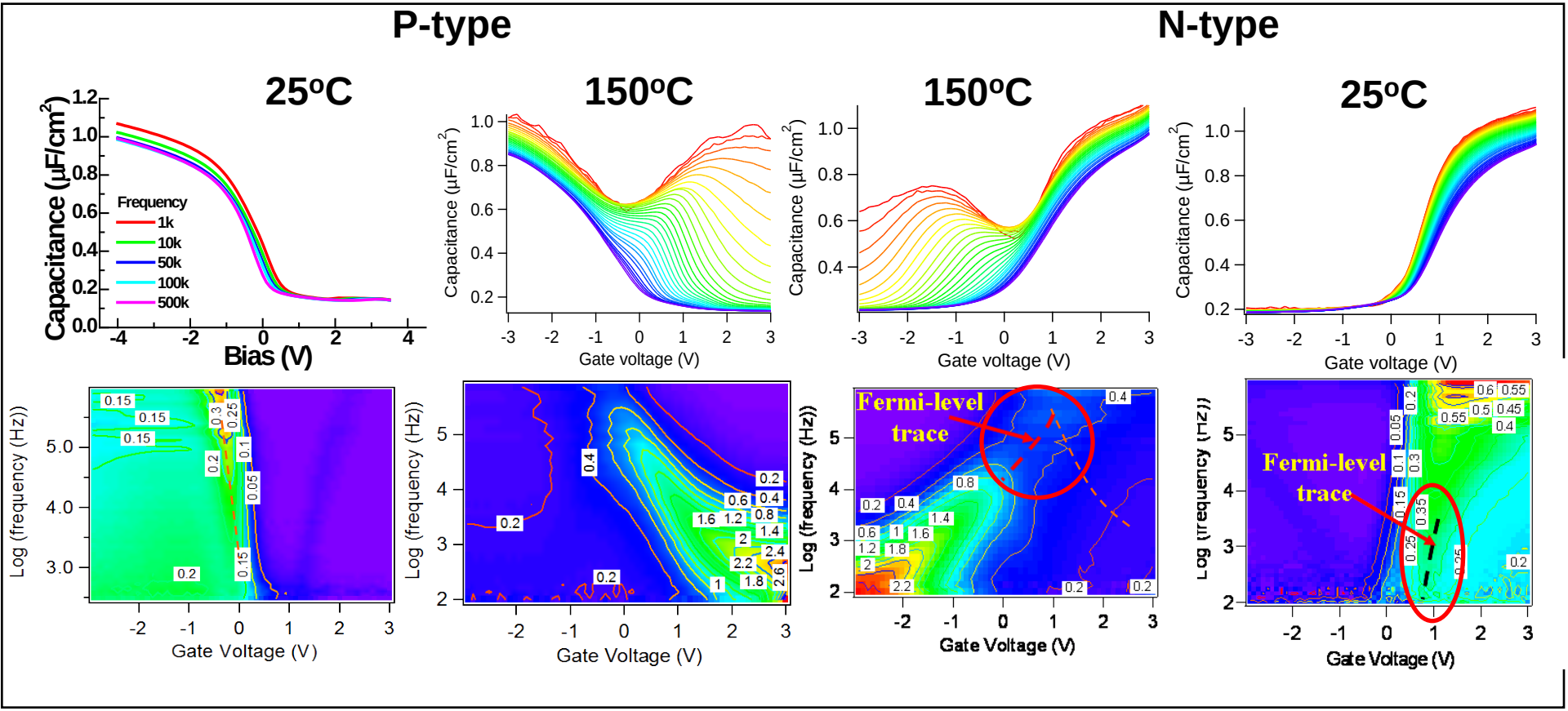
- Energy parameters
- MOSCAPs with different work function metals

In-situ MBE-Al_2O_3/GGO/ n- and p-$In_{0.2}Ga_{0.8}As$



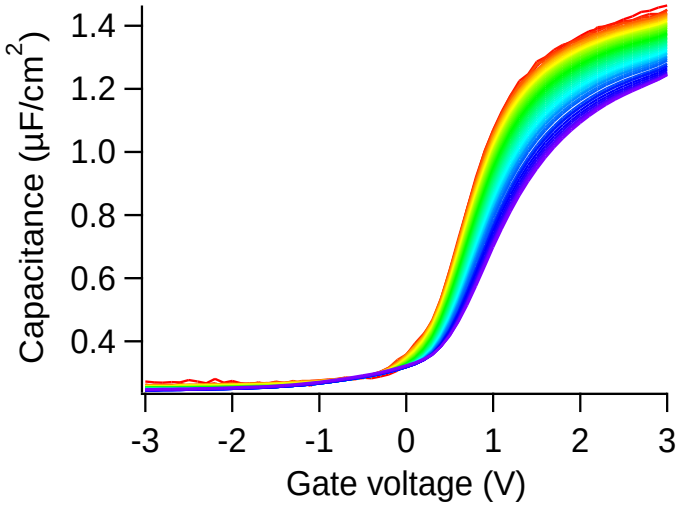
Fermi-level movement efficiency (FLE), an "aid" to show effectiveness of passivation;

FLE ~100% for perfected SiO_2/Si

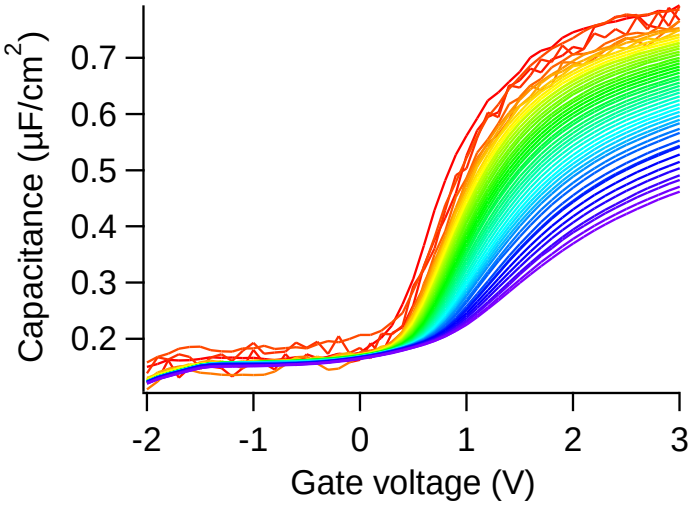
FLE ~ 30% near mid-gap at 150ºC, and much higher away from mid-gap at 25ºC in the p- and n-samples

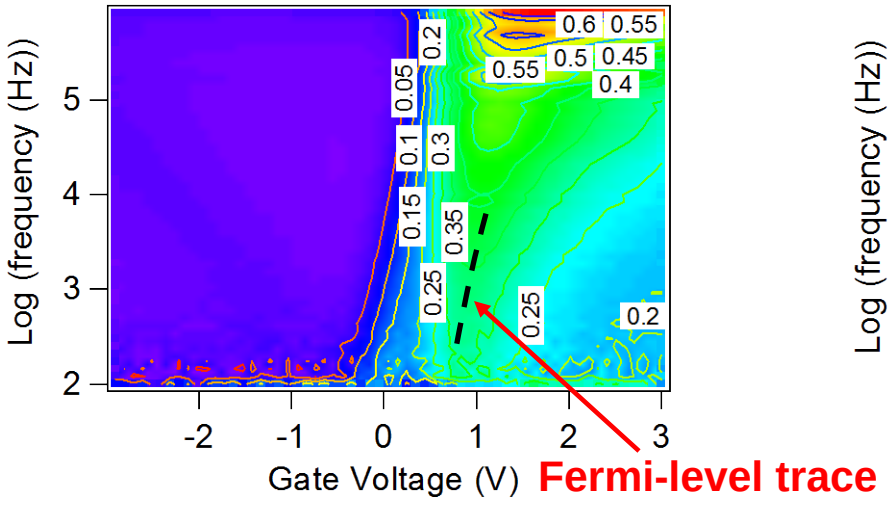
Comparison between Al_2O_3/GGO and ALD-Al_2O_3 n-$In_{0.2}Ga_{0.8}As$ at room temperature

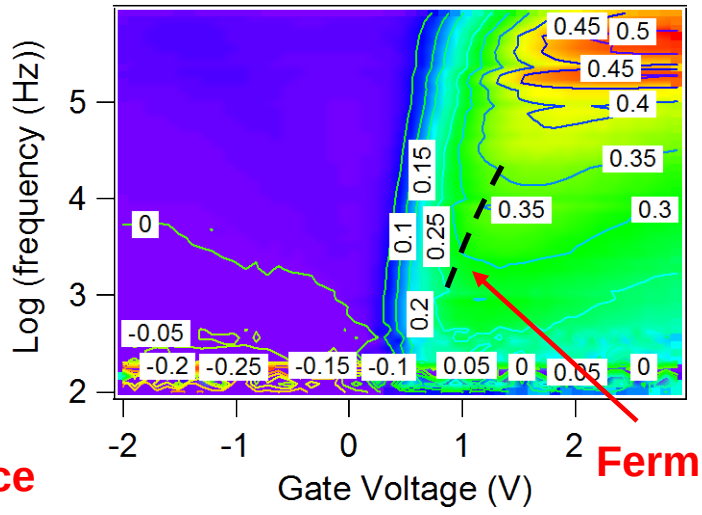
NTHU sample-Al_2O_3(3nm)/ GGO(8.5nm) on $In_{0.2}Ga_{0.8}As$



IMEC sample –ALD Al_2O_3(10nm) on $In_{0.15}Ga_{0.85}As$







GGO/ InGaAs showed much better CV / GV (compared with that of ALD)

Fermi-Level Movement Efficiency (FLME) with Quasi-Static CV

Berglund's integral

$$\psi_s(V_G) - \psi_s(V_{FB}) = \int_{V_{FB}}^{V_G} \left(1 - \frac{C}{C_{ox}}\right)$$

C. N. Berglund et al., IEEE Trans. Electron Dev. Vol. 13, 701 (1966)

Assume gate voltage changes- $\triangle V_g$,

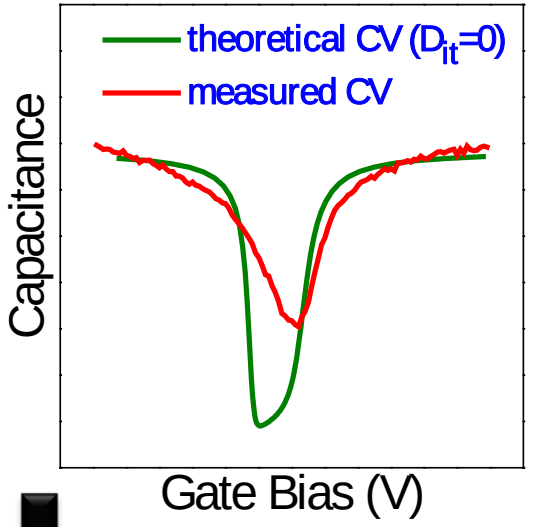
Fermi-level of a measured CV moves $\triangle \psi_s{}^m$

and an theoretical CV (D_{it}=0) moves $\triangle \psi_s{}^{id}$

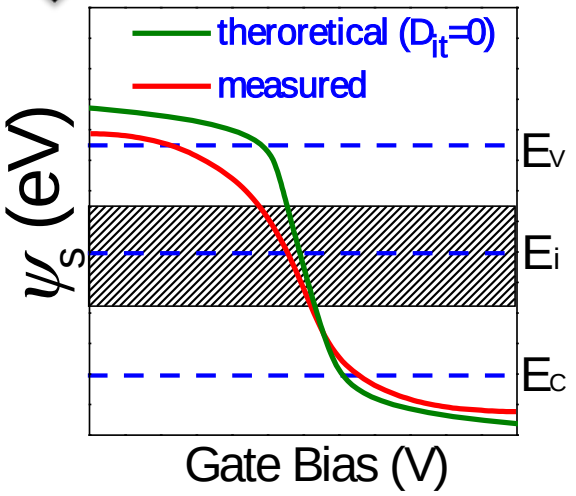
$$\text{Fermi-level movement efficiency (FLME)} = \frac{\triangle \psi_s{}^m}{\triangle \psi_s{}^{id}}$$

$$\frac{\triangle \psi_s{}^m}{\triangle \psi_s{}^{id}} = \frac{\triangle \psi_s{}^m / \triangle V_g}{\triangle \psi_s{}^{id} / \triangle V_g}$$

$$\Rightarrow \text{FLME}(\%) = \frac{\text{measured } \psi_s \text{ - } V_g \text{ slope}}{\text{theoretical } \psi_s \text{ - } V_g \text{ slope}} \times 100\%$$

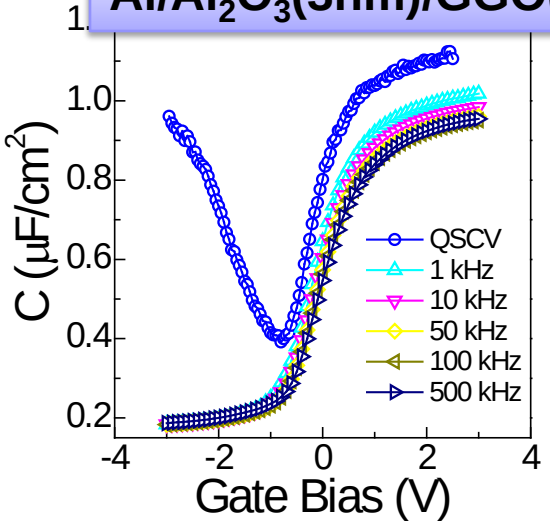


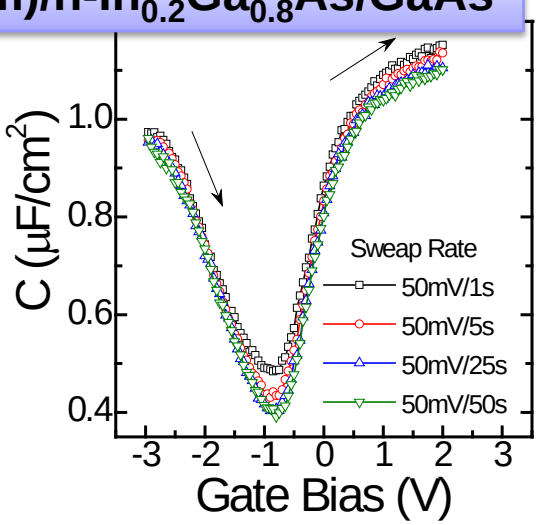
Berglund's integral



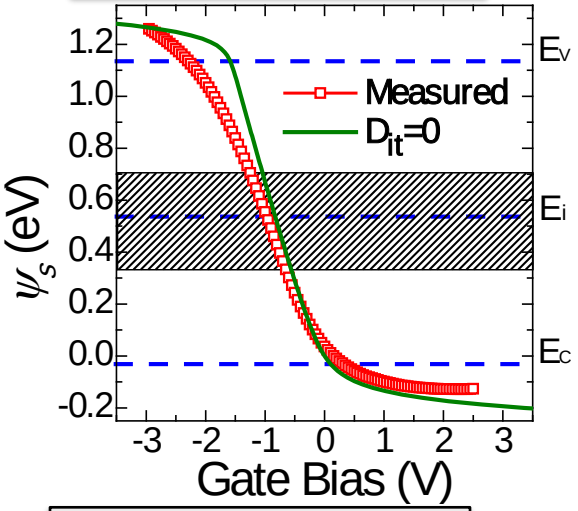
Fermi-Level Movement Efficiency (FLME)

$Al/Al_2O_3(3nm)/GGO(7nm)/n\text{-}In_{0.2}Ga_{0.8}As/GaAs$

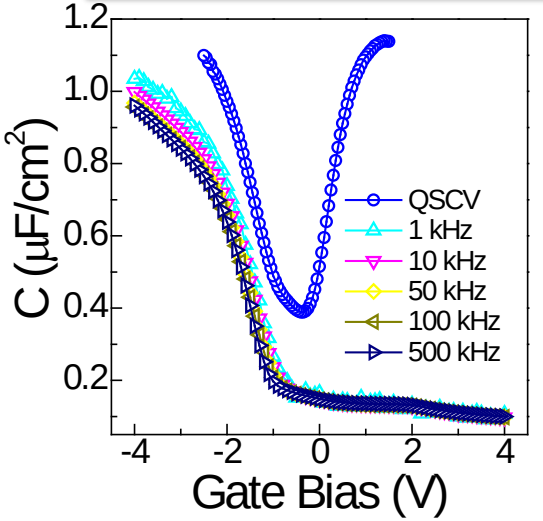


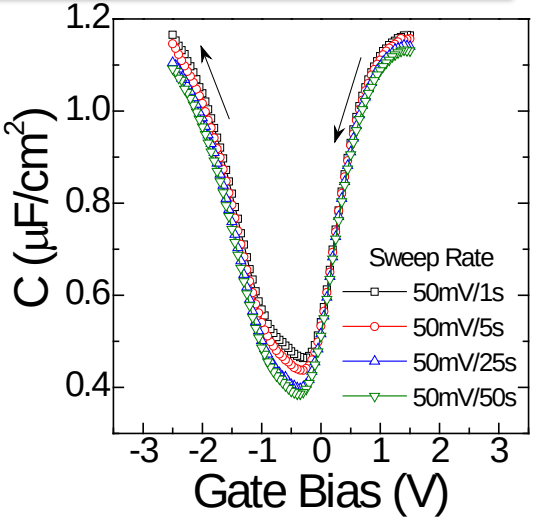


FLME~80%

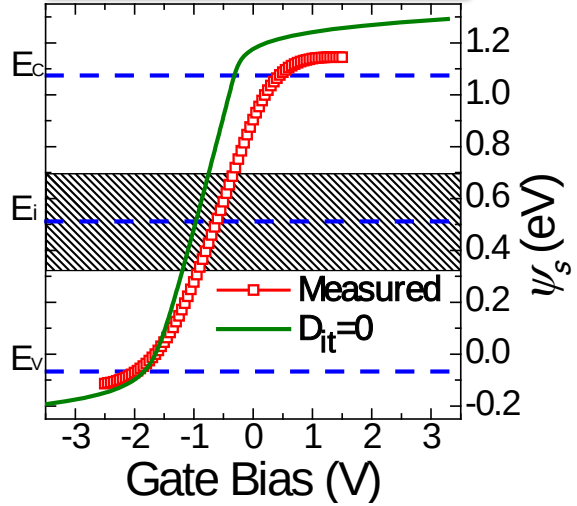


$Al/Al_2O_3(3nm)/GGO(5nm)/p\text{-}In_{0.2}Ga_{0.8}As/GaAs$





FLME~77%

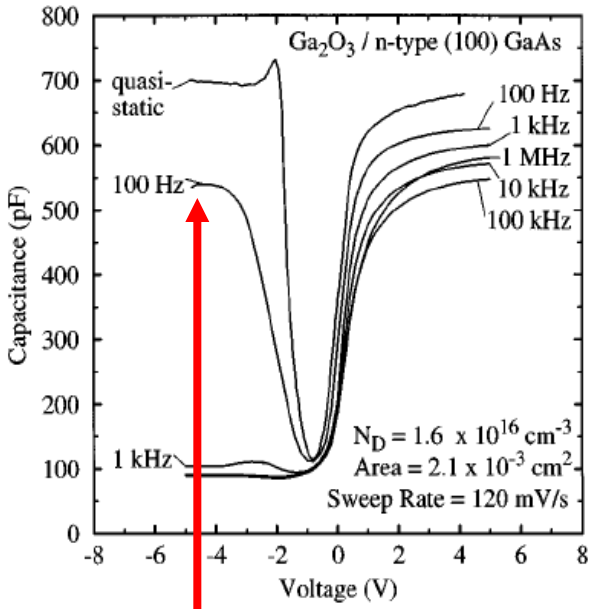


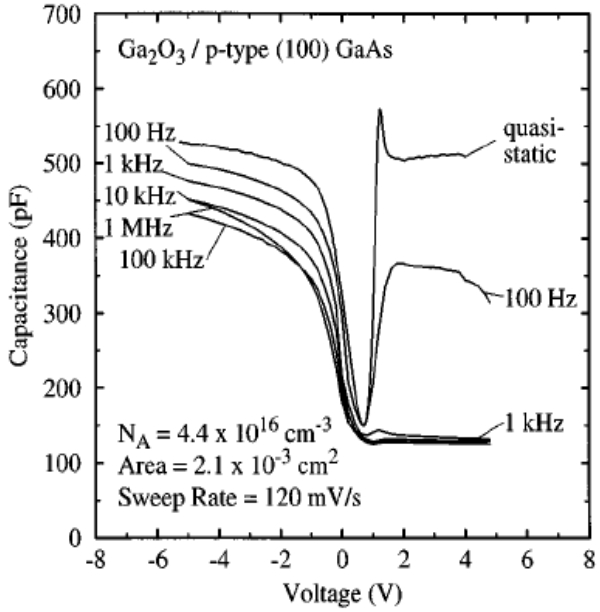
Quasistatic and high frequency capacitance–voltage characterization of Ga_2O_3–GaAs structures fabricated by *in situ* molecular beam epitaxy

M. Passlack,[a] M. Hong, and J. P. Mannaerts
AT&T Bell Laboratories, 600 Mountain Avenue, Murray Hill, New Jersey 07974

(Received 19 October 1995; accepted for publication 13 December 1995)

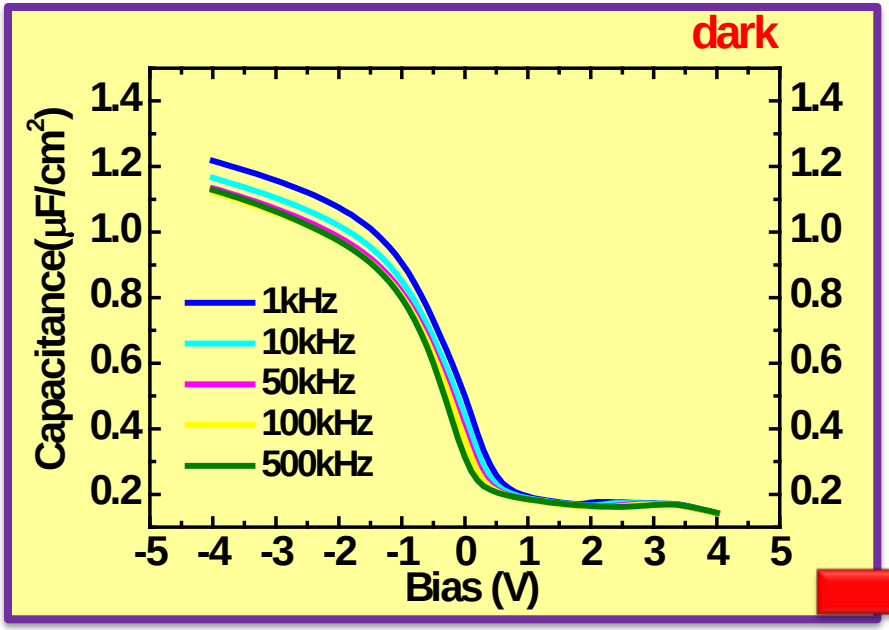
Interface properties of Ga_2O_3–GaAs structures fabricated using *in situ* multiple-chamber molecular beam epitaxy have been investigated. The oxide films were deposited on clean, atomically ordered (100) GaAs surfaces at ≅600 °C by electron-beam evaporation using a $Gd_3Ga_5O_{12}$ single-crystal source. Metal–insulator–semiconductor structures have been fabricated in order to characterize the Ga_2O_3–GaAs interface by capacitance–voltage measurements in quasistatic mode and at frequencies between 100 Hz and 1 MHz. The formation of inversion layers in both *n* and *p*-type GaAs has been clearly established. Using the quasistatic/high frequency technique, the interface state density has been derived as a function of band gap energy and a midgap interface state density in the mid 10^{10} cm^{-2} eV^{-1} range has been inferred. Charge trapping in the oxide has been revealed as the dominant trapping mechanism. [S0003-6951(96)03408-4]

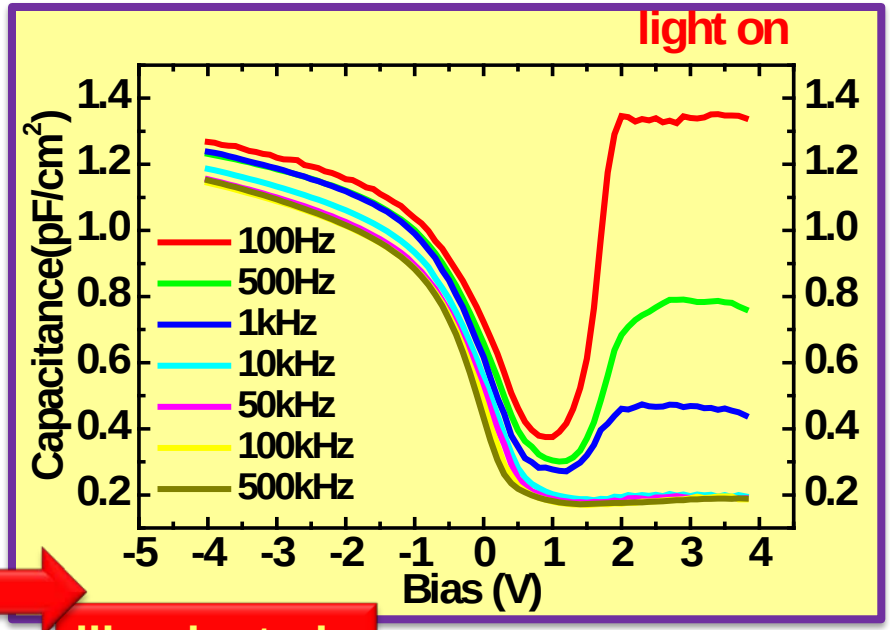




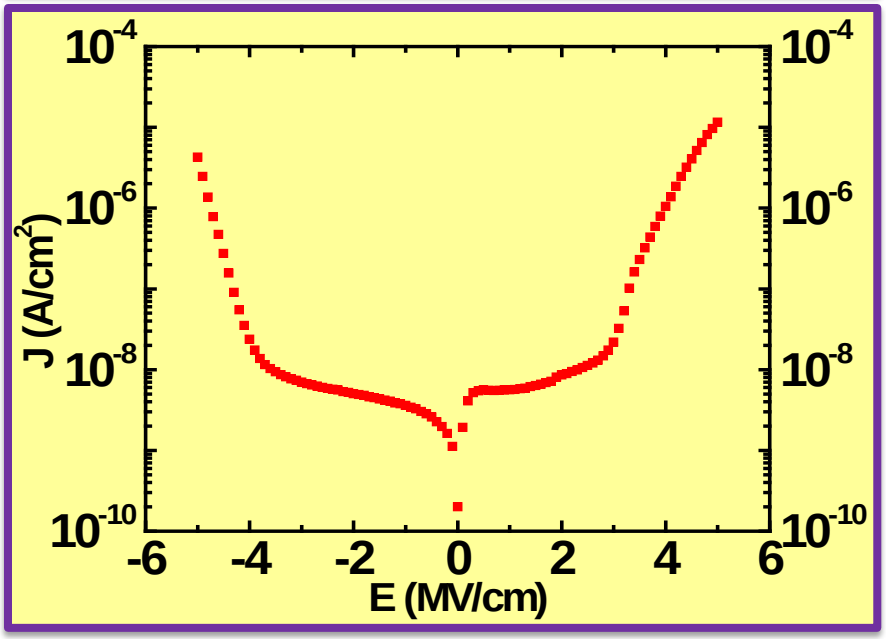
CV curve at 100 Hz should not rise up.

GGO Unpins the $In_{0.2}Ga_{0.8}As$ Fermi level





illuminated

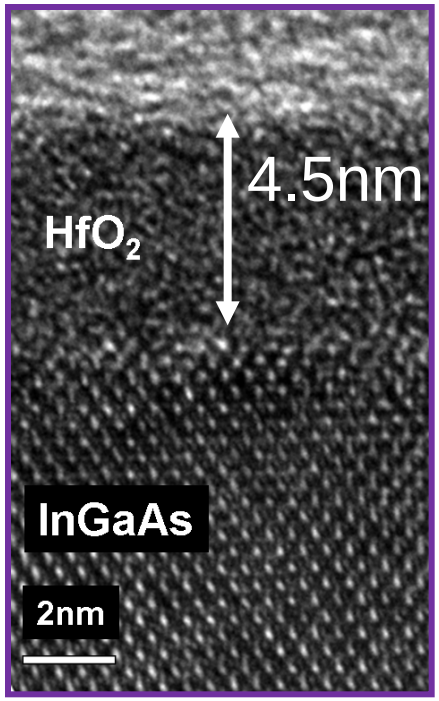


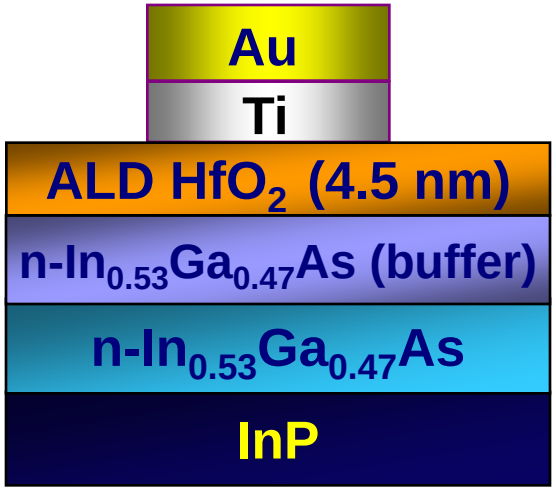
Al_2O_3/GGO/p-$In_{0.2}Ga_{0.8}As$/p-GaAs

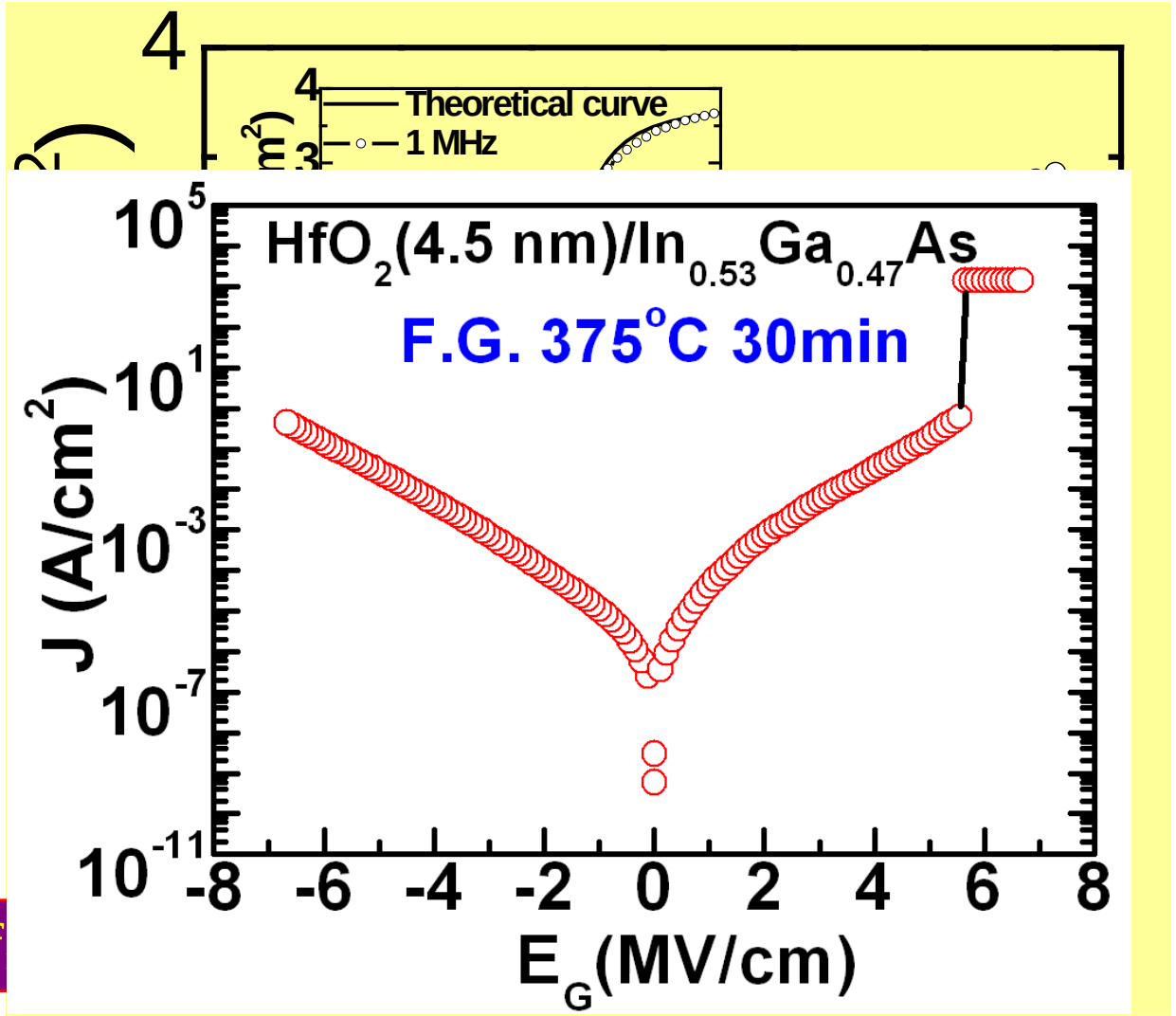
- High k :
  - GGO: 14-15
  - Al_2O_3: 8
- Low leakage
- **unpinned Fermi-level**
- **The role played by In ?**

ALD-HfO_2 on $In_{0.53}Ga_{0.47}As$ with short air exposure ~10 min

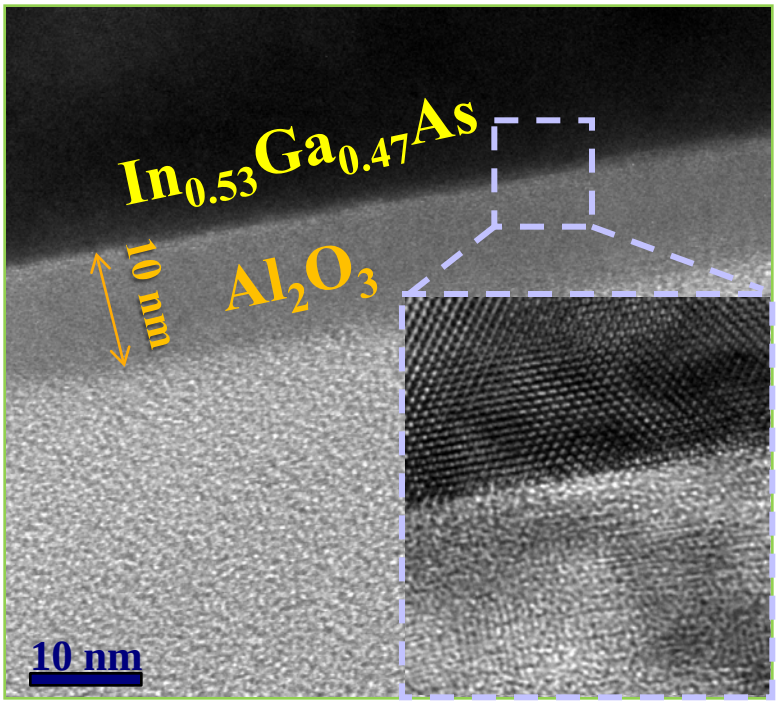
k ~17@100 kHz, CET=1nm

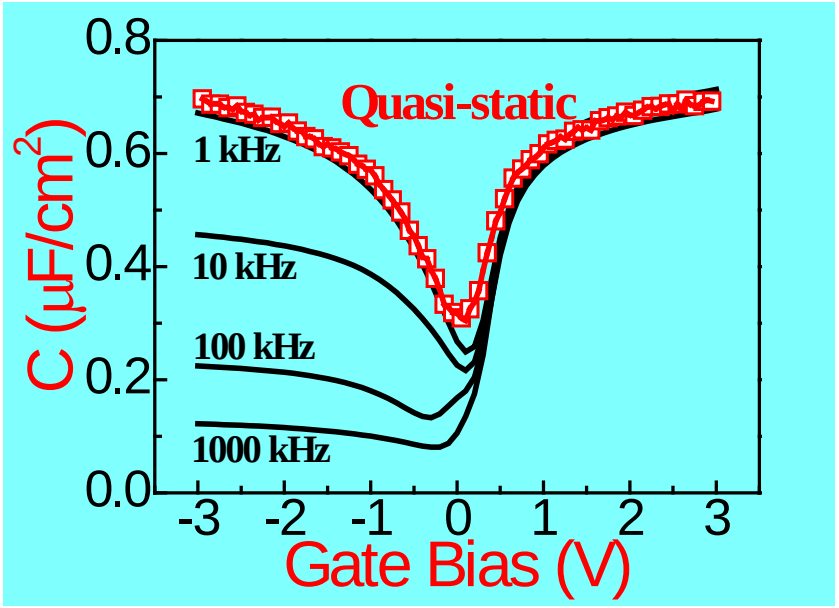




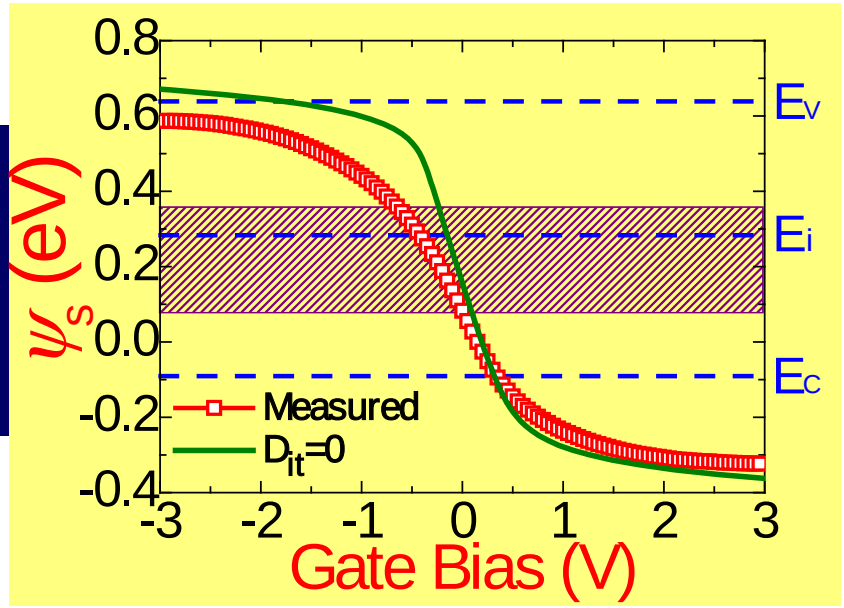


Achieving a low D_{it} in ALD-Al_2O_3 on $In_{0.53}Ga_{0.47}As$ with short air exposure





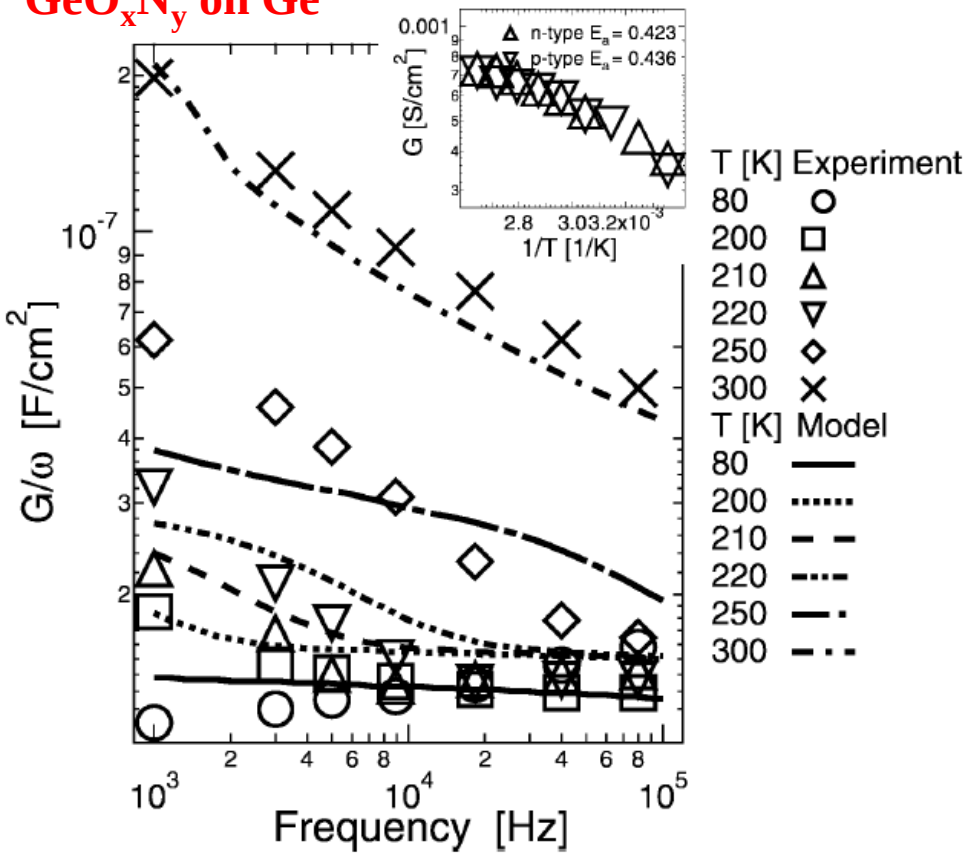
- very sharp Al_2O_3/InGaAs interface
- Fermi-level moves across the nearly entire bandgap
- high FLME of **63%** near midgap



H. C. Chiu et al., *Appl. Phys. Lett.*, 93, p202903 (2008)

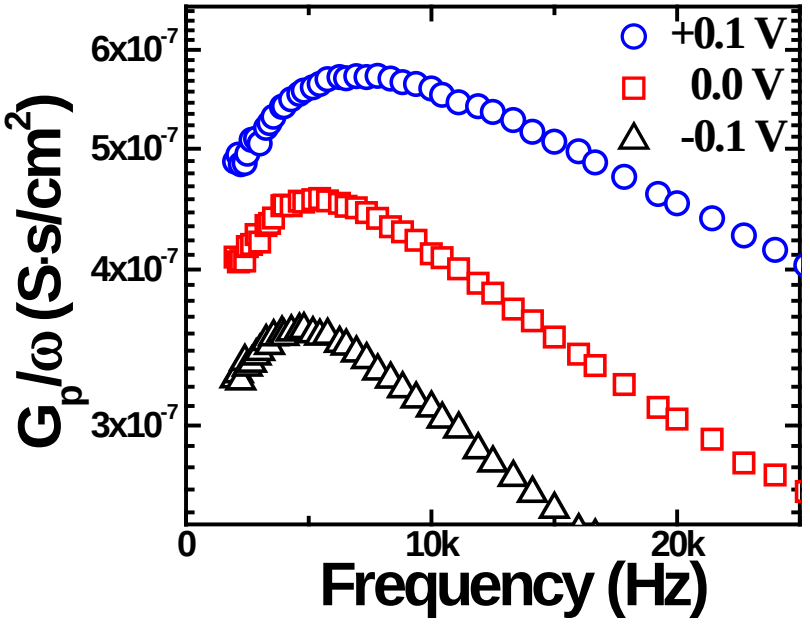
D_{it} Overestimation in Small Band-gap Semiconductors Using Conductance Method

GeO_xN_y on Ge



- D_{it}=8.5×10^{12} cm^{-2}eV^{-1} extracted at 300k
- Di_t=7.0×10^{11} cm^{-2}eV^{-1} extracted at 80k

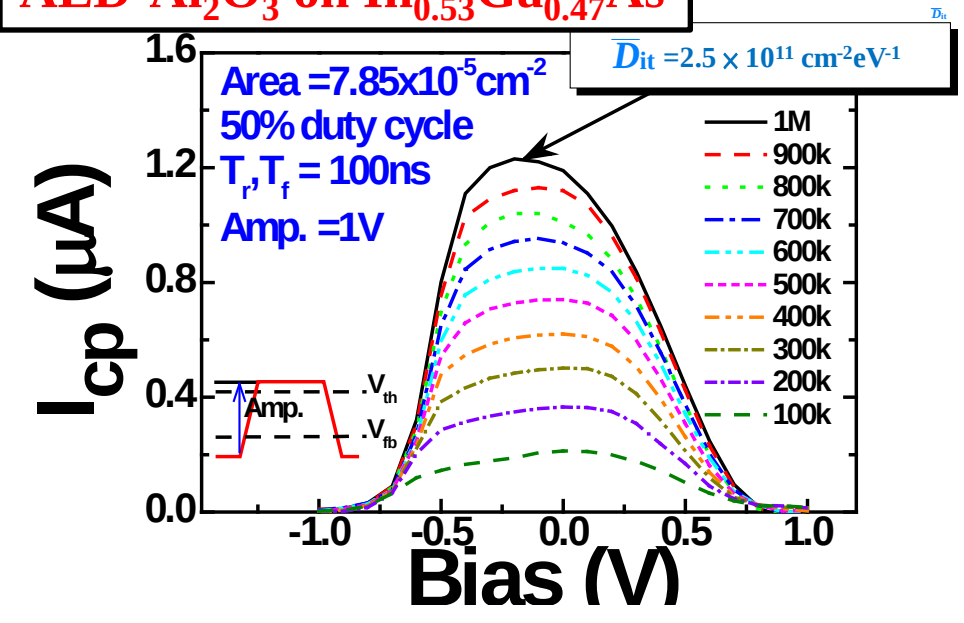
ALD-Al_2O_3 on $In_{0.53}Ga_{0.47}As$

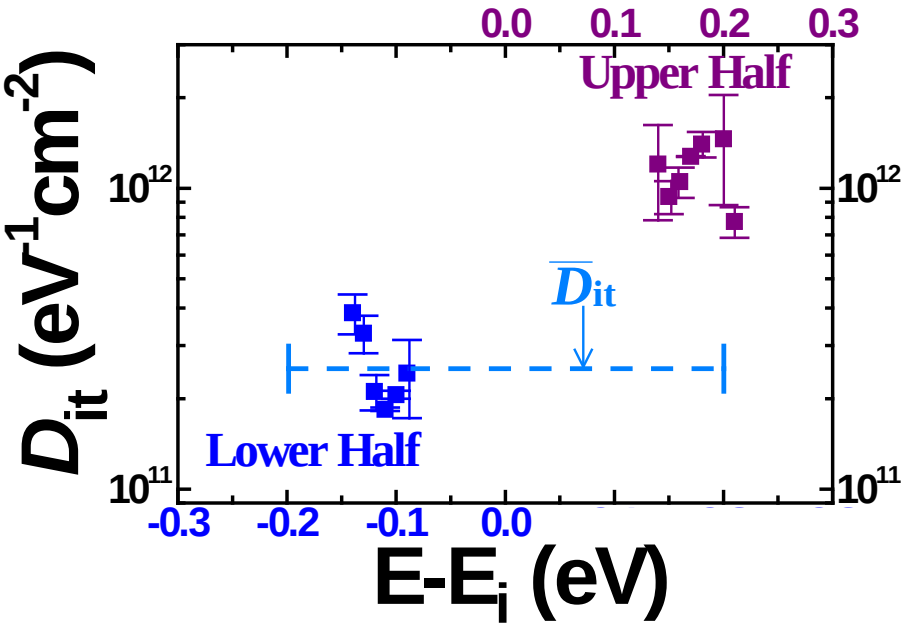


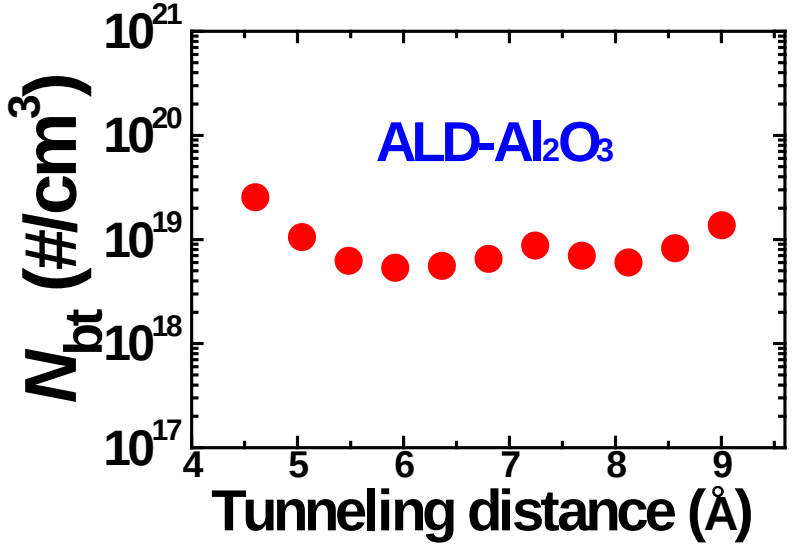
- D_{it}=3×10^{12} cm^{-2}eV^{-1} extracted at 300k
- Overestimating D_{it} due to weak inversion at depletion region

Charge Pumping

ALD-Al_2O_3 on $In_{0.53}Ga_{0.47}As$







- A low mean D_{it} ~ 2.5x10^{11} cm^{-2}eV^{-1} near midgap (±0.2eV)
- A D_{it} of ~ (2-4)x10^{11} cm^{-2}eV^{-1} in the lower half of the bandgap and 10^{12} cm^{-2} eV^{-1} in the upper half of the bandgap
- A low bulk trap density ~ 7x10^{18} cm^{-3}

Key – high κ's/InGaAs interface

- Toward Fermi-level Unpinning and have achieved it
- GGO scalability and high-temperature thermodynamic stability of GGO/InGaAs
- Energy parameters
- MOSCAPs with different work function metals

Summary of samples

N-type

- TH622

  MBE Al_2O_3/GGO(10nm)/$In_{0.2}Ga_{0.8}As$
- TH647

  MBE Al_2O_3/GGO(8.5nm)/$In_{0.2}Ga_{0.8}As$
- TH663

  MBE Al_2O_3/GGO(4.5nm)/$In_{0.2}Ga_{0.8}As$

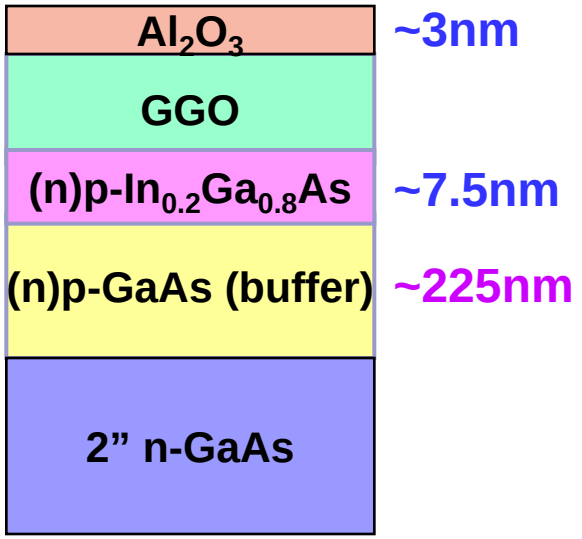
P-type

- TH834

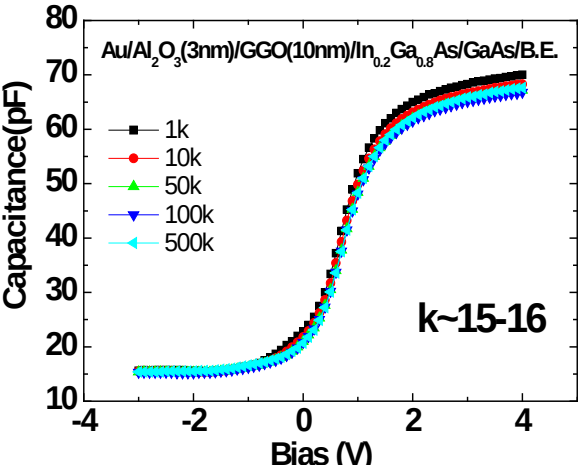
  MBE Al_2O_3/GGO(8.5nm)/$In_{0.2}Ga_{0.8}As$
- TH857

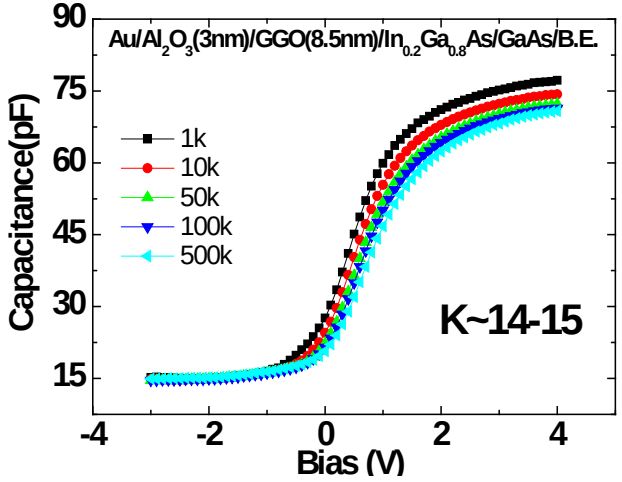
  MBE Al_2O_3/GGO(5.0nm)/$In_{0.2}Ga_{0.8}As$
- TH908

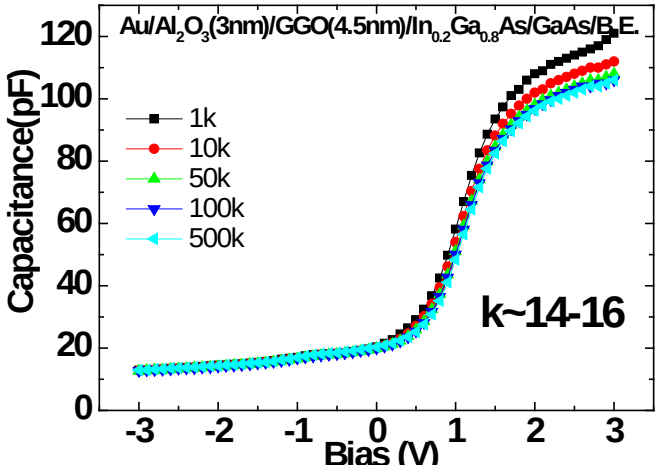
  MBE Al_2O_3/GGO(3.0nm)/$In_{0.2}Ga_{0.8}As$

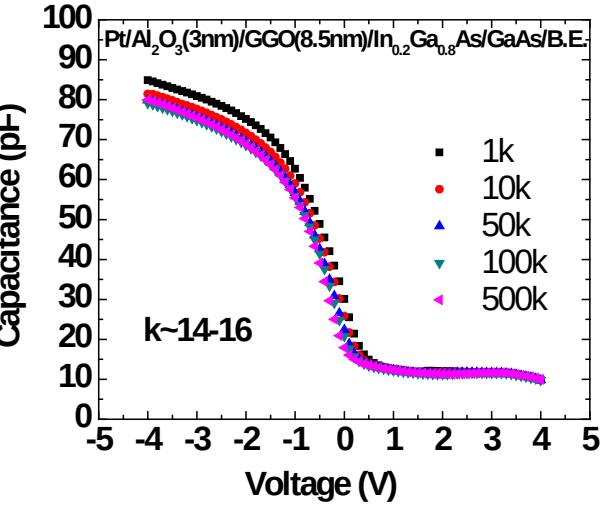


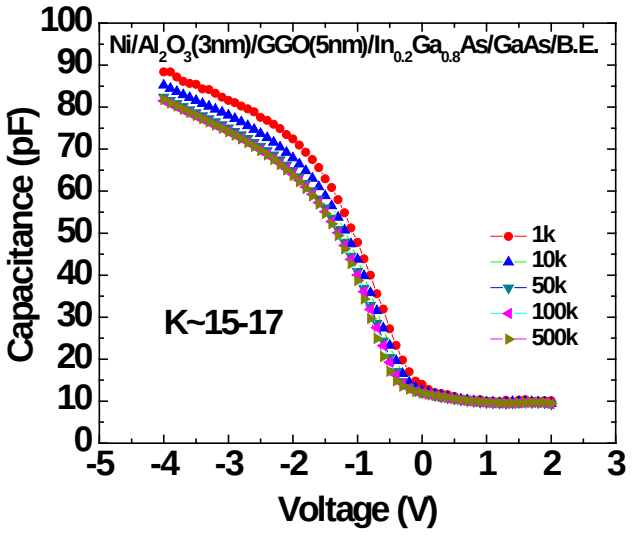
C-V Characteristics

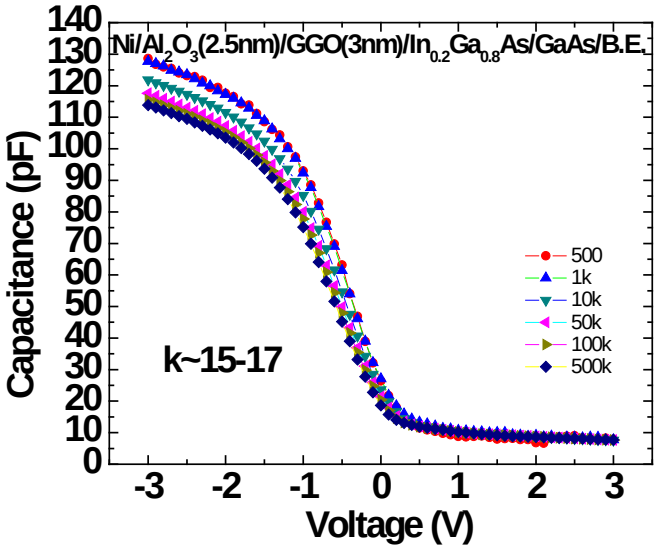




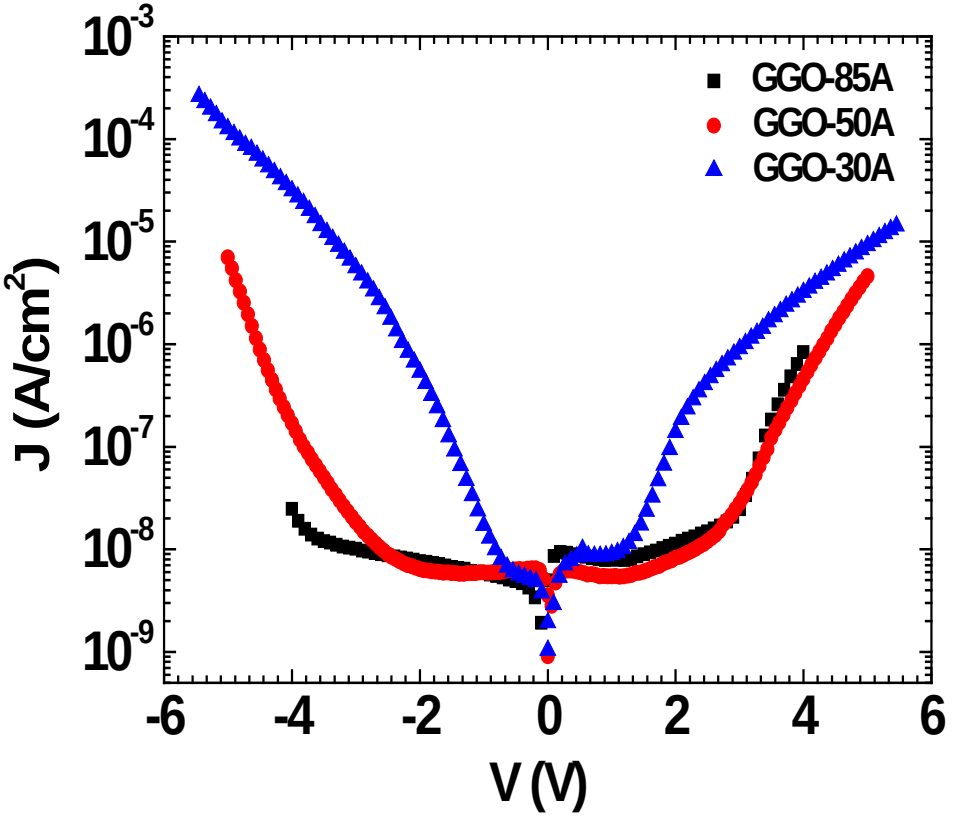


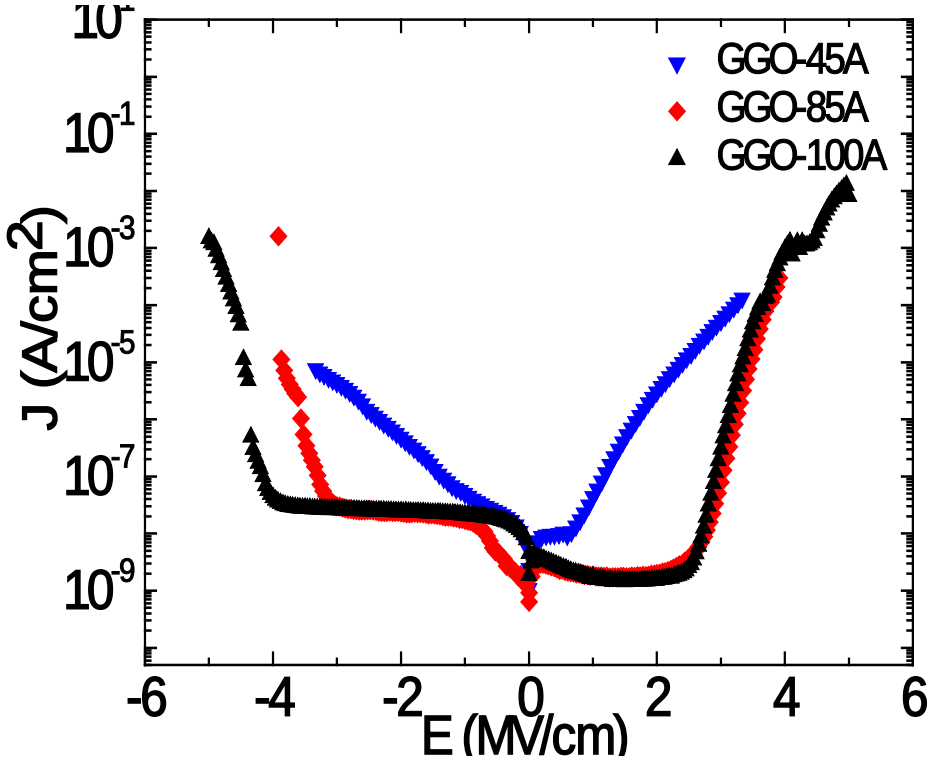






J-E Characteristics





Low leakage current density @$V_g=V_{fb}$-1V
~10^{-8}-10^{-9} A/cm^2 for various GGO thicknesses

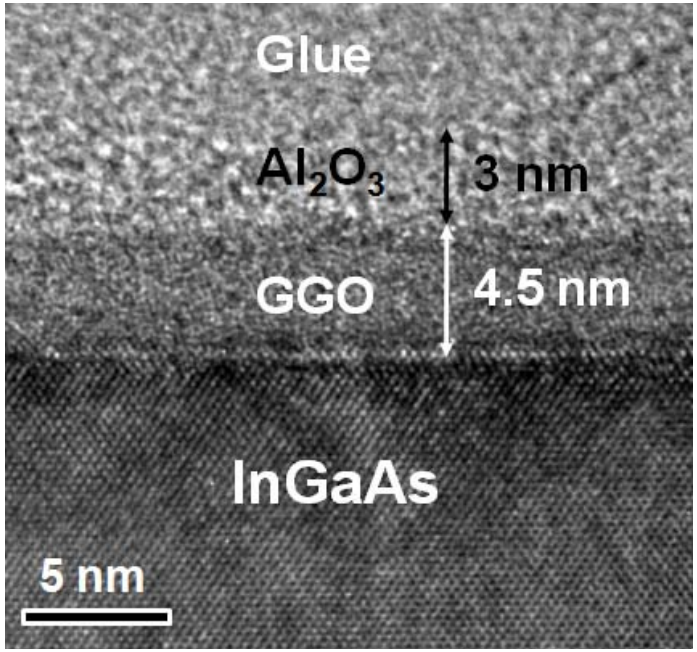
Low leakage current density @$V_g=V_{fb}$+1V
- **10^{-8}-10^{-9} A/cm^2 [GGO ≧ 8.5nm]**
- **3.1×10^{-5} A/cm^2 [GGO 4.5nm]**

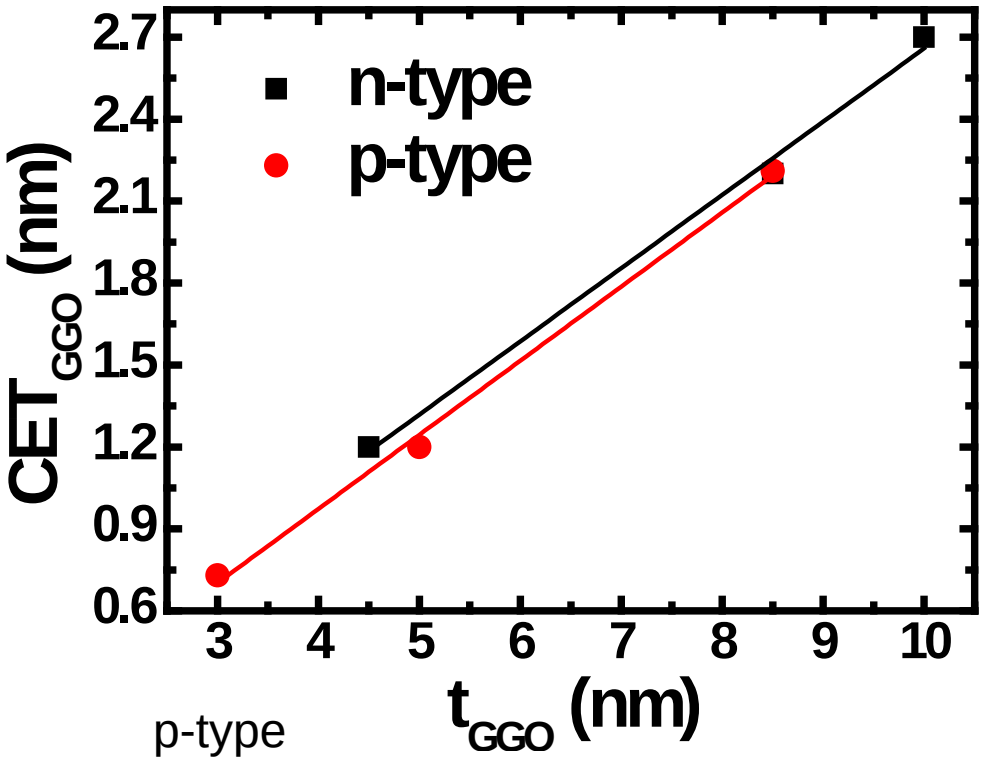
Electrical properties of Au(Ni)/Al_2O_3/GGO/$In_{0.2}Ga_{0.8}As$/GaAs

Au gate metal (N_2 800^{0}C 10 s + FG 375^{0}C 30 min with B.E(AuGe-Ni-Au))						
GGO thickness	GGO κ value	V_{fb}	Dispersion (10k-500k)	J@V_{fb}+1V (A/cm^2)	D_{it}($cm^{-2}eV^{-1}$)	GGO CET
10 nm	14-15	1.1V	2.2%	1.46×10^{-9}	1.4×10^{11}	2.7 nm
8.5 nm	14-16	1.1V	4.7%	1.78×10^{-9}	2.6×10^{11}	2.2nm
4.5 nm	14-16	1.1V	5.4%	3.1×10^{-5}	1.3×10^{11}	1.2 nm

Ni gate metal (He 850^{0}C 10 s + 3000C 30min in with B.E(TiN))						
GGO thickness	GGO κ value	V_{fb}	Dispersion (10k-500k)	J@V_{fb}+1V (A/cm^2)	D_{it}($cm^{-2}eV^{-1}$)	GGO CET
8.5 nm	14-16	-0.9V	5.71%	8.55×10^{-9}	1.1×10^{11}	2.21 nm
5nm	15-17	-0.9V	4.22%	2.9×10^{-9}	1.5×10^{11}	1.2nm
3 nm	15-17	-0.9V	6.62%	4.72×10^{-9}	1.2×10^{11}	0.73 nm

GGO scalability





n-type

t_{GGO} (nm)	10	8.5	4.5
CET_{GGO} (nm)	2.7	2.2	1.2

p-type

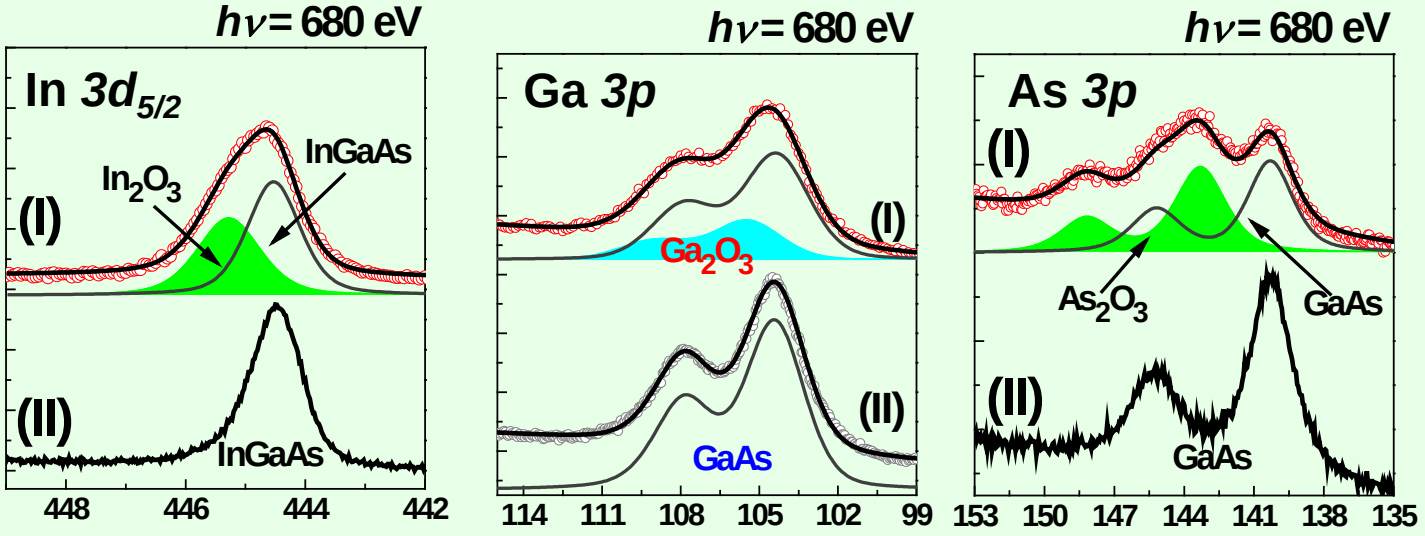
t_{GGO} (nm)	8.5	5	3
CET_{GGO} (nm)	2.21	1.2	0.73

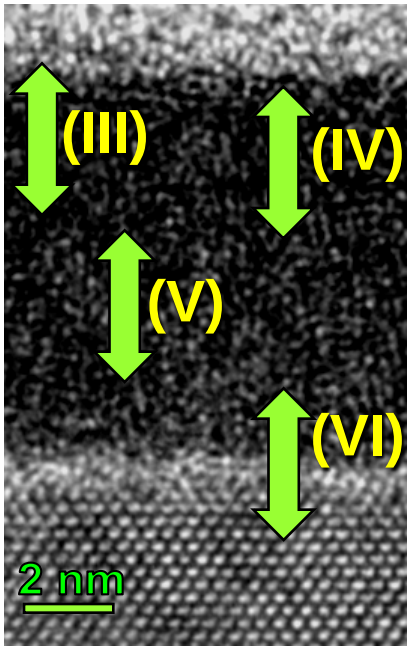
Key – high κ's/InGaAs interface

- Toward Fermi-level Unpinning and have achieved it
- GGO scalability and high-temperature thermodynamic stability of GGO/InGaAs
- Energy parameters
- MOSCAPs with different work function metals

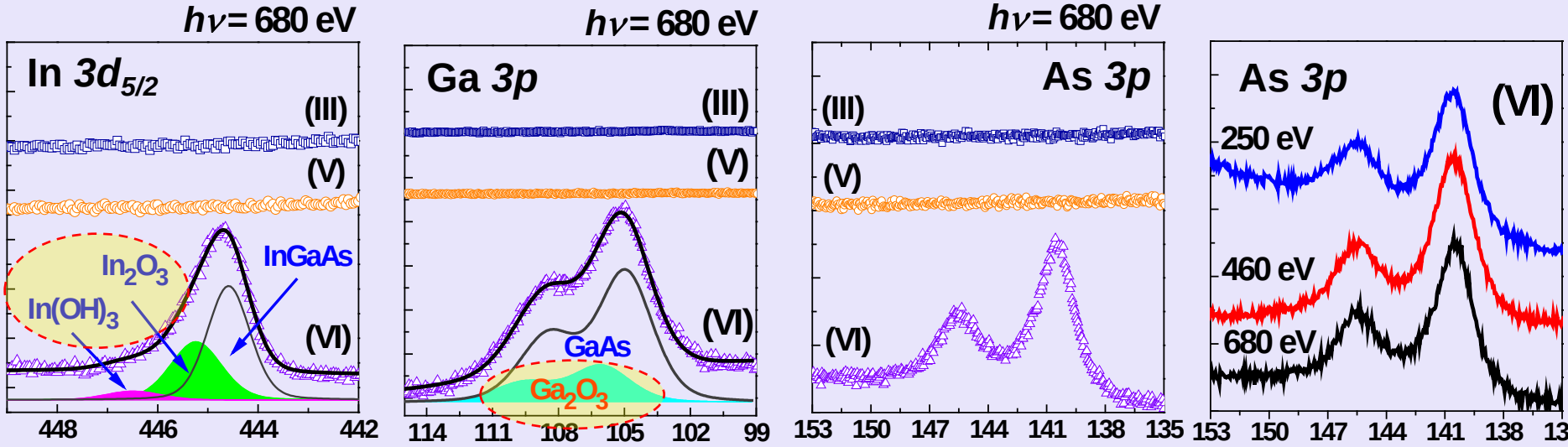
Depth profile of ALD-HfO_2/$In_{0.15}Ga_{0.85}As$: SR-XPS

Native oxide/$In_{0.15}Ga_{0.85}As$





8nm-HfO_2/$In_{0.15}Ga_{0.85}As$

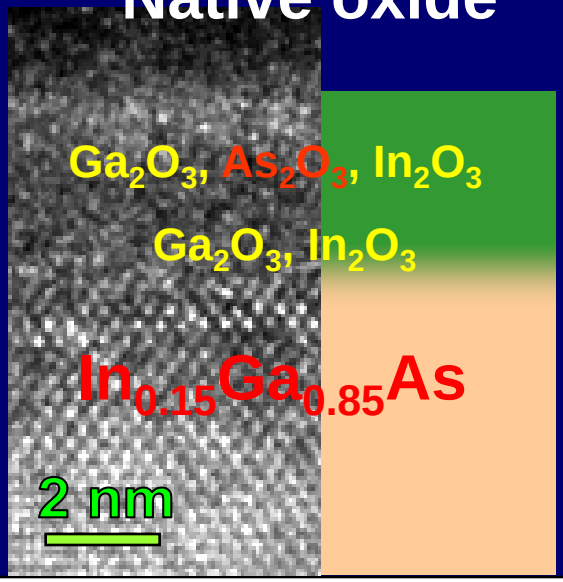


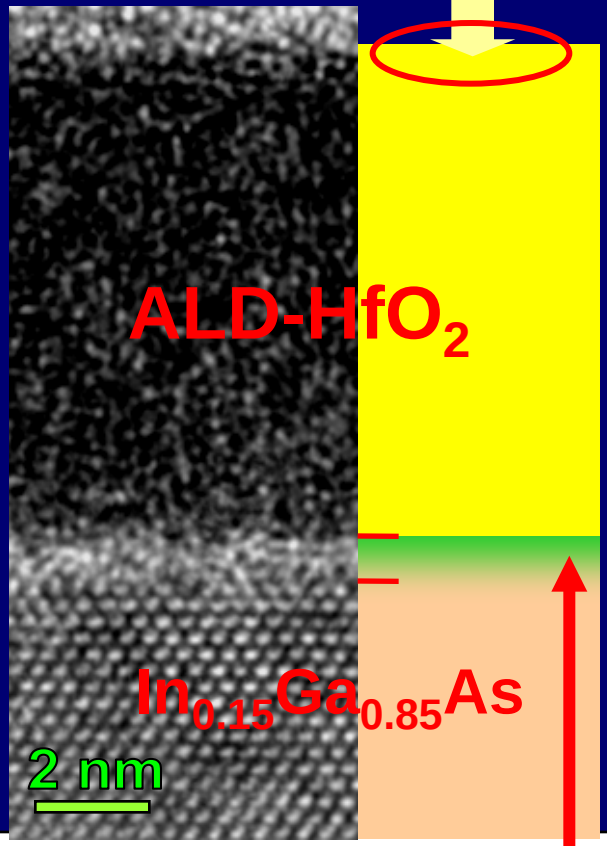
Fermi level unpinning at ALD-oxide/InGaAs

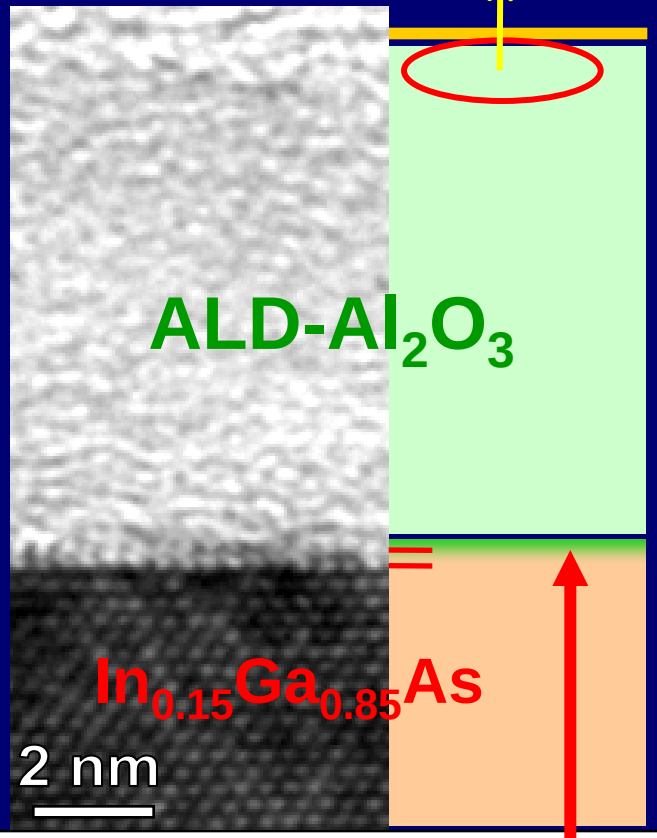
M.L.Huang, et al, APL
Dec 2005; citations:53

Different chemical reaction for TEMAH/H_2O and TMA/H_2O on air-exposed InGaAs surface

Fraction of a mono-layer As_2O_5





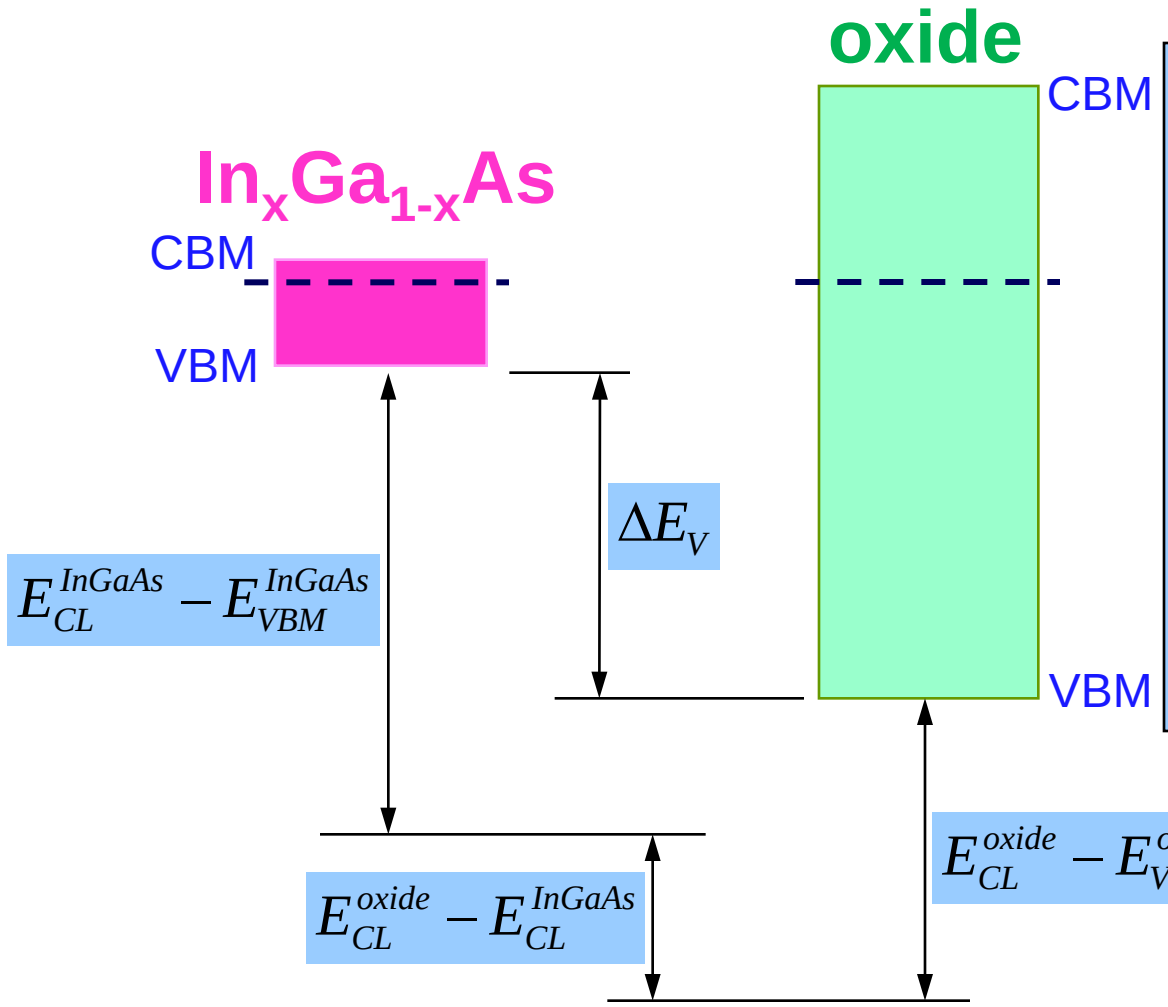


Interfacial layer: Ga_2O_3; In_2O_3; $In(OH)_3$

arsenic oxide was removed

Fermi Level unpinning

Valence band offsets: determined by XPS



E_{CL}^{InGaAs} : core level of InGaAs

E_{VBM}^{InGaAs} : valence level max of InGaAs

E_{CL}^{oxide} : core level of oxide

E_{VBM}^{oxide} : valence level maximum of oxide

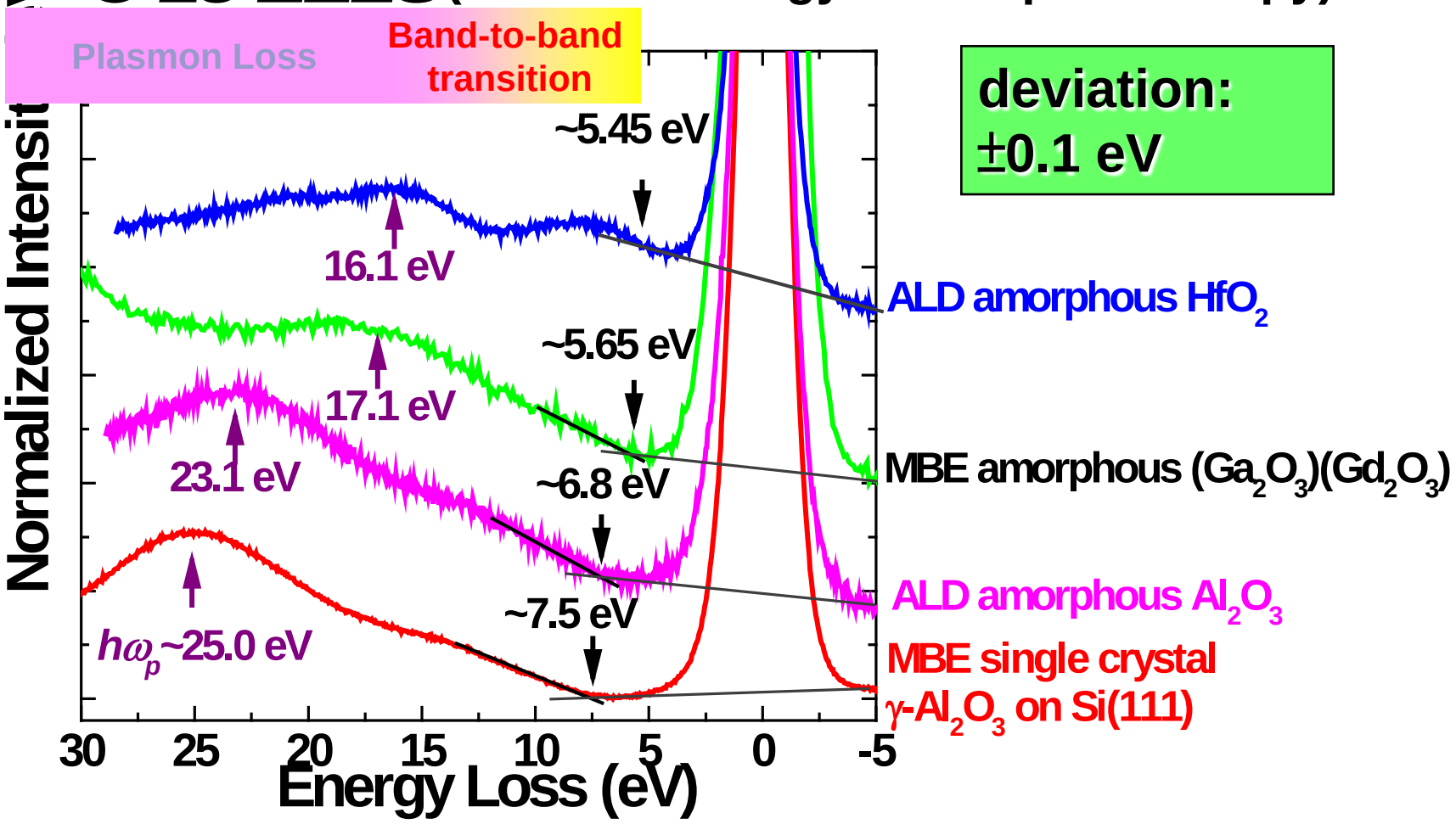
ΔE_v : Valence band offset

$$\Delta E_v = (E_{CL}^{InGaAs} - E_{VBM}^{InGaAs}) + (E_{CL}^{oxide} - E_{CL}^{InGaAs}) - (E_{CL}^{oxide} - E_{VBM}^{oxide})$$

E. A. Kraut et al., PRL 44, 1620 (1980); A. Franciosi et al., Surf. Sci. Rep. 25, 1 (1996)
M. L. Huang et al., APL 89, 012903 (2006)

Bandgap of oxide : determined by photoemission-EELS

O *1s EELS* (Electron Energy Loss Spectroscopy)

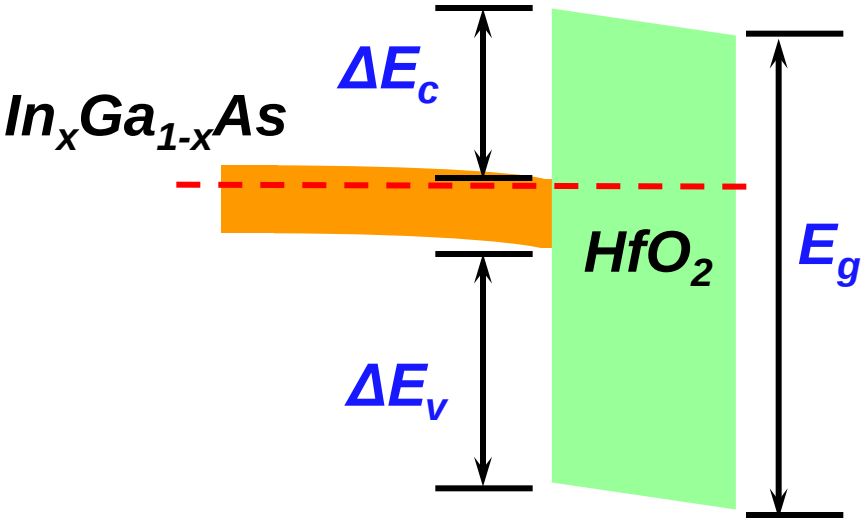


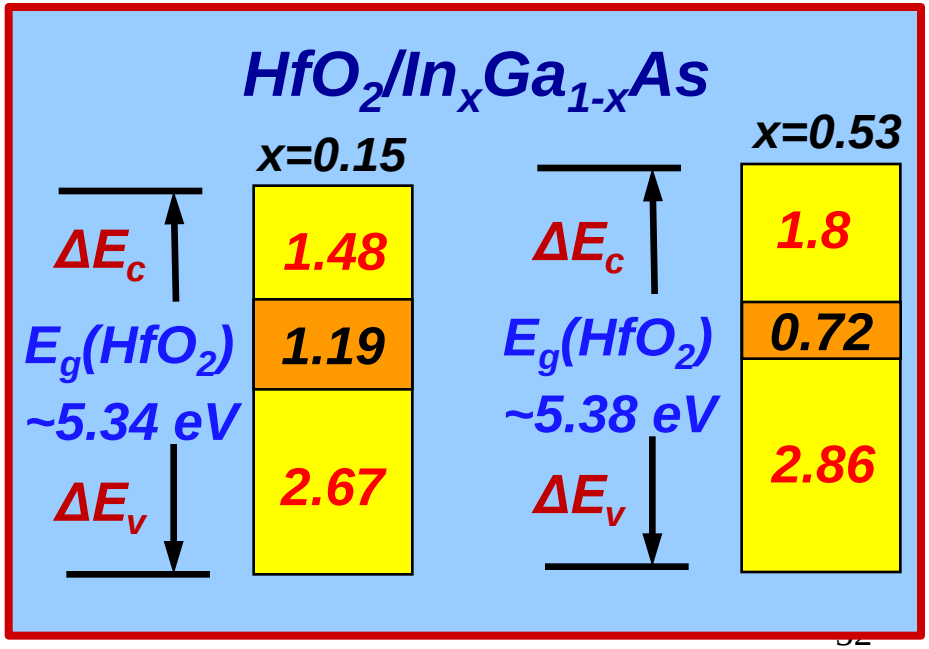
The minimum energy of band-to-band transition => Bandgap (E_g)

Energy-Band Parameters at HfO_2/InGaAs

$$\Delta E_v = (E_{CL}^{InGaAs} - E_{VBM}^{InGaAs}) + (E_{CL}^{oxide} - E_{CL}^{InGaAs}) - (E_{CL}^{oxide} - E_{VBM}^{oxide})$$

	$E_{As3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}$	$E_{Hf\,4f_{7/2}}^{oxide} - E_{As3d_{5/2}}^{InGaAs}$	$E_{Hf\,4f_{7/2}}^{oxide} - E_{VBM}^{oxide}$	ΔE_V
HfO_2/GaAs	40.36 eV	-23.58 eV	14.19 eV	2.62 eV
HfO_2/$In_{0.15}Ga_{0.85}As$	40.42 eV	-23.56 eV	14.19 eV	2.67 eV
HfO_2/$In_{0.53}Ga_{0.47}As$	40.57 eV	-23.52 eV	14.19 eV	2.86 eV





[1] M. L. Huang et al., APL 89, (2006)

Conduction band offsets: F-N tunneling

$\ln(J_{FN}/E_{ox}^2) = S/E_{ox} + \ln(C)$

$S = -8\pi(2m^*)^{1/2}(\varphi)^{3/2}/3qh$

$C = q^3/8\pi h\varphi m^*$

Φ_m: metal work function

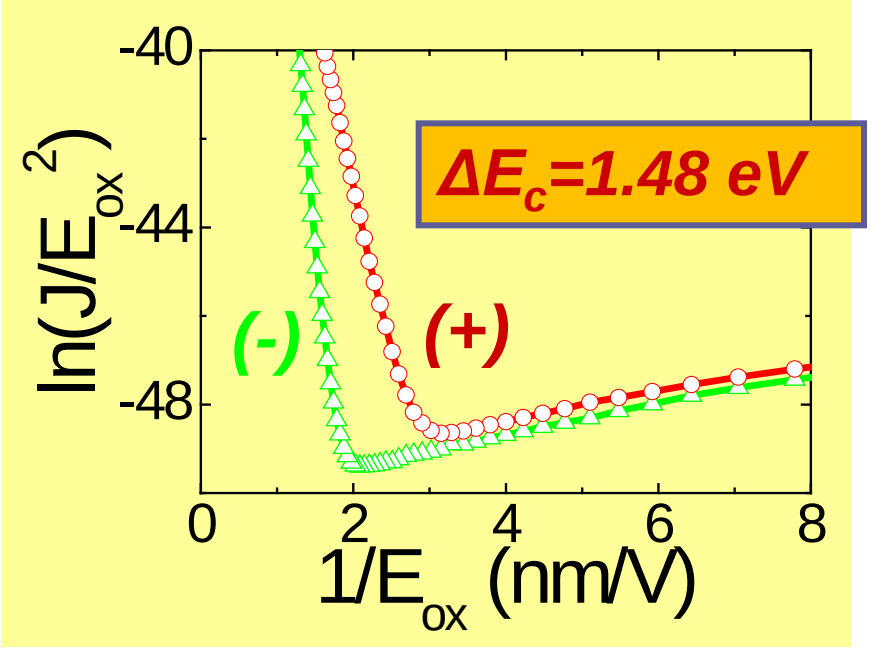
χ_s : electron affinity of InGaAs

$(\varphi^- - \varphi^+) = (\Phi_m - \chi_s)$ --- (1)

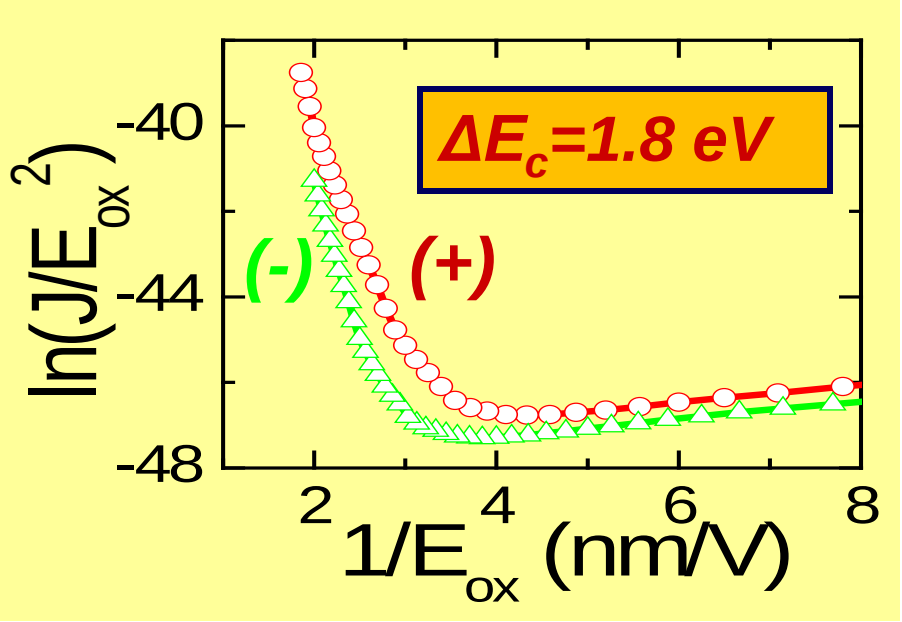
$S^+ = -8\pi(2m^*)^{1/2}(\varphi^+)^{3/2}/3qh$ --- (2)

$S^- = -8\pi(2m^*)^{1/2}(\varphi^-)^{3/2}/3qh$ --- (3)

$8.3nm\text{-}HfO_2 / In_{0.15}Ga_{0.85}As$



$7.8nm\text{-}HfO_2 / In_{0.53}Ga_{0.47}As$



deviation : ±0.08 eV

[1] T.S. Lay et al, Solid State Electron. 45, (2001)

[2] Y. C. Chang, et. al. Appl. Phys. Lett, 92, 072901 (2008).

Discussion: Energy band parameters

ALD-Al_2O_3/$In_xGa_{1-x}As$

	x=0	x=0.15	x=0.25	x=0.5
ΔE_c	1.71	1.83	1.89	2.09
$E_g(Al_2O_3)$ ~6.8 eV	1.42	1.19	1.05	0.75
ΔE_v	3.67	3.78	3.86	3.96

ALD-HfO_2/$In_xGa_{1-x}As$

	x=0	x=0.15	x=0.25	x=0.5
ΔE_c	1.41	1.59	1.66	1.84
$E_g(HfO_2)$ ~5.45 eV	1.42	1.19	1.05	0.75
ΔE_v	2.62	2.67	2.74	2.86

deviation : ±0.1 eV

ALD-Al_2O_3/$In_{0.15}Ga_{0.85}As$

$E_g(Al_2O_3)$ ~6.8 eV

ΔE_c	1.83±0.1eV	1.6 ± 0.1 eV
	1.19 eV	
ΔE_v	3.78 eV	

XPS method

FN tunneling

ALD-HfO_2/$In_{0.5}Ga_{0.5}As$

x=0.5

$E_g(HfO_2)$ ~5.45 eV

ΔE_c	1.84 ±0.1 eV	1.8 ± 0.1 eV
	0.75 eV	
ΔE_v	2.86 eV	

XPS method

FN tunneling

Conclusion

- Perfecting the best atomic-scale hetero-structures and their interfaces in high κ and high mobility semiconductors
- Probing them with the most powerful analytical tools (XPS and x-ray diffraction using synchrotron radiation, *in-situ* XPS, and HR-TEM)
- Producing novel, high-performance electronic devices ready for **beyond Si CMOS**