MOS (metal-oxide-semiconductor)

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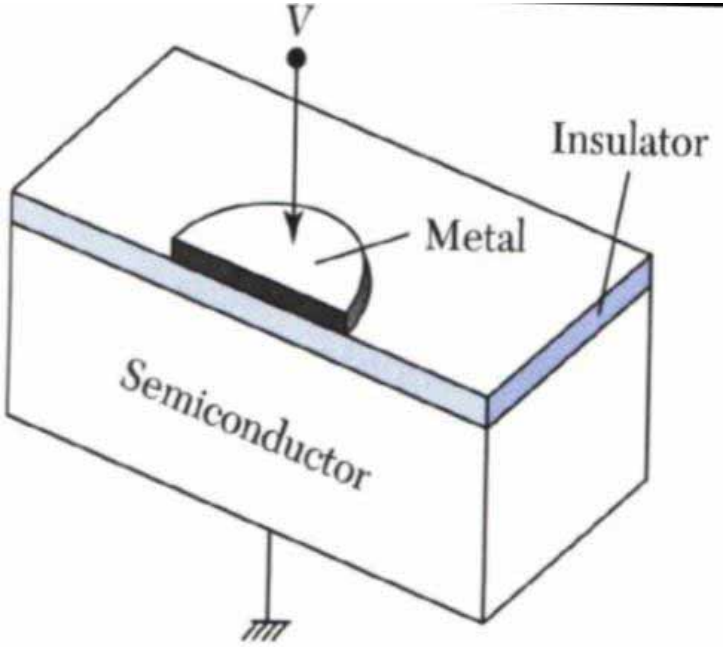
Outline

- Structure
- Ideal MOS
- The surface depletion region
- Ideal MOS curves
- The SiO_2-Si MOS diode (real case)

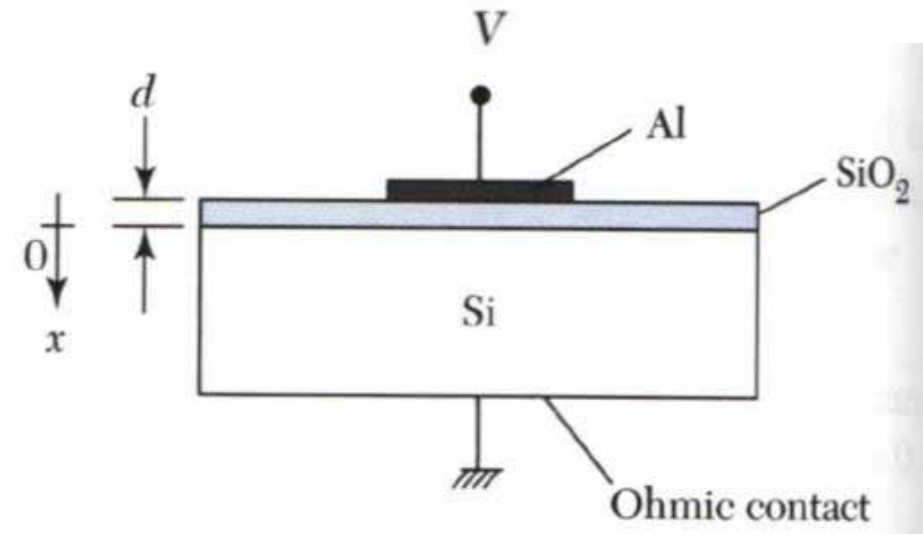
Structure



A basic MOS consisting of three layers.

The top layer is a conductive metal electrode, the middle layer is an insulator of glass or silicon dioxide, and the bottom layer is another conductive electrode made out of crystal silicon. This layer is a semiconductor whose conductivity changes with either doping or temperature.

Structure



- Cross-section of an MOS diode
- d is the thickness of the oxide and V is the applied voltage on the metal field plate
- V>(<)0 metal plate is positively (negatively) biased with respect to the ohmic contact

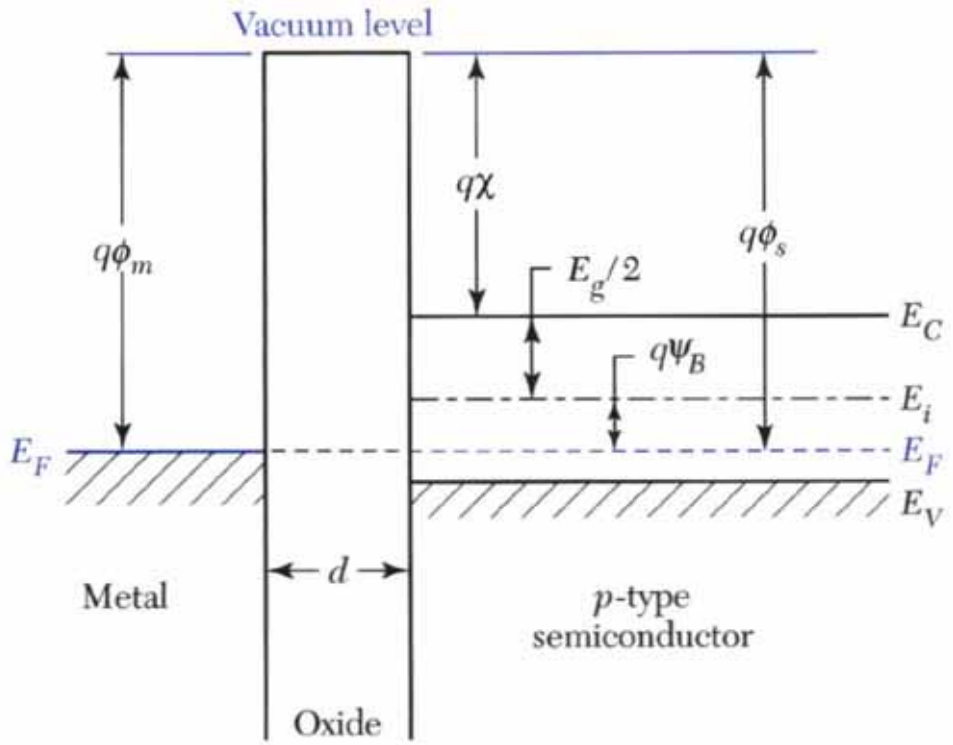
Ideal MOS

- A. at zero applied bias, the energy difference between the metal work function $q\Phi_m$ and the semiconductor work function $q\Phi_s$ is zero (in other words, the energy band is flat called flat band condition)

$$q\phi_{ms} \equiv \left(q\phi_m - q\phi_s\right) = q\phi_m - \left(q\chi + \frac{E_g}{2} + q\psi_B\right) = 0$$

- B. the only charges that exit in the diode under any biasing condition are those in the semiconductor and those with equal but opposite sign on the metal surface adjacent to the oxide
- C. there is no carrier transport through the oxide under dc biasing conditions, or the resistivity of the oxide is infinite

Ideal MOS



Energy band diagram of an ideal MOS diode at V = 0.

Ideal MOS

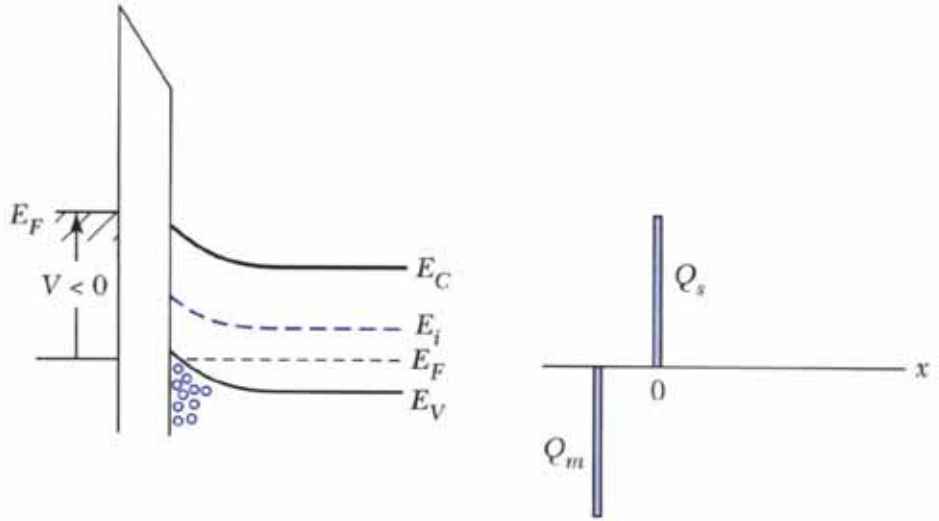
When an ideal MOS diode is biased with positive or negative voltages, three case may exist at the semiconductor surface

A. accumulation

B. depletion

C. inversion

Accumulation

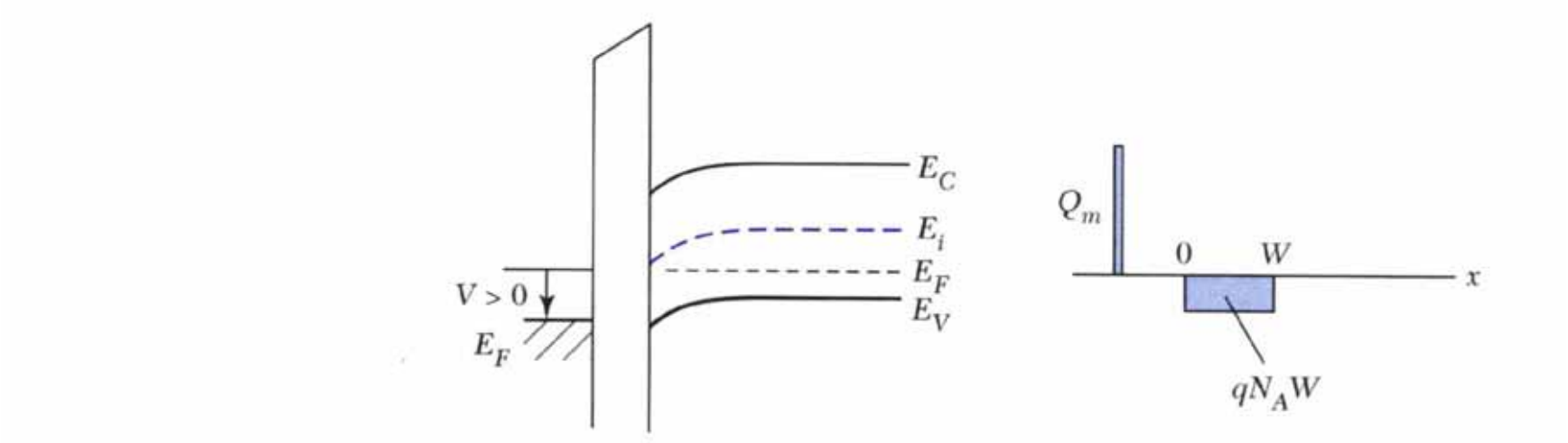


- V<0 →excess ”+” carrier will be induced at the SiO_2-Si interface
- Bands near the semiconductor surface are bent upward

$$p_p = n_i e^{(E_i - E_F)/kT}.$$

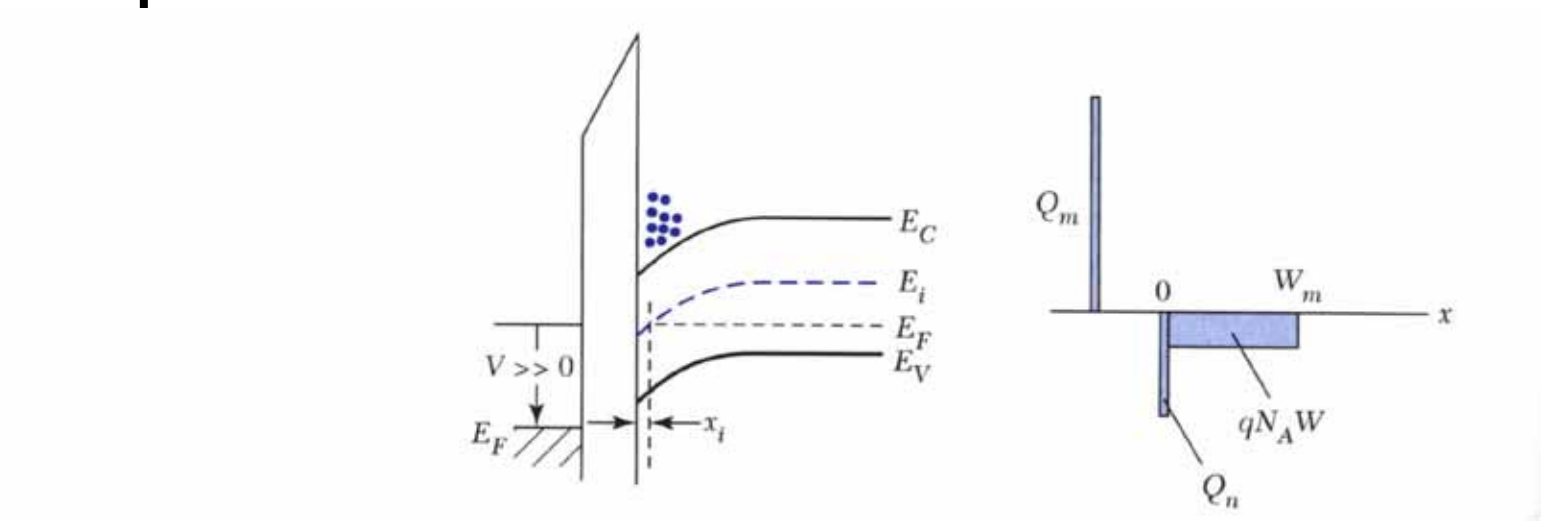
- Charge distribution Qs=lQml (Qs + charge per unit area in the semiconductor)

depletion



- V>0
- Bands near the semiconductor surface are bent downward and the major carriers (holes) are depleted
- Charge distribution Qsc=-qN_AW (space charge per unit area) W (width of depletion region)

inversion



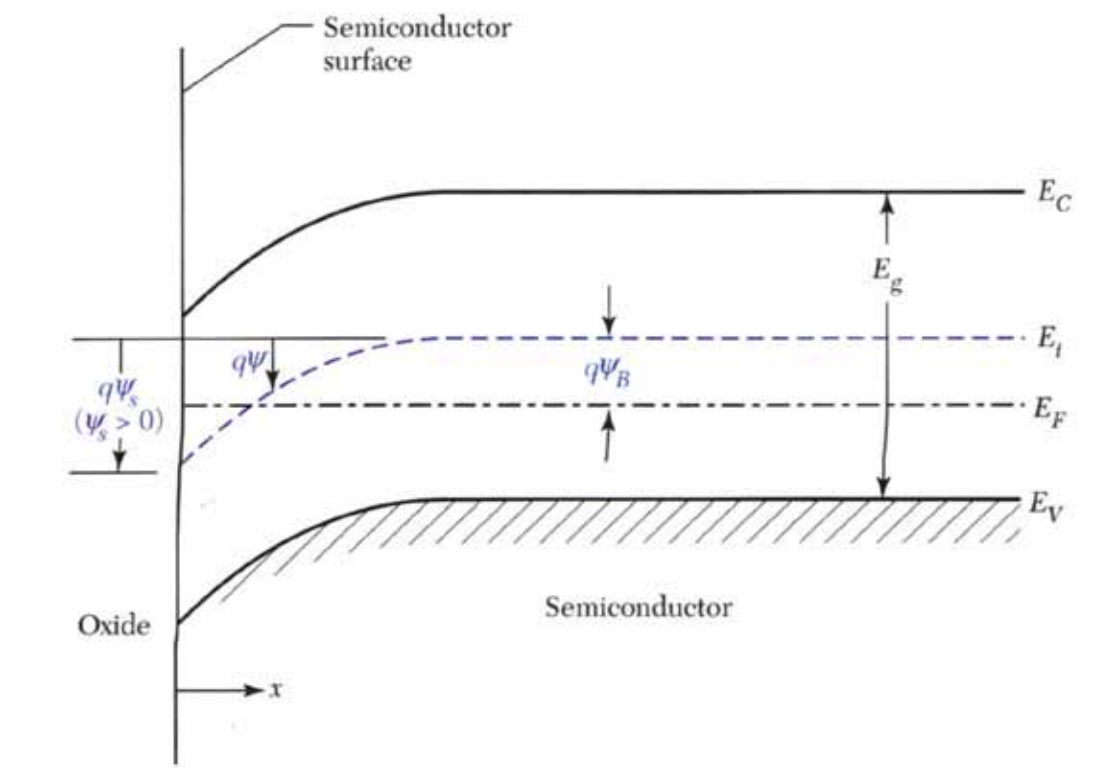
- Larger +V is applied →Ei cross over the Fermi level

$$n_p = n_i e^{(E_F - E_i)/kT}.$$

- Electrons is greater than holes
- Weak and strong inversion (electron concentration in interface equal to the substrate doping level)
- After this point additional e in the n-type inversion layer(1~10nm)

$$Q_s = Q_n + Q_{sc} = Q_n - qN_A W_m,$$

The surface depletion region



Energy band diagrams at the surface of a *p*-type semiconductor.

The surface depletion region

- We can use $q\Phi$ to replace E and get this eq

$$n_p = n_i e^{q(\psi - \psi_B)/kT},$$

$$p_p = n_i e^{q(\psi_B - \psi)/kT},$$

- At the surface

$$n_s = n_i e^{q(\psi_s - \psi_B)/kT},$$

$$p_s = n_i e^{q(\psi_B - \psi_s)/kT}.$$

The surface depletion region

$\psi_s < 0$	Accumulation of holes (bands bend upward).
$\psi_s = 0$	Flat-band condition.
$\psi_B > \psi_s > 0$	Depletion of holes (bands bend downward).
$\psi_s = \psi_B$	Midgap with $n_s = n_p = n_i$ (intrinsic concentration).
$\psi_s > \psi_B$	Inversion (bands bend downward).

Prove the depletion region width

By using the one dimensional Poisson's equation

$$\frac{d^2\psi}{dx^2} = \frac{-\rho_s(x)}{\varepsilon_s},$$

$\rho_s(x)$ is the charge density per unit volume at position x and ε_s is the dielectric permittivity

when the semiconductor is depleted to a width of W and the charge within the semiconductor is given by $\rho_s = -qN_A$ integration of Poisson's equation we get the electrostatic potential distribution as a function of distance x in the surface depletion region

$$\psi = \psi_s\left(1 - \frac{x}{W}\right)^2. \qquad \psi_s = \frac{qN_A W^2}{2\varepsilon_s}.$$

Prove the depletion region width

When strong inversion occurs $n_s=N_A$

$n_s=n_i e^{q(\Phi s-\Phi B)/kT}$ $N_A=n_i e^{q\Phi B/kT}$

$$\psi_s(inv) \cong 2\psi_B = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right).$$

From $\psi_s = \frac{qN_A W^2}{2\varepsilon_s}.$ we can get the max width of the surface depletion region W_m is $W_m = \sqrt{\frac{2\varepsilon_s\psi_s(inv)}{qN_A}} \cong \sqrt{\frac{2\varepsilon_s(2\psi_B)}{qN_A}}$

$$W_m = 2\sqrt{\frac{\varepsilon_s kT\ln\left(\frac{N_A}{n_i}\right)}{q^2 N_A}}$$

The relationship between W and N_A

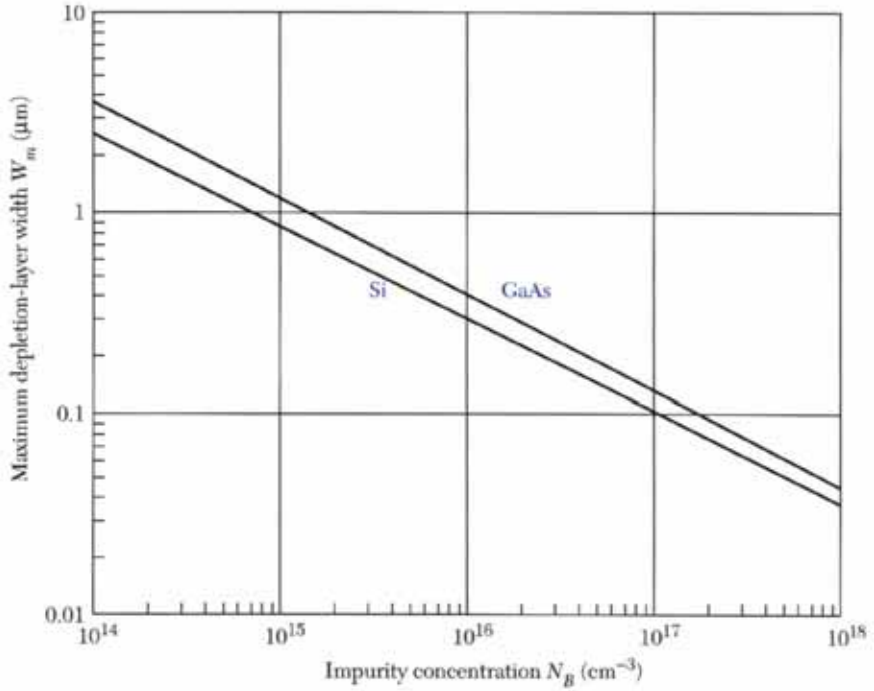


Fig. 5 Maximum depletion-layer width versus impurity concentration of Si and GaAs under strong-inversion condition.

$$W_m = \sqrt{\frac{2\varepsilon_s \psi_s(inv)}{qN_A}} \cong \sqrt{\frac{2\varepsilon_s(2\psi_B)}{qN_A}}$$

$$W_m = 2\sqrt{\frac{\varepsilon_s kT \ln\left(\frac{N_A}{n_i}\right)}{q^2 N_A}}$$

Ideal MOS curves

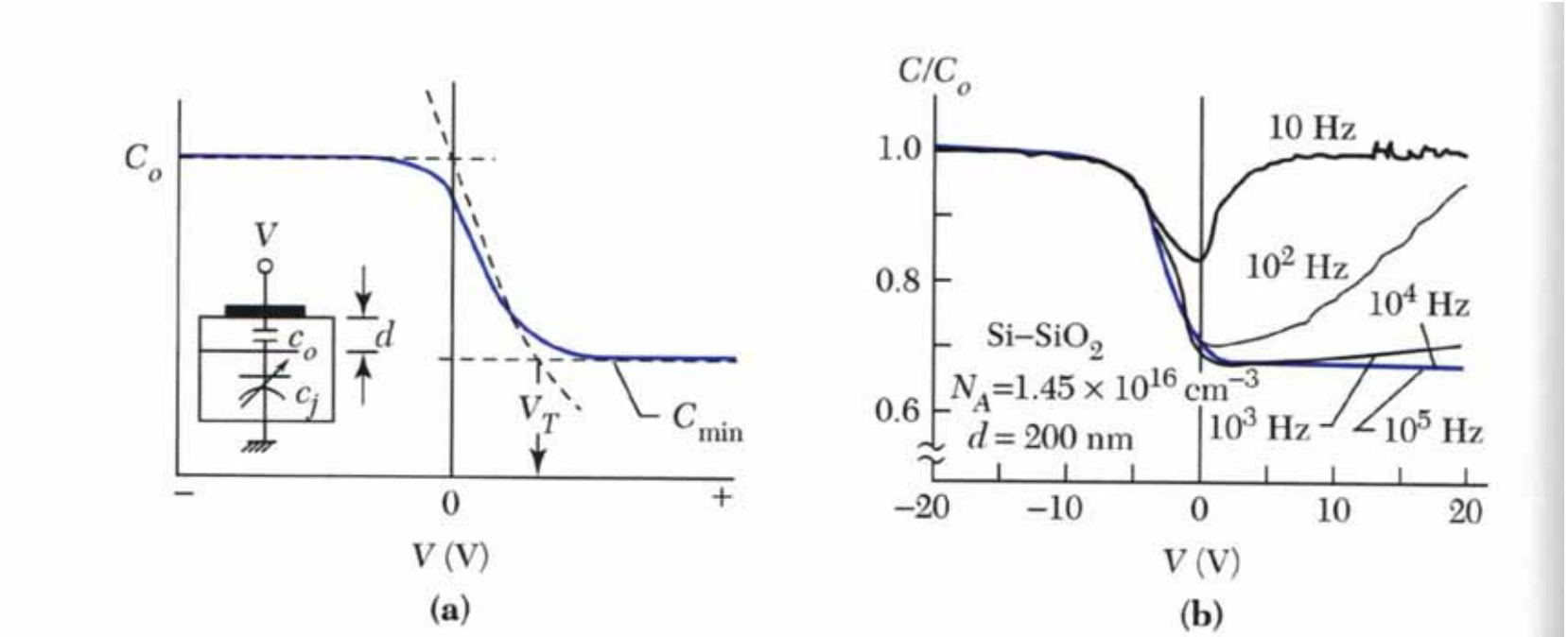


Fig. 7 (*a*) High-frequency MOS *C-V* curve showing its approximated segments (dashed lines). Inset shows the series connection of the capacitors. (*b*) Effect of frequency on the *C-V* curve.[2]

Ideal MOS curves

1.$C=C_o$

2. $$C = \frac{C_o C_j}{\left(C_o + C_j\right)} \text{ F / cm} \qquad \frac{C}{C_o} = \frac{1}{\sqrt{1 + \dfrac{2\varepsilon_{ox}^2 V}{qN_A\varepsilon_s d^2}}},$$

3.Threshold voltage

$$V_T = \frac{qN_A W_m}{C_o} + \psi_s(inv) \cong \frac{\sqrt{2\varepsilon_s qN_A(2\psi_B)}}{C_o} + 2\psi_B.$$

$$C_j = \varepsilon_s / W_m,$$

$$C_{\min} = \frac{\varepsilon_{ox}}{d + \left(\varepsilon_{ox}/\varepsilon_s\right) W_m}.$$

The SiO_2-Si MOS diode

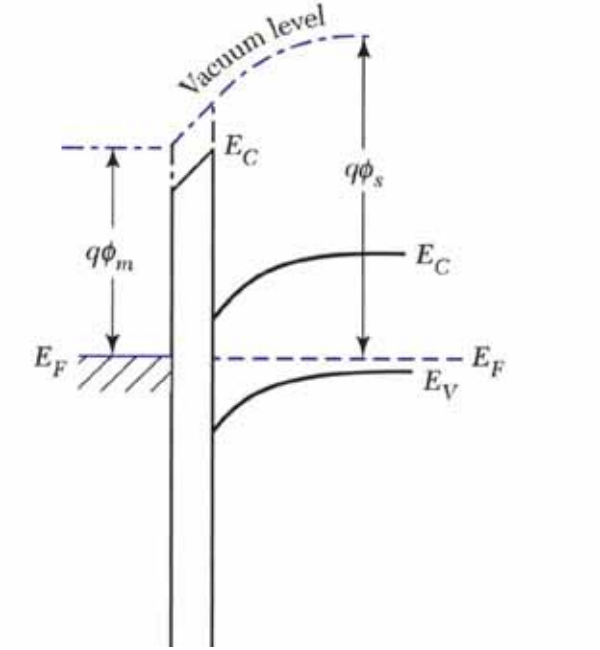
In real case there are some difference between the ideal MOS

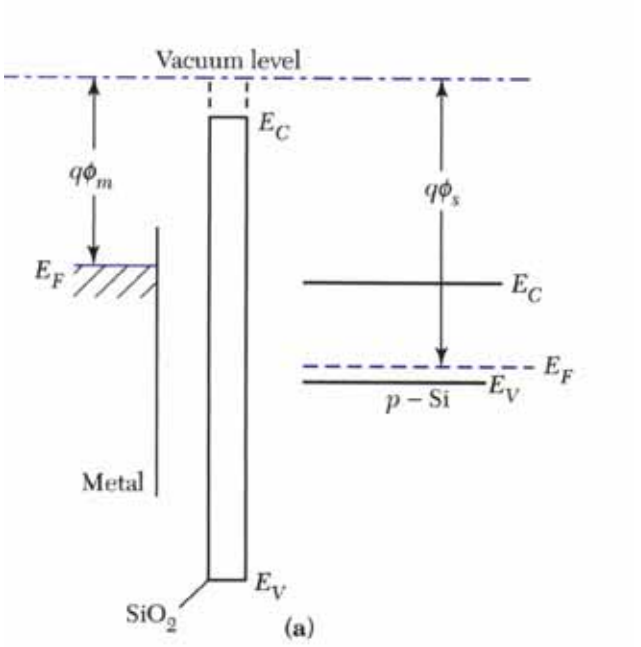
a. the work function difference

b. interface traps and oxide charges

The work function difference

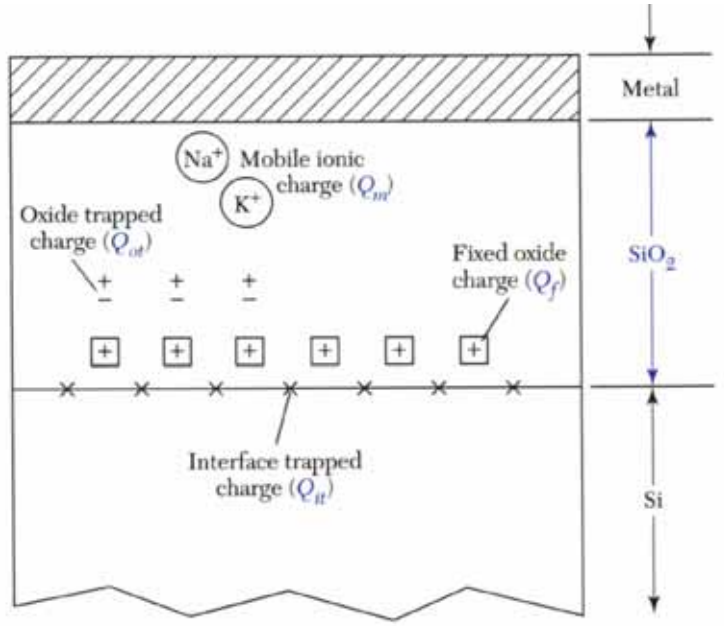
- Flat-band voltage ($V_{FB}=\Phi_{ms}$)





Interface traps and oxide charges

- Interface-trapped charge
- Fixed-oxide charge
- Oxide-trapped charge
- Mobile ionic charge



Terminology for the charges associated with thermally oxidized silicon.[3]

Interface-trapped charge Q_{it}

- It is due to the SiO_2-Si interface properties and dependent on the chemical composition of this interface
- The interface trap density is orientation dependent　for example in <100>orientation the interface trap density is about an order of magnitude smaller than that in <111>orientation
- 450℃ hydrogen annealing the value of Interface-trapped charges for <100>orientation silicon can be as low as $10^{10}cm^{-2}$

Fixed-oxide charge Q_f

- the fixed-oxide charge is located within approximately 3 nm of the SiO_2-Si interface .this charge is fixed and cannot be charged or discharged over a wide variation of surface potential. Generally, Q_f is positive and depends on oxidation and annealing conditions and on silicon orientation
- It has been suggested that when the oxidation is stopped, some ionic silicon is left near the interface. It may result in the positive interface charge Q_f
- Typical fixed-oxide charge densities for a carefully treated SiO_2-Si interface system are about $10^{10}cm^{-2}$ for a <100>surface and about $5x\ 10^{10}cm^{-2}$ for a <111>surface

Oxide-trapped charge Q_{ot}

Oxide-trapped charge are associated with defect in the silicon dioxide. These charges can be created, for example, by X-ray radiation or high – energy electron bombardment the trap are distributed inside the oxide layer. Most of process-related oxide-trapped charge can be removed by low-temperature annealing

Mobile ionic charge Q_m

- The mobile ionic charges Q_m, such as sodium or other alkali ion are mobile within the oxide under raise-temperature (e.g.>100℃) and high-electric field operation
- It may cause stability problem in device

Effect of a fixed oxide charge and interface traps on the C-V characteristics of an MOS diode