Minimizing Switching Noise in a Power Distribution Network Using External Coupled Resistive Termination

Tsun-Hsu Chang, *Member, IEEE*

***Abstract*—Switching noise-induced voltage fluctuation might result in a serious timing skew or false triggering in a high-speed digital system. We propose a new approach called external coupled resistive termination (ECRT) for suppressing this noise. Analyzing the resonant field patterns reveals that the bulk noise is accumulated close to the plane edges because of the open-end boundary condition. Thus, adding extra loading at the field bulk effectively reduces the quality factors and consequently minimizes the noise accumulation. A Y-shaped power distribution network was studied with a frequency controllable input–output (I/O) buffer model. Simulation results indicate that the noise level is significantly suppressed. The optimal noise reduction rate is 80% at resonance with an overall reduction rate of 50%. Scattered placement of the ECRT was also investigated and the corresponding noise reduction rate was 50%. Reasons for that will be discussed.**

***Index Terms*—High-speed digital system, power distribution network, printed circuit board (PCB), quality factor, resonance, simultaneous switching noise.**

I. Introduction

PRECISELY controlling timing skew is one of the major challenges in high-speed digital signaling. Among various reasons that cause timing skew, power integrity (PI) has been recently considered to be the principal concern, especially under the requirement of high data throughput and low-voltage signaling [1]. Switching noise is the dominant source in a power distribution network (PDN) [2]–[5]. Therefore, minimizing this noise can reduce timing skew and benefit signal integrity.

When the input–output (I/O) buffer is switching, not only does it draw energy from the PDN in a very short period of time, but it also induces broad-band noise in the PDN. The noise level is exacerbated even further when multiple signals transition at the same time, called simultaneously switching noise (SSN) [2]. The high-frequency noise signals are basically in phase or nearly in phase resulting in their addition. If designed improperly, a pair of power-ground planes form a resonator, then the noise with the frequency close to the resonance could be accumulated, causing more severe PI problems.

The most widely used means of noise-suppressing is to place decoupling/bypass capacitors close to the I/O buffer(s). However, the existence of equivalent series inductance (ESL) of the lead limits its application to the high-frequency regime [3]. Besides, the decoupling capacitor and its ESL form a circuit which will store noise energy at resonance [6]. Since the switching noise is deteriorated at resonance, lowering the resonant effect can effectively alleviate the noise accumulation. Resonance can be avoided by either staggering the resonant frequency from the noise frequency [1] or adding more loss to reduce the quality factor [7]–[11]. The latter approach is considered herein.

Fig. 1 schematically depicts a power distribution network. The voltage of the I/O buffer is provided with a dc power supply on a main-board/mother-board, through the shortest current loop on the power plane and connecting vias, which eventually lead in to the I/O buffer on chip. Normally, decoupling capacitors are employed to compensate for the deficiency of the voltage supply and reduce the switching noise due to plane inductance. Plane and via inductance excites the noise in the PDN during switching, while decoupling capacitors alleviate this induced noise by shortening the effective current loop.

Using the absorption/lossy materials (electric and magnetic) to suppress noise has been proposed, called the edge termination [7]–[9]. The absorption material, commonly applied at the circuit board edge, can effectively minimize the reflection and radiation from the edge discontinuity particularly in the high-frequency regime. However, in the type of the electric loss, leakage current was reported, while in the magnetic loss condition, a broad-band absorption material is still unavailable. Recently, a novel printed circuit board (PCB) stackup with thin laminated dielectric layer was proposed [10], [11]. It exhibits good suppression of plane resonance by providing a loss scheme for high-frequency noise. In addition, the thin laminated PCB can minimize the plane inductance of a current loop and, thus, significantly reduce the switching noise. Although various solutions have been proposed, less study has attempted to alleviate the noise by coupling it to the external loading.

The objective of this study is to provide an approach to minimizing the noise within a PDN by coupling out the noise and converting it into the dissipative heat. Section II delineates the simulation setup and the I/O buffer modeling. Section III explains how the external coupled resistive termination (ECRT) works from the frequency-domain perspective. The quality-factor reduction mechanism is to be explained. Section IV discusses three results: the improvement of the power integrity; the position dependent effect; and the placement of ECRT. Finally, concluding remarks are made in Section V.

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The author was with the Silicon Integrated System Corporation (SiS), Hsinchu, 300 Taiwan, R.O.C. He is now with the Department of Physics, National Tsing Hua University, Hsinchu, 30013 Taiwan, R.O.C. (e-mail: thschang@ phys.nthu.edu.tw).

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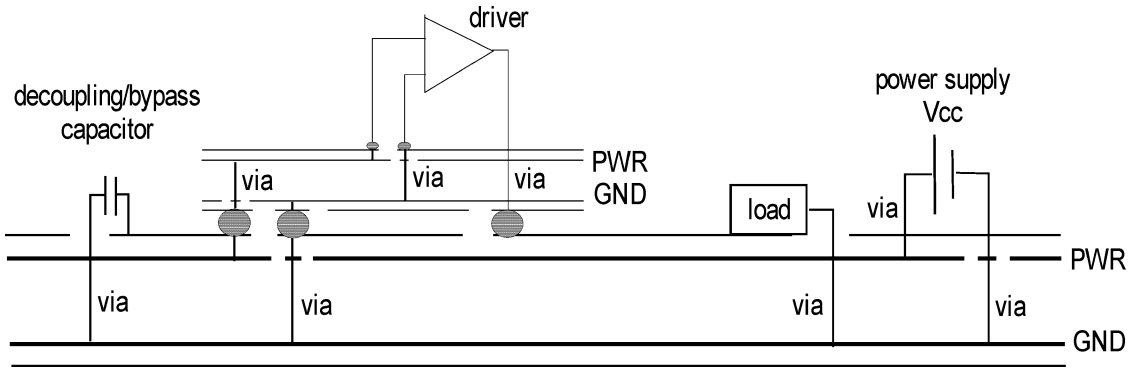

Fig. 1. Schematic diagram of the power distribution network. The I/O buffer draws its energy from a far-end power supply. The decoupling capacitor in the vicinity of the driver shortens the effective power delivery loop and compensates the voltage drop during transition.

TABLE I
STACKUP AND CIRCUIT ILLUSTRATION UNDER STUDY. THE SWITCHING NOISE IS STORED IN THE POWER (L2) AND GROUND (L3) PLANES. THE ECRT CIRCUIT EXTRACTS THE SWITCHING NOISE AND DUMPS IT ONTO A TERMINATION RESISTOR. THE RESISTIVITY OF THE DETECTING CIRCUIT IS HIGH TO PREVENT INTERFERENCE WITH THE VOLTAGE SUPPLY. ONLY THE RELEVANT CIRCUITS ARE SHOWN IN THE TABLE

Layer	Thickness (mil)	Material	Circuit illustration
L1 (Signal 1)	1.4	metal: copper	Driver, D*
D1 (FR4)	4.0	dielectric: FR4	
L2 (PWR)	1.4	metal: copper	
D2 (core, FR4)	44.0	dielectric: FR4	Detecting circuit, P*
L3 (GND)	1.4	metal: copper	
D1 (FR4)	4.0	dielectric: FR4	ECRT circuit, E*
L4 (Signal 2)	1.4	metal: copper	

II. SIMULATION SETUP AND I/O BUFFER MODELING

The PDN of a multilayer PCB normally comprises power and ground planes, involving a complex electromagnetic field distribution. Hence, a field solver is very useful. Moreover, a circuit solver is necessary to properly model the I/O buffers and the lumped circuit. Therefore, Speed2000 was chosen to serve as our principal simulator.[1] The RF-field distribution and resonant effect is supplemented with a widely accepted full-wave solver, HFSS.[2]

The power/ground layout in the application of a multilayer PCB is usually manifold and adaptable. Extracting characteristics and establishing guidelines are useful to the designer and the layout engineer. A Y-shape power corridor is commonly employed in the SiS (Silicon Integrated System Corporation) chipsets. Thus, this study uses such shape as a starting point.

Table I shows the stackup and illustration of the circuit under study. The voltage fluctuation (or noise) is detected without interfering with the power delivery system. The I/O buffer drives the output signal along the trace referenced to the ground plane on the second layer. Likewise, the passive ECRT circuit leads the ac noise out of the power/ground resonator and terminates it with the external resistor. All the traces are well terminated, except the ECRT circuit, to elude the influence of multiple reflections. This table presents only the relevant circuits.

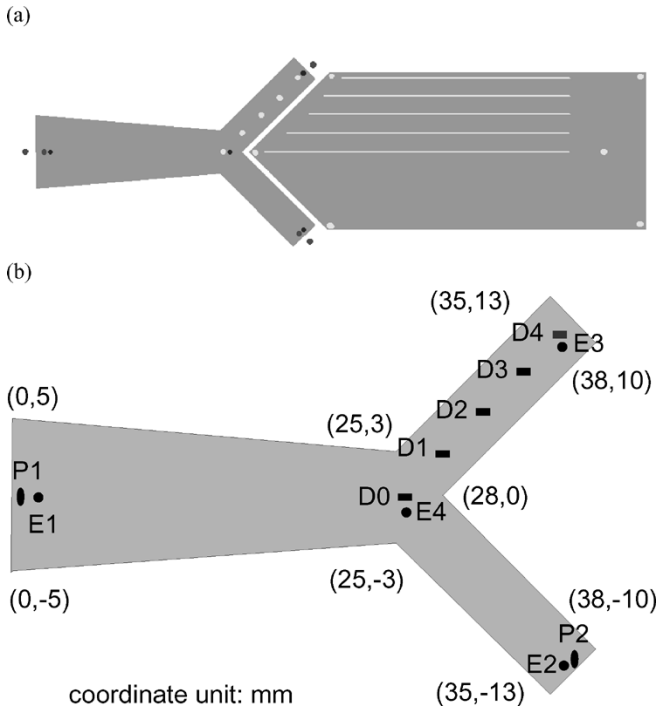

Fig. 2. (a) Top view of the second layer (L2), showing the power plane (Y-shaped) and the ground plane (pentagon). The traces and connecting pads on the Signal 1 layer are also projected. The third layer (L3) is a ground plane. (b) Position of the I/O buffers (denoted by D0 to D4), the detecting points (P1 to P2), and the external coupled resistive termination (ECRT) circuits (E1 to E4). The coordinates are in millimeters.

Fig. 2(a) shows the top view of the power plane (Y-shape) and the ground plane (pentagon). The traces and connecting pads on Signal 1 (upper layer) are also projected onto it. The third layer (L3) is a ground plane. Fig. 2(b) depicts the position of the I/O buffers (denoted by D0 to D4), the detecting points (P1 and P2), and the external-coupled resistive termination circuits (E1 to E4). The dimensions of the Y-shape layout are marked on each corner point with a pair of numbers to specify the corresponding abscissa and ordinate. Interestingly, like-planes (such as the ground–ground or the power–power plane) can still form a resonator that stores electromagnetic noise. However, due to the

[1]PowerSI and Speed2000, Sigrity Corporation http://www.sigrity.com/

[2]HFSS, Ansoft Corporation http://www.ansoft.com/

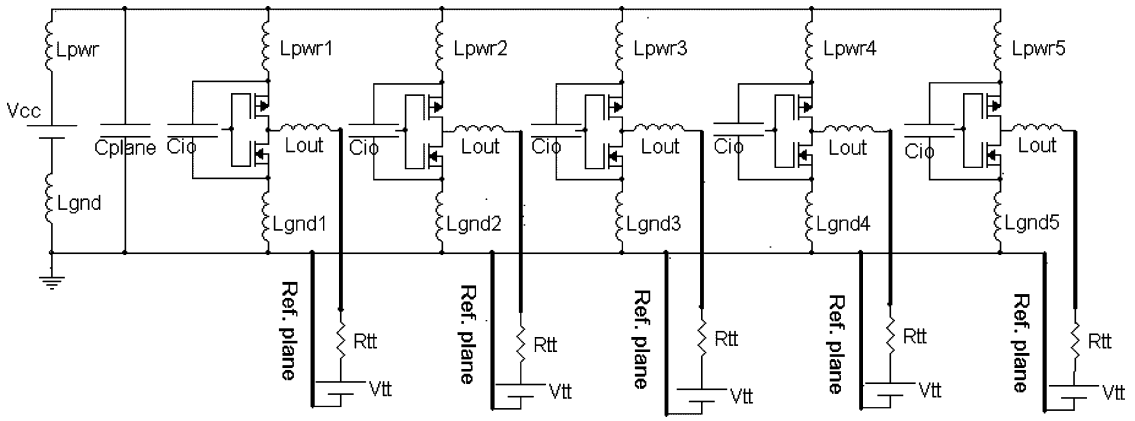

Fig. 3. Equivalent SPICE model of five CMOS buffers. A VCR model is employed to represent the CMOS to study the frequency response. This illustration is used to clarify how the I/O buffer is modeled.

lack of a considerable noise source, noise cannot effectively accumulate in homo-planes. Consequently, only the voltage fluctuation of the hetero-planes is studied in this paper.

A voltage-controlled resistor (VCR) buffer model is preferable for studying the frequency response of the PDN. For the linear-behavior model (or piecewise VCR), the impedance during the switching interval is dynamic, meaning that it varies with time. This linear-behavior model (piecewise linear VCR) is taken from the behavior of a SiS 648 chipset. The resistivity is controlled with an internal trigger signal. The waveform of this signal is trapezoidal with the rise/fall time of 200 ps. Increasing the operating frequency reduces the period (T: ps) and the flattop time becomes T/2-200 ps.

Fig. 3 shows the equivalent model of the CMOS buffer. The responses of the p-MOS and n-MOS can be replaced with a VCR model extracted from the I/O buffer information specification.[3] The rising/falling waveform can be derived accordingly. A capacitance (Cio) of 20 pF is assumed in this simulation. The effective parallel plane capacitor (Cplane) is considered, and decoupling capacitor is not used. The power/ground inductance (denoted as Lpwr* and Lgnd*) is position-dependent and declines as the voltage supply source moves closer to the pin of the I/O buffer. This SPICE model is presented just to give the reader an idea of how the I/O buffer is modeled. It is not further explored.

III. External-Coupled Resistive Termination

Fig. 4(a) presents the physical structure of the ECRT. A metal post is placed between the power and the ground planes. The upper end of the metal post is not in contact with the power plane but is normally as close as possible. The lower end is connected to the ground plane through a termination resistor. Fig. 4(b) shows the effective circuit. When dc is applied, the opened circuit does not compromise the dc power supply. At high-frequency, the entire structure functions as a high-pass filter. The unwanted noise is coupled out to the external circuit and is terminated with a resistor. A similar concept used to excite the waveguides could be found in [12] and [13]. In practice, the whole ECRT circuit can be readied using the existing via plus a termination resistor.

[3]I/O Buffer Information Specification. http://www.eigroup.org/ibis/

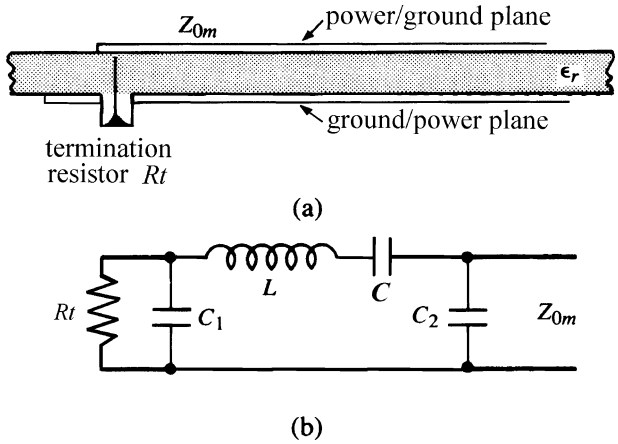

Fig. 4. (a) Structure and (b) the equivalent circuit of the ECRT under study. The central post is not in physical contact with the other hetero plane. Therefore, it does not affect the dc voltage, but damps RF noise as can be seen in the equivalent circuit. In practice, the whole ECRT circuit is made ready using the existing via plus a termination resistor.

The quality factor of a resonant system specifies the strength of the resonant effect and the effective bandwidth. Minimizing the quality factor effectively alleviates the resonant effect. The quality factor of a resonator is inversely proportional to the power dissipation. The unloaded quality factor Q_U of a microstrip resonator can be expressed as follows:

$$Q_U = \frac{2\omega W_e}{P_d + P_c} \tag{1}$$

where ω is the resonant frequency, W_e is the total electric field energy, and P_d and P_c are dielectric and conductor power loss, respectively. For a resonant frequency of a few hundred megahertz, the dominant loss mechanism is conductor loss. However, this intrinsic loss is not sufficient to yield a sufficiently low quality factor. Therefore, an extra loss mechanism must be provided. It can be achieved by applying some ECRTs functioning as probes to extract the noise. The loaded quality factor Q_L becomes

$$Q_L = \frac{2\omega W_e}{P_d + P_c + P_e} = \left(\frac{P_d + P_c}{P_d + P_c + P_e}\right) Q_U \tag{2}$$

where P_e is the external power loss due to ECRT.

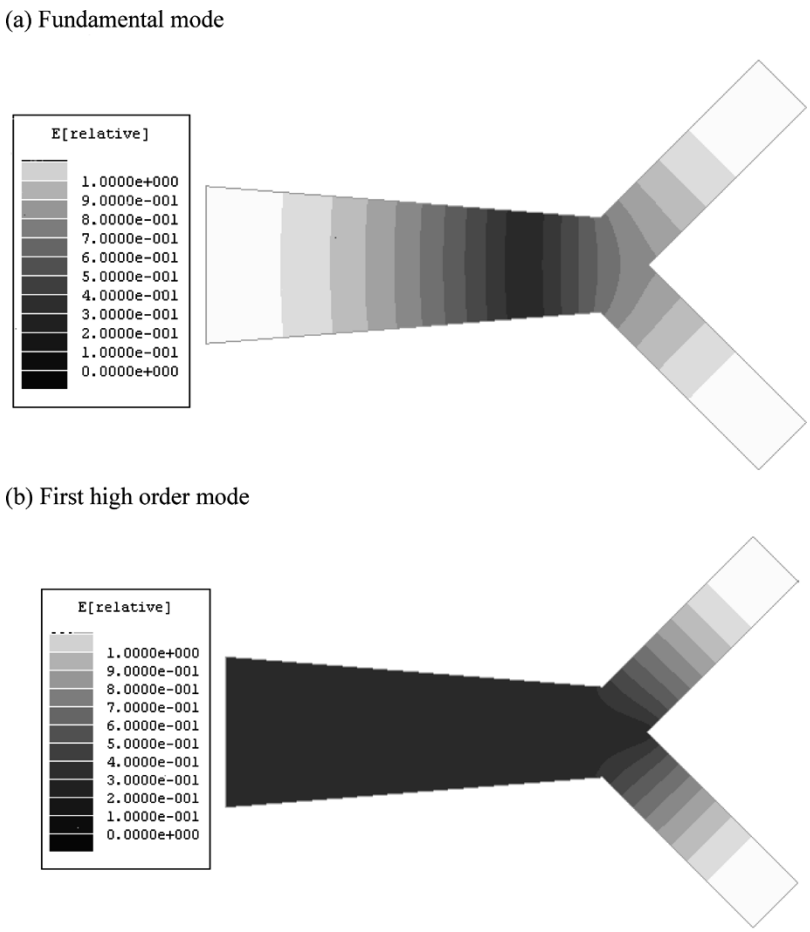

Fig. 5. Normalized electric field patterns of the first two resonant modes under study obtained using HFSS. (a) Fundamental mode and (b) first high-order mode. The electric fields of the two wings in the fundamental mode are in phase, while in the first high-order mode, they are out of phase, and the central stem is not excited.

To study the noise distribution pattern and to find out the optimal position of placing the ECRT, a bare-board with a pair of power and ground planes was investigated using HFSS. Fig. 5(a) and (b) displays the electric field patterns of the first two resonant modes. The fundamental mode [Fig. 5(a), in which the lowest resonant frequency is 1.632 GHz] has field maxima at the end of the central stem and the tips of the two wings. The field variations at the two wings are in phase. However, in the first high-order mode [Fig. 5(b), in which the resonant frequency is 2.347 GHz], the field variation at the two wings are completely out of phase, resulting in field cancellation at the central stem. The characteristics of the unique field patterns will be further explored in Figs. 6 and 7.

The loaded and unloaded quality factors are related as follows:

$$Q_L = \frac{1}{1+K} Q_U \tag{3}$$

where K is the coupling parameter, defined as $K = P_e/(P_d + P_c)$, which is related to the reflection coefficient. A higher coupling coefficient K corresponds to a better quality factor reduction. In this simulation, no attempt has been made to optimize the external impedance (including the coaxial section impedance as well as termination resistivity).

Fig. 6 plots the reflection coefficient versus the operating frequency given various external loading configurations. The resonant effect is clearly demonstrated so the quality factor can be derived. Fig. 6(a) shows the results of probing at P1 with P2 disabled. The first high-order mode does not exhibit any resonant effect because the fields are zero at the central stem. The noise pattern in the fundamental mode has its field maxima at both wings (E2 and E3) and at the central corridor (E1), but a relatively low field close to the center (E4). The fields at both wings are in phase and have equal amplitude, so E2 and E3 have the same effect. Therefore, the figure presents only E1, E2, and E4. When E2 is employed, the quality factor reduction is much larger than that obtained when E1 and E4 are used. E1 and E4 are less effective than E2 because the fields in the former regimes are relatively diverse. The highest quality factor is obtained without an ECRT, and the lowest quality factor is obtained with all ECRTs, as expected.

Fig. 6(b) present the results of probing at P2 with P1 disabled. Resonant effects are observed in both modes. The first high-order mode can be clearly detected at P2, due to the intrinsic field distribution. The variation in the quality factor in the first high-order mode exhibits the same trend as that in the fundamental mode, i.e., placing the external load (ECRT) at the field maximum significantly reduces the quality factor. This generic property suggests that coupling out the noise at the field maximum of a target mode will be advantageous.

Speed2000 is not a full-wave solver and is subject to some theoretical constraints. Therefore, HFSS was used to simulate the resonant effect. The ECRT is now modeled as a coaxial

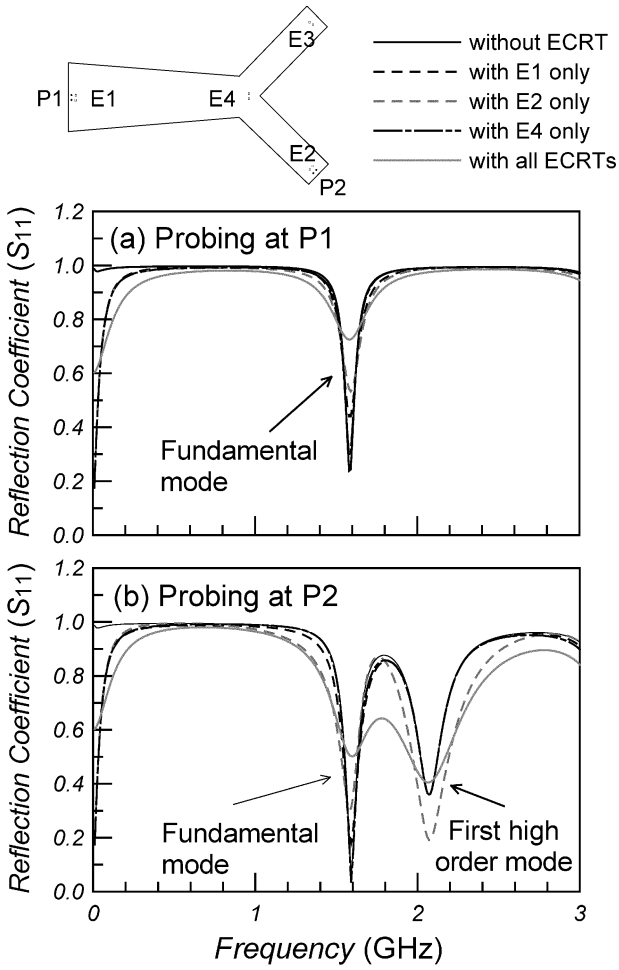

Fig. 6. Speed2000 simulation results concerning the reflection coefficient (a) when probes at P1 with P2 disabled and (b) when probes at P2 with P1 disabled, given various ECRT configurations. In both modes, as expected, with no ECRT, the quality factors are highest, whereas with all ECRTs present, the quality factors are lowest.

waveguide port with inner and outer radii of 0.4 and 1.0 mm, respectively. The characteristic impedance of the coaxial waveguide is not optimized. Fig. 7 shows the simulation results: the Q-factors of the first two modes are reduced from 51.4 (without ECRTs) to 23.6 (with all ECRTs) and from 52.1 to 15.2, respectively. Notably, placing the ECRT affects the resonant frequencies. Figs. 6 and 7 are calculated under different conditions, and so can not be directly compared, but they basically reveal that ECRTs effectively reduce the quality factor. Therefore, Speed2000 can still be used to demonstrate the effect of noise suppression associated with the decline in the Q-factors, although the resonant frequencies are shifted.

IV. Results and Discussion

The single I/O buffer and then multiple I/O buffers were investigated with different placement of ECRTs to deal with the problem systematically. The variation of the noise voltage fluctuation with the probing position is demonstrated and examined. Finally, two ECRT configurations are made to explore the placement effect. A long simulation duration of 30 ns is used. However, only the worse noise fluctuation value, corresponding to a particular operating frequency, is recorded and analyzed.

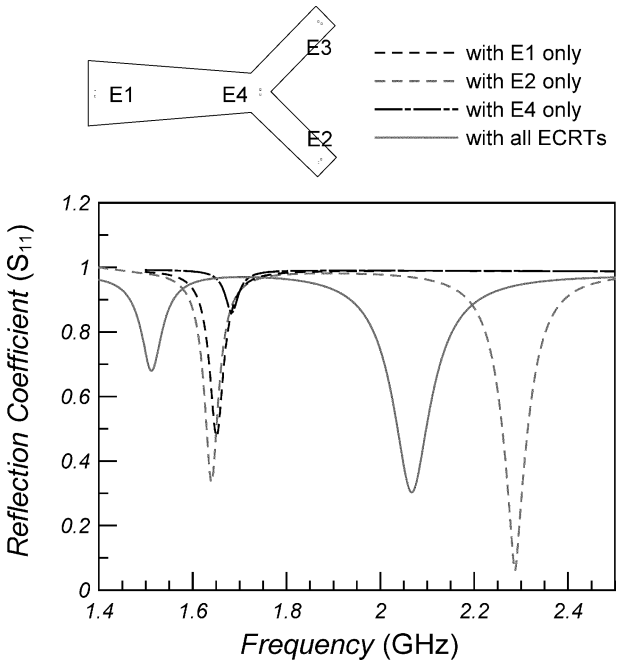

Fig. 7. HFSS simulation results; the reflection coefficients are obtained by treating each ECRT circuit as a coaxial port. Placing the ECRT close to the field bulk affects the resonant frequency and lowers the quality factor. The characteristic impedance of the coaxial port of the ECRT is not optimized.

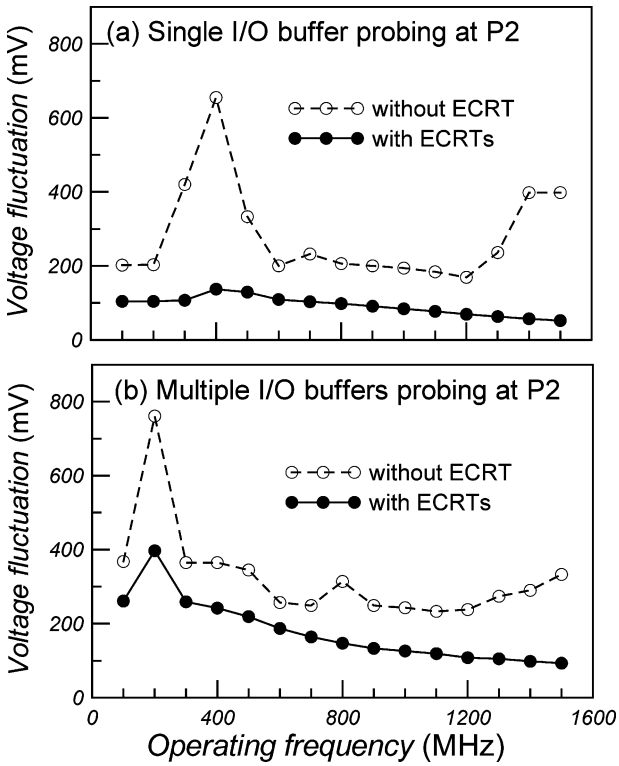

Fig. 8. Maximum voltage fluctuation detected at the end of one wing, P2, without ECRT (dashed lines with open circles) and with ECRT (solid lines with close dots) for (a) single and (b) multiple I/O buffers.

A. Improvement of the Power Integrity

Fig. 8(a) and (b) shows the noise suppression when probing at P2 for single and multiple I/O buffers, respectively. The dashed lines with open circles represent the original noise voltage fluctuation (without ECRT), and the solid lines with closed circles

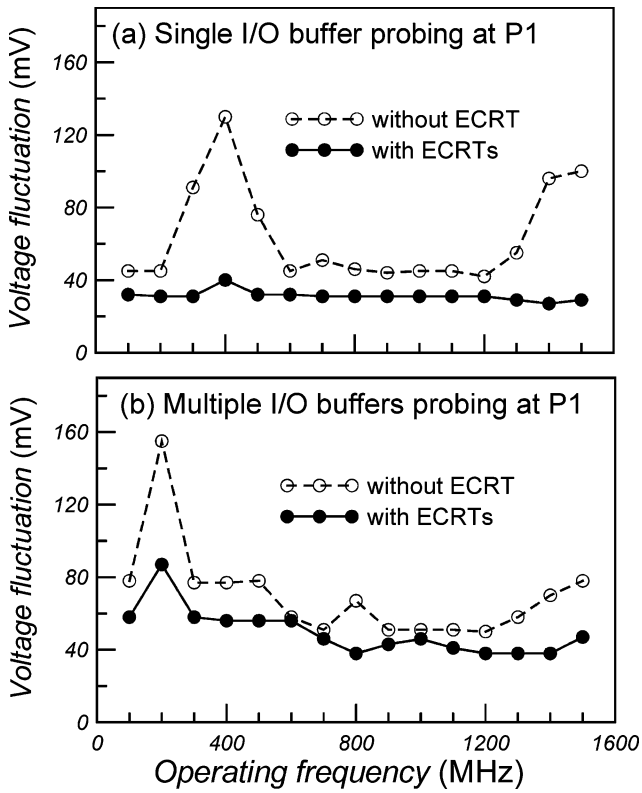

Fig. 9. Maximum voltage fluctuation detected at the end of the central stem, P1, without ECRT (dashed lines with open circles) and with ECRT (solid lines with closed dots) for (a) single and (b) multiple I/O buffers.

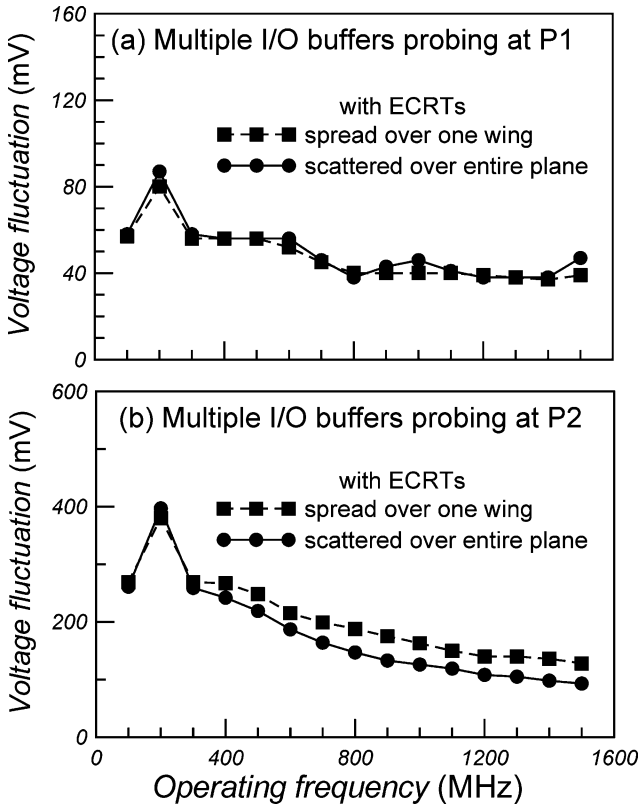

Fig. 10. Maximum voltage fluctuation for two placement configurations of the ECRT. The switching noise when the ECRTs are uniformly spread over one wing is represented by dashed lines with squares, while that when the ECRTs are scattered over the entire plane, as in Fig. 2(b), are represented by solid lines with dots. The results detected (a) at P1 and (b) at P2 are displayed.

represent the suppressed noise level when all four ECRTs are applied. The frequency of the peak noise is around 400 MHz in Fig. 8(a) and 200 MHz in Fig. 8(b). The resonant frequencies differ from the bare-board simulation results because the circuits are changed.

When multiple I/O buffers switch simultaneously, the overall noise level slightly exceeds that obtained with single I/O buffer switching, but these noise levels are not simply related by a multiplicative factor. Hence, the noise generated in each noise source, I/O buffer, is not always in phase with each other. The noise might diminish due to a certain level cancellation.

Fig. 8(a) shows rather favorable noise suppression performance, especially at resonance, where the noise was significant suppressed from 750 mV down to 150 mV. Fig. 8(b), referring to the case of multiple I/O buffers, reveals that this approach is still effective in suppressing the noise, but not as effectively as the single-buffer case. This is because the noise patterns in both cases differ. In the single-buffer case, the entire PDN is more like that in the bare-board, so a single resonant mode can be excited. However, when multiple I/O buffers switch simultaneously, the EM field distribution may be much more complex, reducing the effectiveness of the noise suppression. This implies the higher mode purity the better noise suppression.

B. Position Dependent Effect

Fig. 9(a) and (b) shows the voltage fluctuation versus the operating frequency when detected at another position, P1. All the parameters and settings are the same as in Fig. 8(a) and (b), except the detecting point is different (P1 in Fig. 9 and P2 in Fig. 8). Again, Fig. 9 displays a favorable noise suppression rate for single excitation, but for multiple excitations, the suppression rate is only moderately favorable.

The absolute noise levels obtained by probing at P2 and P1 differ dramatically, despite the fact that the suppression ratios are almost the same. Probing at P1 yields a lower voltage fluctuation than that at P2 for two reasons. The first is that P1 is close to the power supply, so the detected voltage seems to be stuck, instead of being dominated by the open-end boundary condition. The other reason is that once the noise is excited, it radiates to the surroundings. The width of the strip at P1 is wider than at P2, and so has larger effective capacitance, resulting in a much lower voltage fluctuation.

The mitigation ratios in Figs. 8 and 9, detecting at P2 and P1, exhibit the similar trend. This result supports our argument that the resonant PDN must be treated as an entire system. As the quality factor is reduced, the reduction rate of the fluctuated voltage must be the same at all points of the resonant system. However, the absolute values of the fluctuated voltages need not be the same. The absolute fluctuated voltage depends on the field distribution of the resonant mode.

C. Placement of the ECRT

Fig. 10 show the noise voltage fluctuation of multiple I/O buffers for two ECRT placements. The dashed lines with squares correspond to the uniform distribution of ECRT over one wing. The solid lines with dots correspond to scattered

ECRTs as shown in Fig. 2(b). The scattering of the ECRTs improves the power integrity, but not markedly.

Fig. 10(a) and (b) implies that the worst case generally occurs in the transient state and not in the steady state. In the transient state, the noise field pattern has not settled to a specific mode, and the noise is still scattered in the planar microstrip resonator. The results also reveal that although the resonant noise accumulation can be effectively diminished with ECRT, the transient noise interference could not be overlooked.

V. Conclusion

Analyzing the field pattern suggests the positions of placing ECRT for a specific mode. A significant reduction in the switching noise by placing the ECRT was demonstrated. Up to an 80% noise reduction was achieved at resonance when a single buffer was used, while an overall noise reduction of 50% was obtained when multiple I/O buffers switched simultaneously. In addition, two configurations of ECRT were investigated and shown not to differently affect noise absorption. This approach reduces the maximum noise level, especially at resonance, and suggests that a higher mode purity corresponds to more effective ECRTs.

The proposed ECRT scheme can effectively extract the unwanted RF noise without dissipating dc power. In addition to the proposed scheme, such circuit could be made in several ways, e.g., a lossy transmission line with open circuit at the end and a quarter-wavelength lossy trace. Among these approaches, the proposed scheme is the simplest and maybe the most cost effective.

The decoupling capacitor is generally regarded as the most effective means in stabilizing the dc voltage supply, but its use is limited to a low-frequency regime because of the presence of the ESL. However, the proposed ECRT scheme is used to extract the high-frequency noise, and serves as an auxiliary approach. The author does not seek to replace the decoupling capacitor with an ECRT. Rather, these two approaches should be used together to eliminate broad-band noise.

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Tsun-Hsu Chang (M'99) received the B.S. degree from National Central University, Chungli, Taiwan, R.O.C., and the Ph.D. degree from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1991 and 1999, respectively.

Upon graduation, he became a Postdoctor in the Physics Department for two years, and then he joined Silicon Integrated Systems Corporation (SiS), Taipei, Taiwan, R.O.C., for another two years. He is currently an Assistant Professor with the Department of Physics, National Tsing Hua University. From 1999 to 2001, he was a Postdoctor working on the development of high-power millimeter-wave sources (gyrotrons) as well as on the design and analysis of microwave/plasma reaction chambers (ECR). From 2001 to 2003, he served as a Technical Manager and was responsible for high-speed signal and power integrity analysis in both simulation and measurement. His current research focuses on the nonlinear dynamics and nonstationary behavior of the electron cyclotron maser and the characterization of the microwave/nanoparticle interaction.